

THREE PLLs BASED CLOCK GENERATOR FOR DIGITAL TV APPLICATIONS

FEATURES

- High Performance Clock Generator
- Clock Input Compatible With LVCMOS/LVTTL
- Requires a 54-MHz Input Clock to Generate Multiple Output Frequencies
- Low Jitter for Clock Distribution
- Generates the Following Clocks:
 - VIDCLK 74.175824 MHz/54 MHz (Buffered)
 - AUDCLK 16.9344 MHz/12.288 MHz
 - CPUCLK 64 MHz
 - ASICCLK 32 MHz
 - USBCLK 48 MHz
 - MCCLK 38.4 MHz/19.2 MHz/12 MHz
- Operates From Single 3.3-V Supply
- Low Peak-to-Peak Period Jitter (150 ps Max)
- PLLs Are Powered Down, if No Valid REF_IN Clock (< 5 MHz) is Detected or the V_{DD} is Below 2 V
- PLL Loop Filter Components Integrated
- Packaged in TSSOP (PW) 20-Pin Package
- Industrial Temperature Range -40°C to 85°C Applications

APPLICATIONS

- Digital Television With a Memory Card Interface

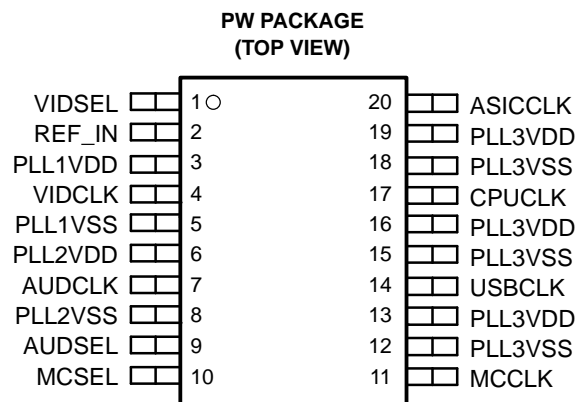
DESCRIPTION

The CDC5806 is a clock generator which synthesizes video clocks, audio clocks, CPU clock, ASIC clock, USB clock, and a memory card clock from a 54-MHz system clock.

Three phase-locked loops (PLLs) are used to generate the different frequencies from the system clock. On-chip loop filters and internal feedback eliminate the need for external components.

Since the CDC5806 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLLs. The PLL stabilization time begins after the reference clock input has a stable phase and frequency.

The device operates from a single 3.3-V supply voltage. The CDC5806 device is characterized for operation from -40°C to 85°C.

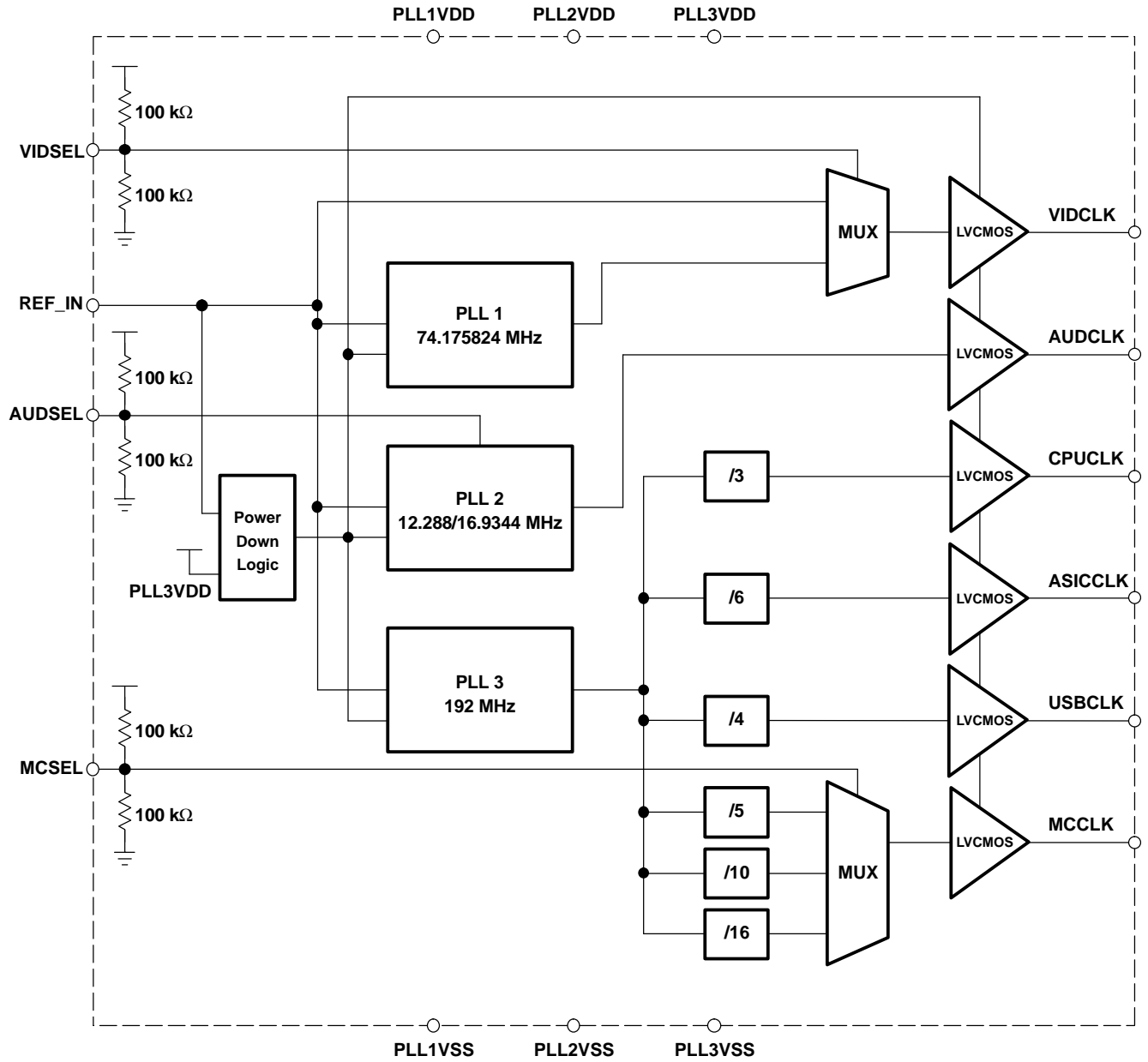


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	NO	TYPE	DESCRIPTION
REF_IN	2	I LVCMOS	Reference frequency input
VIDSEL	1	I LVCMOS	VIDSEL select input for VIDCLK. It selects between 74.175824 MHz from PLL1 and buffered input frequency of 54 MHz, 100k 100k pull to mid-level.
AUDSEL	9	I LVCMOS	AUDSEL select input for AUDCLK. It selects between 16.9344 MHz and 12.288 MHz from PLL2, 100k 100k pull to mid level.
MCSEL	10	I LVCMOS	MCSEL select input for MCCLK. It selects from 38.4 MHz, 19.2 MHz, and 12 MHz from PLL3, 100k 100k pull to mid level.
VIDCLK	4	O LVCMOS	VIDCLK output 74.175824 MHz or 54 MHz
AUDCLK	7	O LVCMOS	AUDCLK output 16.9344 MHz or 12.288 MHz
CPUCLK	17	O LVCMOS	CPUCLK output 64 MHz
ASICCLK	20	O LVCMOS	ASICCLK output 32 MHz
USBCLK	14	O LVCMOS	USBCLK output 48 MHz
MCCLK	4	O LVCMOS	MCCLK output 38.4 MHz / 19.2 MHz / 12 MHz
VDD_PLL1	3	Power	3.3-V supply for PLL1 and VIDCLK
VDD_PLL2	6	Power	3.3-V supply for PLL2 and AUDCLK
VDD_PLL3	13, 16, 19	Power	3.3-V supply for PLL3 and CPUCLK, ASICCLK, USBCLK, and MCCLK
VSS_PLL1	5	Ground	Ground for PLL1 and VIDCLK
VSS_PLL2	8	Ground	Ground for PLL2 and AUDCLK
VSS_PLL3	12, 15, 18	Ground	Ground for PLL3 and CPUCLK, ASICCLK, USBCLK, and MCCLK

FUNCTIONAL DESCRIPTION OF THE LOGIC

Table 1. Select Function for Video, Audio, CPU, ASIC, and USB Clocks

VIDSEL	AUDSEL	VIDCLK	AUDCLK	CPUCLK	ASICCLK	USBCLK	Unit
L	L	54 (buffered)	12.288	64	32	48	MHz
L	M	Reserved	Reserved	64	32	48	MHz
L	H	54 (buffered)	16.9344	64	32	48	MHz
M	L	Reserved	Reserved	64	32	48	MHz
M	M	Reserved	Reserved	REFCLK/3	REFCLK/6	REFCLK/4	MHz
M	H	Reserved	Reserved	64	32	48	MHz
H	L	74.175824	12.288	64	32	48	MHz
H	M	Reserved	Reserved	64	32	48	MHz
H	H	74.175824	16.9344	64	32	48	MHz

Table 2. Select Function for MC Clock

MCSEL	MCCLK	MCCLK if VIDSEL = M and AUDSEL = M	UNIT
H	12 MHz	REFCLK/16	MHz
M	38.4 MHz	REFCLK/5	MHz
L	19.2 MHz	REFCLK/10	MHz

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)⁽¹⁾

Supply voltage range, V_{DD}	0.5 V to 4.6 V
Input voltage range, V_I ⁽²⁾	0.5 V to $V_{DD} + 0.5$ V
Output voltage range, V_O ⁽²⁾	0.5 V to $V_{DD} + 0.5$ V
Input current ($V_I < 0$, $V_I > V_{DD}$)	± 20 mA
Continuous output current, I_O	± 50 mA
Package thermal impedance, θ_{JA} ⁽³⁾ : TSSOP20 package	104 C/W
Storage temperature range T_{stg}	65°C to 150°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51 (no airflow condition) and JEDEC2S1P (high-k board).

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V_{DD} Supply voltage	3	3.3	3.6	V
T_A Operating free-air temperature	-40		85	°C
V_{IL} Low-level input voltage REF_IN			0.3 V_{DD}	V
$V_{I\text{ thresh}}$ Input voltage threshold REF_IN		0.5 V_{DD}		V
V_{IH} High-level input voltage REF_IN	0.7 V_{DD}			V
$V_{IL(L)}$ Three level input low for control inputs			0.13 V_{DD}	V
$V_{IM(M)}$ Three level input mid for control inputs	0.4 V_{DD}		0.6 V_{DD}	V
$V_{IH(H)}$ Three level input high for control inputs	0.87 V_{DD}			V
I_{OH} High-level output current LVCMOS			-8	mA
I_{OL} Low-level output current LVCMOS			8	mA
V_I Input voltage range LVCMOS	0		3.6	V
C_L Output load LVCMOS	5		10	pF

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature

PARAMETER	MIN	NOM	MAX	UNIT
REF_IN REQUIREMENTS				
f_{CLK_IN} LVCMOS REF_IN clock input frequency		54		MHz
t_r / t_f Rise and fall time REF_IN signal (20% to 80%)			4	ns
duty _{REF} Duty cycle of REF_IN ($V_{DD}/2$)	40%		60%	
AUDSEL, VIDSEL, MCSEL REQUIREMENTS				
t_r / t_f Rise and fall time (20% to 80%)			4	ns
t_1 Transitional time between AUDSEL and VIDSEL control pins ⁽¹⁾	6			ns

- (1) If VIDSEL and AUDSEL are switched from from one state to another state at the same time, then the CPUCLK, ASICCLK, USBCLK, or MCCLK are affected. This is due to the selected reserved mode with VIDSEL = M and AUDSEL = M. This mode causes the PLL3 to be bypassed and the REFCLK will be seen with the appropriate divider ratios at the correspondent outputs.

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OVERALL							
I_{CC}	Supply current	Test load		35	45	mA	
$I_{CC(ST)}$	Standby current	$f_{IN} = 0$ MHz, $V_{DD} = 3.6$ V			1.1	mA	
V_{PUC}	Supply voltage threshold for power up control circuit			2		V	
LVCMOS							
V_{IK}	LVCMOS input voltage	$V_{DD} = 3$ V, $I_I = -18$ mA			-1.2	V	
I_I	REF_IN input current	$V_I = 0$ V or V_{DD}			± 5	μ A	
I_I	SELECT input current	$V_I = 0$ V or V_{DD}			± 55	μ A	
V_{OH}	High-level output voltage	$V_{DD} = \text{MIN to MAX}$, $I_{OH} = -5$ mA	$V_{DD} - 0.4$			V	
V_{OL}	Low-level output voltage	$V_{DD} = \text{MIN to MAX}$, $I_{OL} = 5$ mA			0.4	V	
I_{OH}	High-level output current	$V_{DD} = 3$ V, $V_O = V_{DD} - 0.4$ V		-5		mA	
		$V_{DD} = 3.3$ V, $V_O = 1.65$ V			-35		
		$V_{DD} = 3.6$ V, $V_O = 0.4$ V					-75
I_{OL}	Low-level output current	$V_{DD} = 3$ V, $V_O = 0.4$ V		5		mA	
		$V_{DD} = 3.3$ V, $V_O = 1.65$ V			35		
		$V_{DD} = 3.6$ V, $V_O = V_{DD} - 0.4$ V					75
AC							
C_I	Input capacitance (Ref_IN)			2		pF	
f_{err}	Output accuracy VIDCLK, CPUCLK, ASICCLK, USBCLK, MCCLK (38.4 MHz, 19.2 MHz, 12 MHz)	See Note (1)			± 1	ppm	
f_{err}	Output accuracy AUDCLK (16.9344 MHz, 12.288 MHz)	See Note (1)			± 40	ppm	
t_L	PLL start up lock time	See Figure 2			0.5	ms	
$t_{L(\omega)}$	PLL lock time after frequency change on AUDCLK	See Figure 2			0.5	ms	
odc	Duty cycle for MCCLK	Threshold = $V_{DD}/2$	47%	50%	53%		
odc	Duty cycle for VIDCLK, AUDCLK, CPUCLK, ASICCLK, USBCLK	Threshold = $V_{DD}/2$	45%	50%	55%		
t_r/t_f	Rise and fall time of the output	20%–80% of V_O			2	ns	
$t_{jit(per)}$	Peak-to-peak period jitter for	VIDCLK (74.175824 MHz)	10,000 cycles		75	150	ps
		CPUCLK (64 MHz)			60	150	
		USBCLK (48 MHz)			65	150	
		MCCLK (38.4 MHz)			65	150	
		ASICCLK (32 MHz)			60	150	
		MCCLK (19.2 MHz)			70	150	
		AUDCLK (16.9344 MHz)			75	150	
		AUDCLK (12.288 MHz)			85	150	
MCCLK (12 MHz)		65	150				

(1) This parameter is assured by design as a result of the chosen settings of the internal dividers in the PLL's.

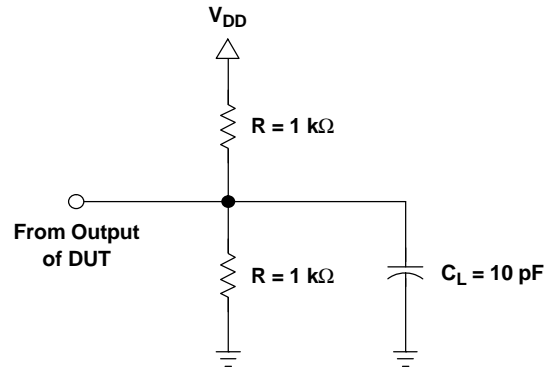


Figure 1. LVC MOS Output Test Load

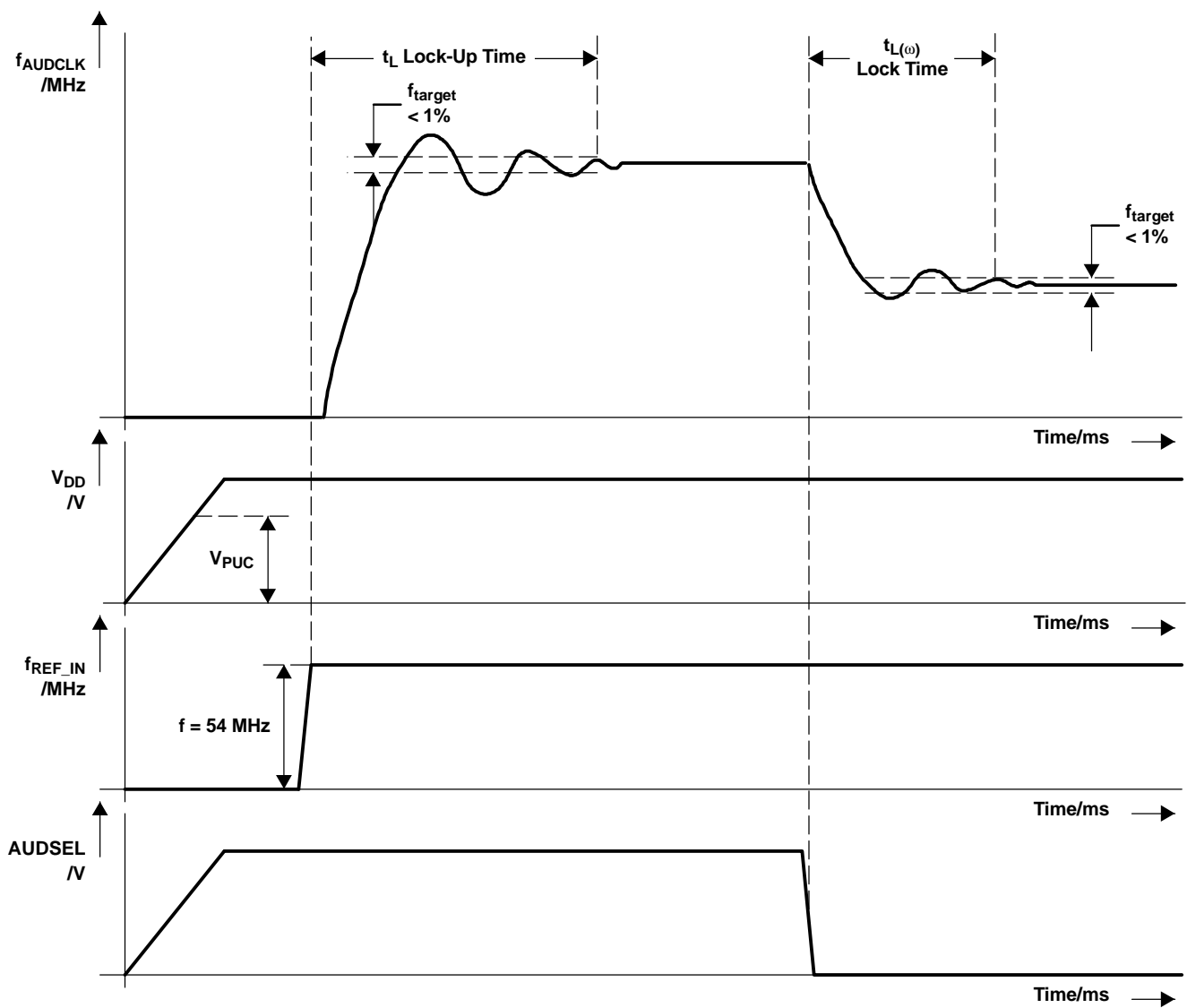


Figure 2. Timing Diagram of PLL Lock Time of Audio Clock

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC5806PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC5806PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC5806PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC5806PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

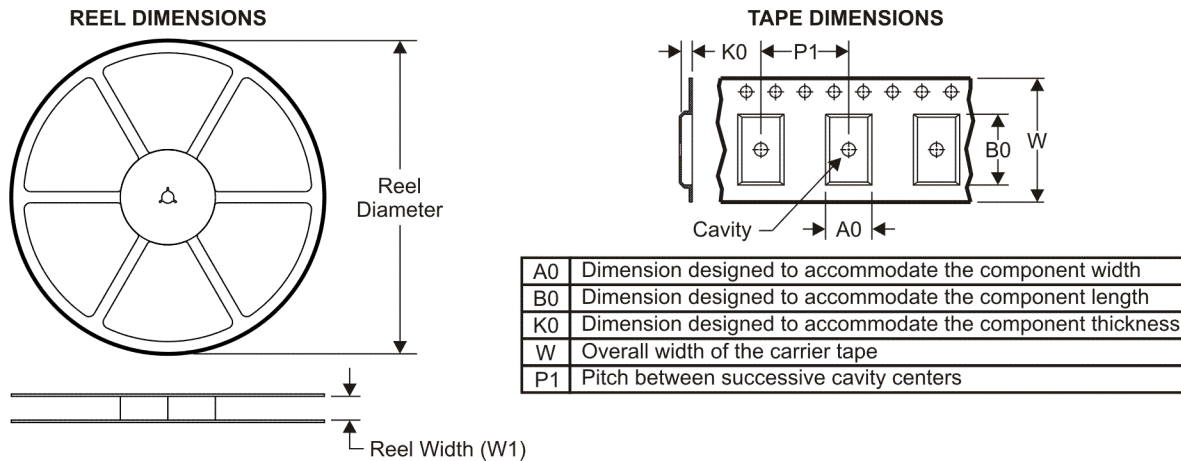
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

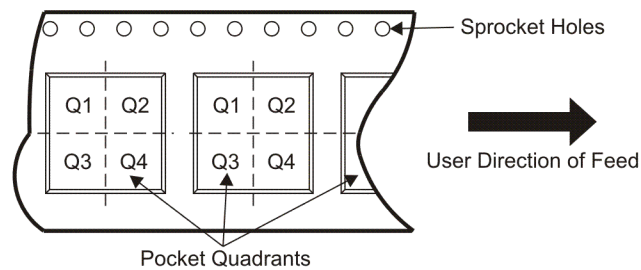
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC5806PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

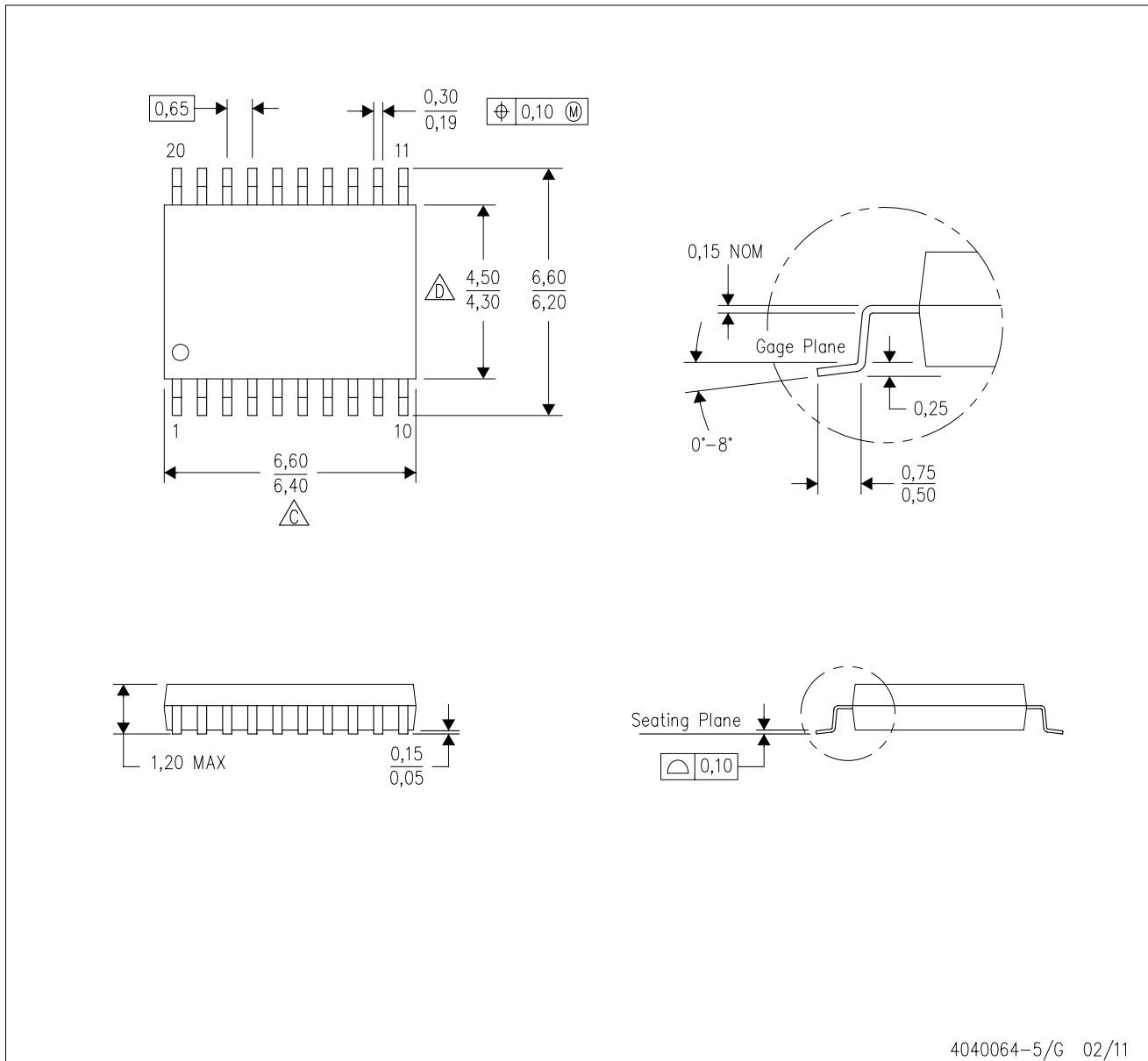


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC5806PWR	TSSOP	PW	20	2000	333.2	345.9	28.6

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

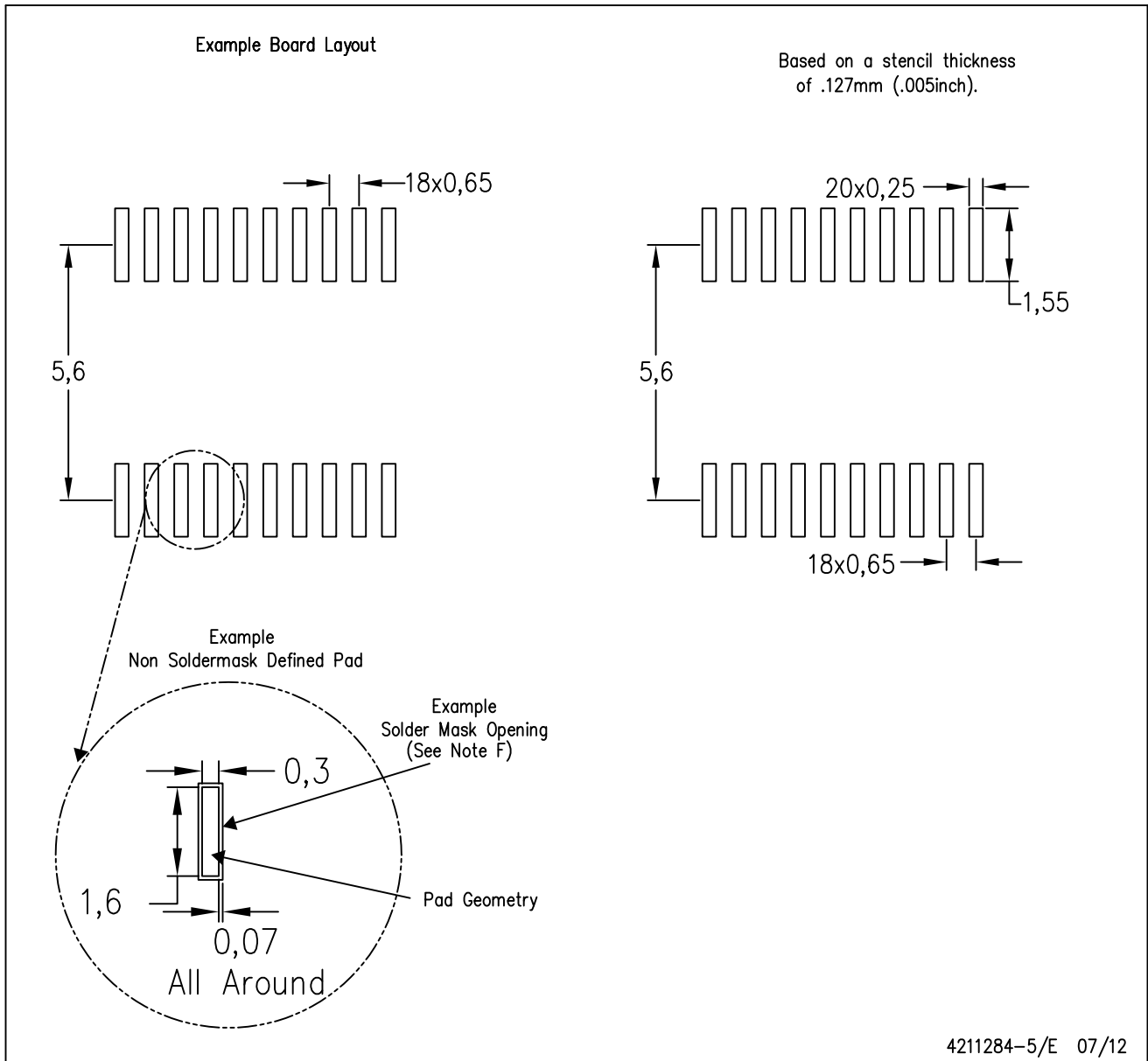


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated