SCAS782B - SEPTEMBER 2004 - REVISED JANUARY 2008

		50A5762D - 5EI				
•	Qualified for Automotive Applications Operates From 1.65 V to 3.6 V	D OR PW PACKAGE (TOP VIEW)				
•	Inputs Accept Voltages to 5.5 V	1 <u></u> 1 <u></u> 1				
٠	Max t _{pd} of 6.2 ns	1A 🛛 2	15 2 2 G			
•	Typical V _{OLP} (Output Ground Bounce) <0.8 V at V _{CC} = 3.3 V, T _A = 25°C	1B [] 3 1Y0 [] 4	14] 2A 13] 2B			
•	Typical V _{OHV} (Output V _{OH} Undershoot) >2 V at V _{CC} = 3.3 V, T _A = 25°C	1Y1 []5 1Y2 []6	12 2Y0 11 2Y1			
•	Latch-Up Performance Exceeds 250 mA Per JESD 17	1Y3 [7 GND [8	10 2Y2 9 2Y3			
•	ESD Protection Level Per AEC-Q100					

- Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine Model
 - 1000-V (C5) Charged-Device Model

description/ordering information

This dual 2-line to 4-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION[†]

T _A	PACK	AGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC139AQDRQ1	LVC139AQ	
-40 C to 125°C	TSSOP – PW	Reel of 2000	SN74LVC139AQPWRQ1	LC139AQ	

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLE

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(each decoder/demultiplexer)											
	INPUTS			OUTPUTS							
G	SEL	ECT		0011	-015						
G	в	Α	Y3	Y2	Y1	Y0					
L	LL		Н	Н	Н	L					
L	L	н	Н	н	L	Н					
L	H L		н	L	Н	н					
L	н	Н	L	Н	Н	Н					
Н	Х	Х	Н	Н	Н	Н					



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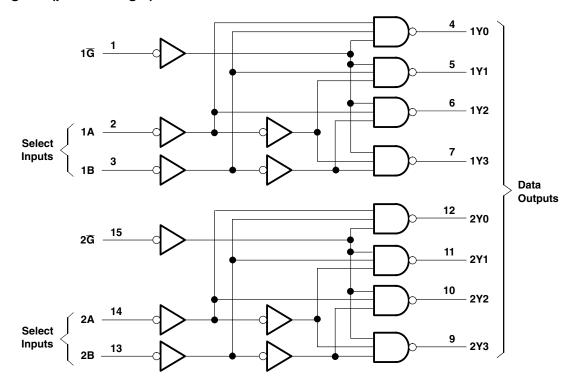
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SCAS782B - SEPTEMBER 2004 - REVISED JANUARY 2008

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V _O (see Notes 1 and 2)	\dots –0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): PW package	108°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The value of V_{CC} is provided in the recommended operating conditions table.

3. The package thermal impedance is calculated in accordance with JESD 51-7.



SCAS782B - SEPTEMBER 2004 - REVISED JANUARY 2008

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
.,		Operating	1.65	3.6		
V _{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 imes V_{CC}$			
VIH	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
VIL	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
		$V_{CC} = 2.3 V$		-8	4	
I _{ОН}	High-level output current	$V_{CC} = 2.7 V$		-12	- mA	
		$V_{CC} = 3 V$		-24		
		V _{CC} = 1.65 V		4		
		$V_{CC} = 2.3 V$		8		
I _{OL}	Low-level output current	$V_{CC} = 2.7 V$		12	mA	
		$V_{CC} = 3 V$		24	7	
Δt/Δv	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature		-40	125	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				$T_{A} = -40^{\circ}$	°C TO 12	5°C	T _A = -40	°C TO 8	5°C	
PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2			
		I _{OH} = -4 mA	1.65 V	1.2			1.2			
		I _{OH} = -8 mA	2.3 V	1.7			1.7			
V _{OH}		1 10 A	2.7 V	2.1			2.2			V
		I _{OH} = -12 mA	3 V	2.3			2.4			
		I _{OH} = -24 mA	3 V	2.1			2.2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2			0.2	
		I _{OL} = 4 mA	1.65 V			0.45			0.45	
VOL		I _{OL} = 8 mA	2.3 V			0.7			0.7	V
		I _{OL} = 12 mA	2.7 V			0.4			0.4	
		I _{OL} = 24 mA	3 V			0.55			0.55	
l _l	All inputs	V _I = 5.5 V or GND	3.6 V			±5			±5	μA
I _{CC}	-	$V_{I} = V_{CC} \text{ or GND}, I_{O} = 0$	3.6 V			10			10	μA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500			500	μA
Ci		V _I = V _{CC} or GND	3.3 V		5			5		pF

 † All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS782B - SEPTEMBER 2004 - REVISED JANUARY 2008

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
	A or B	X	1	8.8	1	7.7	
t _{pd}	G	Ŷ	1	6.7	1	6.2	ns
t _{sk(o)}						1	ns

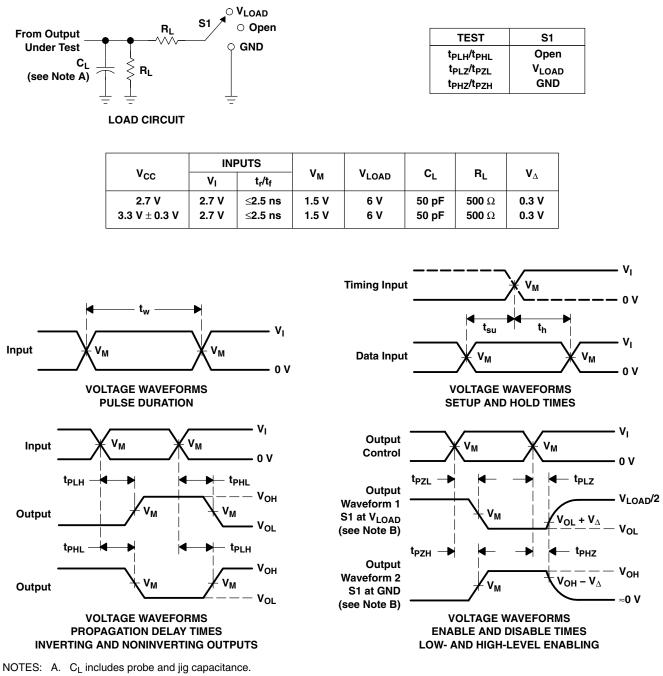
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST	V _{CC} = 1.8 V	V_{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		CONDITIONS	ТҮР	TYP	ТҮР	UNIT
Cp	Power dissipation capacitance	f = 10 MHz	28.5	29.5	30.5	pF

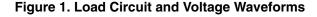


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PARAMETER MEASUREMENT INFORMATION



- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.







11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
CLVC139AQPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC139AQ	Samples
SN74LVC139AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC139AQ	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC139A-Q1 :



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PACKAGE OPTION ADDENDUM

11-Apr-2013

• Catalog: SN74LVC139A

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC139AQPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC139AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

14-Mar-2013



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC139AQPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LVC139AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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