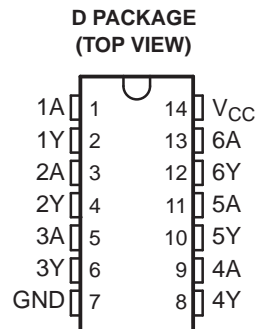


FEATURES

- **Controlled Baseline**
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- **Extended Temperature Performance of -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Operates From 1.65 V to 3.6 V**
- **Inputs and Open Drain Outputs Accept Voltages up to 5.5 V**
- **Max t_{pd} of 3.7 ns at 3.3 V**
- **I_{off} Supports Partial Power Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



DESCRIPTION/ORDERING INFORMATION

The SN74LVC06A is a hex inverter buffer/driver that is designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the SN74LVC06A device are open drain and can be connected to other open-drain outputs to implement active low wired OR or active high wired AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V system environment.

This device is fully specified for partial power down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLE
(EACH INVERTER)**

INPUT A	OUTPUT Y
H	L
L	H

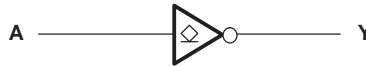


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SN74LVC06A-EP HEX INVERTER BUFFER/DRIVER WITH OPEN DRAIN OUTPUTS

SCAS832A—APRIL 2007—REVISED MAY 2007

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOIC – D	Reel of 2500	SN74LVC06AMDREP	LVC06AM

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	6.5	V	
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V	
V _O	Output voltage range	-0.5	6.5	V	
I _{IK}	Input clamp current	V _I < 0 V		-50	mA
I _{OK}	Output clamp current	V _O < 0 V		-50	mA
I _O	Continuous output current			±50	mA
Continuous current through V _{CC} or GND				±100	mA
θ _{JA}	Package thermal impedance ⁽³⁾			86	°C/W
T _{stg}	Storage temperature range	-65	150	°C	
P _{tot}	Power dissipation ⁽⁴⁾	T _A = -55°C to 125°C		500	mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Above 70°C the value of P_{tot} derates linearly with 8 mW/K.

Recommended Operating Conditions⁽¹⁾

		T _A = 25°C		-55°C to 125°C		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	V	
V _O	Output voltage	0	5.5	0	5.5	V	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions (continued)

		T _A = 25°C		–55°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	4	mA	
		V _{CC} = 2.3 V	8	8		
		V _{CC} = 2.7 V	12	12		
		V _{CC} = 3 V	24	24		

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.1		0.3	V
	I _{OL} = 4 mA	1.65 V			0.24		0.6	
	I _{OL} = 8 mA	2.3 V			0.3		0.75	
	I _{OL} = 12 mA	2.7 V			0.4		0.6	
	I _{OL} = 24 mA	3 V			0.55		0.8	
I _I	V _I = 5.5 V or GND	3.6 V			±1		±20	μA
I _{off}	V _I or V _O = 5.5 V	0 V			±1		±20	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			1		40	μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500		5000	μA
C _I	V _I = V _{CC} or GND	3.3 V		5				pF

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

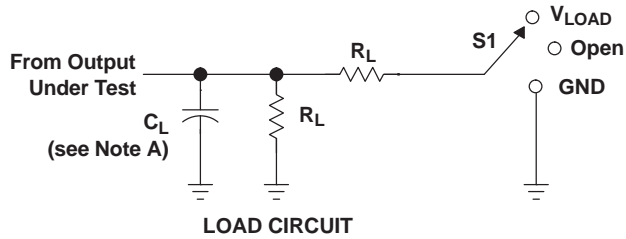
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	1.4	3	5.1	1.4	7.6	ns
			2.5 V ± 0.2 V	1	1.9	2.8	1	4	
			2.7 V	1	2.4	3.7	1	5	
			3.3 V ± 0.3 V	1	2.2	3.5	1	5	

Operating Characteristics

T_A = 25°C

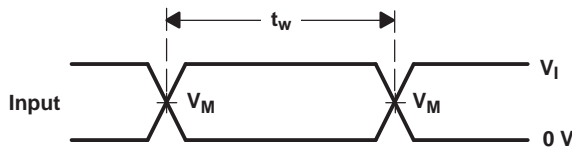
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer/driver	f = 10 MHz	1.8 V	2.1	pF
			2.5 V	2.3	
			3.3 V	2.5	

PARAMETER MEASUREMENT INFORMATION

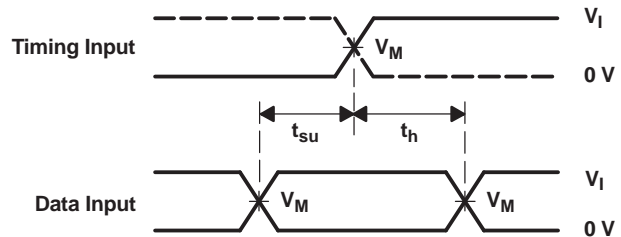


TEST	S1
t_{pZL} (see Notes E and F)	V_{LOAD}
t_{pLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

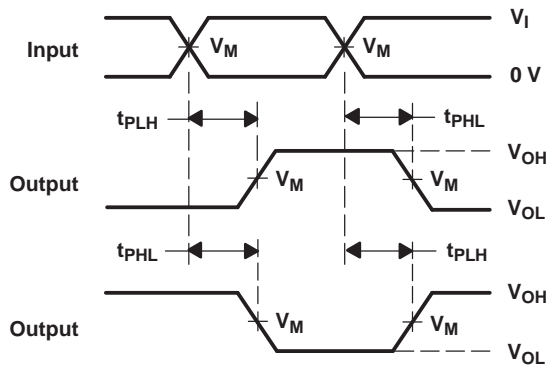
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



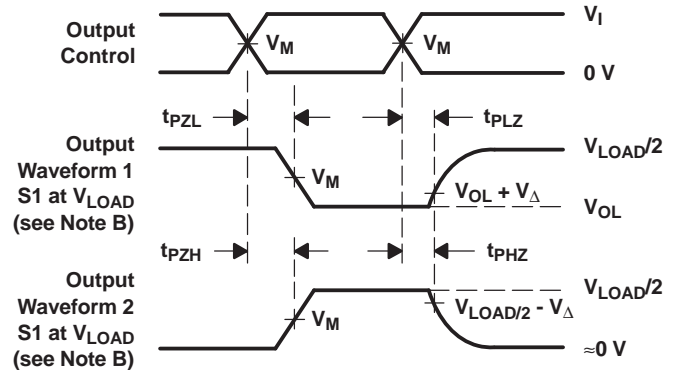
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
F. t_{pZL} is measured at V_M .
G. t_{pLZ} is measured at $V_{OL} + V_{\Delta}$.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC06AMDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06661-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC06A-EP :

- Catalog: [SN74LVC06A](#)
- Automotive: [SN74LVC06A-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC06AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC06AMDREP	SOIC	D	14	2500	333.2	345.9	28.6

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

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