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28-BIT TO 56-BIT REGISTERED BUFFER WITH ADDRESS-PARITY TEST

FEATURES

- Member of the Texas Instruments
 Widebus+ ™Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- 1-to-2 Outputs Supports Stacked DDR2 DIMMs
- One Device Per DIMM Required
- Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Supports SSTL_18 Data Inputs
- Differential Clock (CLK and CLK) Inputs

- Supports LVCMOS Switching Levels on the Chip-Select Gate-Enable, Control, and RESET Inputs
- Checks Parity on DIMM-Independent Data Inputs
- Supports Industrial Temperature Range (-40°C to 85°C)
- RESET Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low, Except QERR

APPLICATIONS

DDR2 registered DIMM

DESCRIPTION

This 28-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. One device per DIMM is required to drive up to 18 SDRAM loads or two devices per DIMM are required to drive up to 36 SDRAM loads.

All inputs are SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset (RESET) inputs, which are LVCMOS. All outputs are edge-controlled <u>circuits</u> optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error (QERR) output.

The 74SSTUB32868 operates from a differential clock (CLK and CLK). Data are registered at the crossing of CLK going high and CLK going low.

The 74SSTUB32868 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1-D5, D7, D9-D12, D17-D28 when C = 0; or D1-D12, D17-D20, D22, D24-D28 when C = 1) and indicates whether a parity error has occurred on the open-drain \overline{QERR} pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

The 74SSTUB32868 includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. Two clock cycles after the data are registered, the corresponding QERR signal is generated.

ORDERING INFORMATION

T _A	PACK	PACKAGE ⁽¹⁾		TOP-SIDE MARKING
-40°C to 85°C	TFBGA-ZRH	Tape and Reel	74SSTUB32868ZRHR	SB868

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity error duration or until RESET is driven low. If a parity error occurs on the clock cycle before the device enters the low-power mode (LPM) and the QERR output is driven low, it stays latched low for the LPM duration plus two clock cycles or until RESET is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, DCS0 and DCS1) are not included in the parity check computation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hard-wired to a valid low or high level to configure the register in the desired mode.

In the DDR2 RDIMM application, RESET is specified to be completely asynchronous with respect to CLK and CLK. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared and the data outputs is driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the 74SSTUB32868 must ensure that the outputs remain low, thus ensuring no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The device supports low-power standby operation. When \overline{RESET} is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when RESET is low, all registers are reset and all outputs are forced low except QERR. The LVCMOS RESET and C inputs always must be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{DCS0}$ and $\overline{DCS1}$) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, $\overline{DCS0}$, and $\overline{DCS1}$ inputs are high. If CSGEN, $\overline{DCS0}$ or $\overline{DCS1}$ input is low, the Qn outputs function normally. Also, if both $\overline{DCS0}$ and $\overline{DCS1}$ inputs are high, the device will gate the \overline{QERR} output from changing states. If either $\overline{DCS0}$ or $\overline{DCS1}$ is low, the QERR output functions normally. The \overline{RESET} input has priority over the $\overline{DCS0}$ and $\overline{DCS1}$ control and when driven low forces the Qn outputs low, and the \overline{QERR} output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{DCS0}$ and $\overline{DCS1}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{DCS0}$ and $\overline{DCS1}$ only, then the CSGEN input should be pulled up to V_{CC} through a pullup resistor.

The two V_{REF} pins (A5 and AB5) are connected together internally by approximately 150 Ω . However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V _{CC}	Supply voltage range		-0.5 to 2.5	V
VI	Input voltage range (see notes (2) and (3))		-0.5 to $V_{CC} + 0.5$	V
Vo	Output voltage range (see notes (2) and (3))		-0.5 to $V_{CC} + 0.5$	V
I _{IK}	Input clamp current (V _I < 0, V _I > V _{CC})		±50	mA
I _{OK}	Output clamp current (V _I < 0, V _O > V _{CC})		±50	mA
lo	Continuous output current (V _O = 0 to V _{CC})		±50	mA
I _{CC}	Continuous current through each V _{CC} or GND		±100	mA
D	Thermal registeres innotice to embient (see note (4))	No airflow	46.8	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient (see note ⁽⁴⁾)	Airflow 200 ft/min	42.9	k/W
$R_{\theta JC}$	Thermal resistance, junction-to-case (see note (4))	No airflow	17.9	
T _{stg}	Storage temperature range	·	-65 to 150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
SUPPLY	Y VOLTAGES, CURRENTS AND	TEMPERATURE RANGE	1		1	
V _{CC}	Supply voltage		1.7		1.9	V
V_{REF}	Reference voltage		0.49 x V _{CC}	0.5 x V _{CC}	0.51 x V _{CC}	V
V _{TT}	Termination voltage		V _{REF} - 40 mV	V_{REF}	V _{REF} + 40 mV	V
VI	Input voltage		0		V _{CC}	V
V _{IH}	AC high-level input voltage	Data inputs, DCSn, PAR_IN	V _{REF} + 250 mV			V
V_{IL}	AC low-level input voltage	Data inputs, DCSn, PAR_IN			V _{REF} - 250 mV	V
V _{IH}	DC high-level input voltage	Data inputs, DCSn, PAR_IN	V _{REF} + 125 mV			V
V _{IL}	DC low-level input voltage	Data inputs, DCSn, PAR_IN			V _{REF} - 125 mV	V
V_{IH}	High-level input voltage	RESET, CSGEN, C	0.65 x V _{CC}			V
V _{IL}	Low-level input voltage	RESET, CSGEN, C			0.35 x V _{CC}	V
V_{ICR}	Common-mode input voltage range	CLK, CLK	0.675		1.125	٧
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	0.6			V
I _{OH}	High-level output current	Q outputs			-8	mA
I _{OL} Low-level output current	Q outputs			8	mΛ	
	Low-level output current	QERR output	30			mA
T _A	Operating free-air temperature		-40		85	°C

⁽¹⁾ The RESET and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless RESET is low. See the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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⁽²⁾ The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

³⁾ This value is limited to 2.5 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

I	PARAMETER	TEST CONDITION		V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
V	Q outputs	I _{OH} = -100 μA		1.7 V to 1.9 V	V _{CC} - 0.2			V
V _{OH}	Q outputs	I _{OH} = -6 mA		1.7 V	1.2			V
	Q outputs	I _{OL} = 100 μA	1.7 V to 1.9 V			0.2		
V_{OL}	Q outputs	I _{OL} = 6 mA		1.7 V			0.5	V
	QERR	I _{OL} = 25 mA		1.7 V			0.5	
PAR_IN		$V_I = GND$					-5	
I	PAR_IN	$V_I = V_{CC}$		1.9 V			25	μΑ
	All other inputs ⁽²⁾	$V_I = V_{CC}$ or GND					±5	
I _{OZ}	QERR outputs	$V_O = V_{CC}$ or GND	V _O = V _{CC} or GND				±10	μΑ
	Static standby (3)	RESET = GND					200 (3)	μΑ
I _{CC}	Static operating	$\overline{\text{RESET}} = V_{CC}, VI = V_{IH(AC)} \text{ or } V_{IL(AC)}$	I _O = 0	1.9 V			80	mA
	Dynamic operating – clock only	namic operating – $\frac{\overline{RESET} = V_{CC}, VI = V_{IH(AC)}}{V_{IL(AC)}, CLK}$ and $\frac{\overline{CLK}}{Switching}$ so duty cycle			64		μΑ/MHz	
I _{CC(D)}	Dynamic operating – per each data input		I _O = 0	1.8 V		37		μΑ/clock MHz/ D inputs
	Chip-select-enabled low-power active mode – clock only	$\overline{\text{RESET}} = \text{V}_{\text{CC}}, \ \text{VI} = \text{V}_{\text{IH}(\text{AC})} \text{ or} \\ \text{V}_{\text{IL}(\text{AC})}, \text{CLK} \text{ and } \overline{\text{CLK}} \text{ switching} \\ 50\% \text{ duty cycle}$				68		μA/MHz
I _{CC(DLP)}	Chip-select-enabled low-power active mode	$\label{eq:RESET} \hline \textbf{RESET} = \textbf{V}_{\text{CC}}, \textbf{V}_{\text{L}} = \textbf{V}_{\text{IH}(\text{AC})} \text{ or } \\ \textbf{V}_{\text{IL}(\text{AC})}, \text{ CLK and } \overrightarrow{\text{CLK}} \text{ switching } \\ 50\% \text{ duty cycle, One data input } \\ \textbf{switching at one half clock} \\ \text{frequency, 50% duty cycle} \\ \hline $	l _O = 0	1.8 V		2.7		μΑ/clock MHz/ D inputs
	Data inputs, DCSn, PAR_IN, CSGEN	V _I = V _{REF} ±250 mV			2	2.5	3	_
Cı	CLK, CLK	$V_{ICR} = 0.9 \text{ V}, V_{I(PP)} = 600 \text{ mV}$		1.8 V	2		3 pF	
	RESET	V _I = V _{CC} or GND				4		

 ⁽¹⁾ All typical values are at V_{CC} = 1.8 V, T_A = 25°C.
 (2) Each V_{REF} pin (A5 or AB5) should be tested independently, with the other (untested) pin open.
 (3) The maximum static standby current I_{CC} is 100 μA if the device is exposed to commercial temperature range (0°C to 70°C) only. For industrial temperature range (-40°C to 85°C), the static I_{CC} is 200 μA .



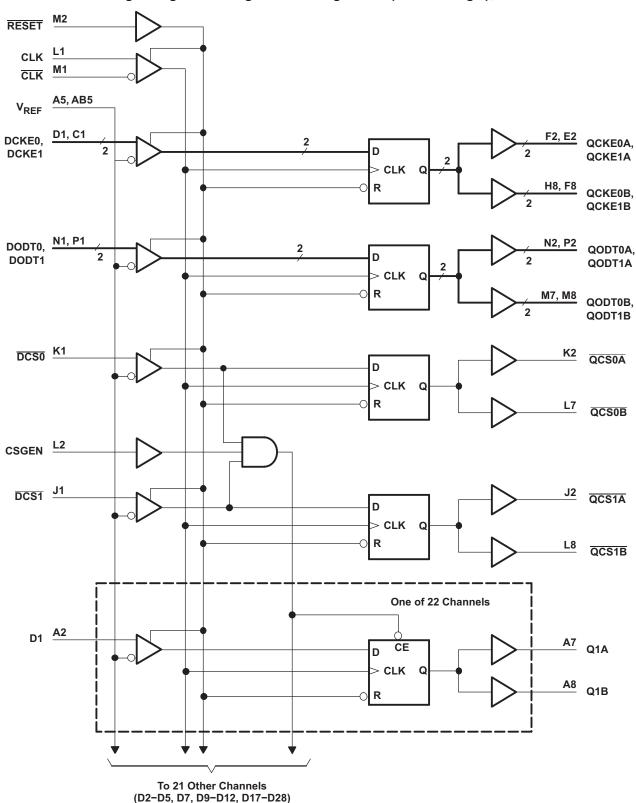
PACKAGE (TOP VIEW) Terminal Assignment for Register-A (C = 0) 5 7 2 3 4 8 1 2 3 4 5 6 7 8 1 V_{REF} D₂ С **GND GND** Q1A Q₁B Α **D1** 000000000Α V_{CC} V_{CC} В D4 D3 V_{CC} v_{cc} Q2A Q2B 000000000В D6 00000000 С Q3A Q3B С D5 **GND GND GND GND** (DCKE1) 00000000 D **D8** v_{cc} v_{cc} v_{cc} D D7 v_{cc} Q4A Q4B (DCKE0) 00000000 Ε Q6A 000000000Е D9 **GND GND GND GND** Q5A Q5B F (QCKE1A) 00000000 G Q8A Q6B $\mathbf{v}_{\mathbf{cc}}$ v_{cc} v_{cc} v_{cc} Q7A F D10 (QCKE0A) (QCKE1B) Н 00000000 00000000 G D11 Q10A **GND** GND **GND GND** Q9A Q7B J Q8B 000000000Κ н D12 Q12A Vcc V_{CC} V_{CC} V_{CC} Q11A (QCKE0B) 00000000 L D13 Q13A Q10B J **GND** GND **GND GND** Q9B 0000000000М (DCS1) (QCS1A) 00000000 Ν D14 **Q14A** v_{cc} v_{cc} K v_{cc} v_{cc} **Q12B** Q11B (DCS0) (QCS0A) Р 00000000 Q14B Q13B PAR_IN **GND GND GND** R 000000000L CLK **CSGEN** (QCS0B) (QCS1B) Т 000000000Q15B Q16B **QERR** v_{cc} v_{cc} V_{CC} M CLK RESET (QODT0B) (QODT1B) 000000000U D15 Q15A ٧ 00000000 **GND** GND **GND GND** Q17B Q18B Ν (DODT0) (QODT0A) W 00000000 D16 Q16A v_{cc} v_{cc} V_{CC} V_{CC} Q19B Q20B Р 00000000 (DODT1) (QODT1A) Υ Q17A 000000000D17 **GND GND GND GND** Q18A **Q21B** R AA AB 000000000Т Q19A v_{cc} v_{cc} V_{CC} V_{CC} Q20A Q22B **D18 Q23B** U D19 **Q21A GND GND GND GND** Q22A v_{cc} v_{cc} V_{CC} V_{CC} ν Q23A D20 Q24A Q24B **GND GND** Q25A Q25B W **D21 D22 GND** GND V_{CC} V_{CC} Υ D23 D24 V_{CC} v_{cc} Q26A **Q26B D25 D26 GND** GND **GND** GND **Q27A Q27B** AA v_{cc} v_{cc} NC V_{REF} **Q28A Q28B** AΒ **D27 D28**

A. Each pin name in parentheses indicates the DDR2 DIMM signal name.

B. NC - No internal connection.

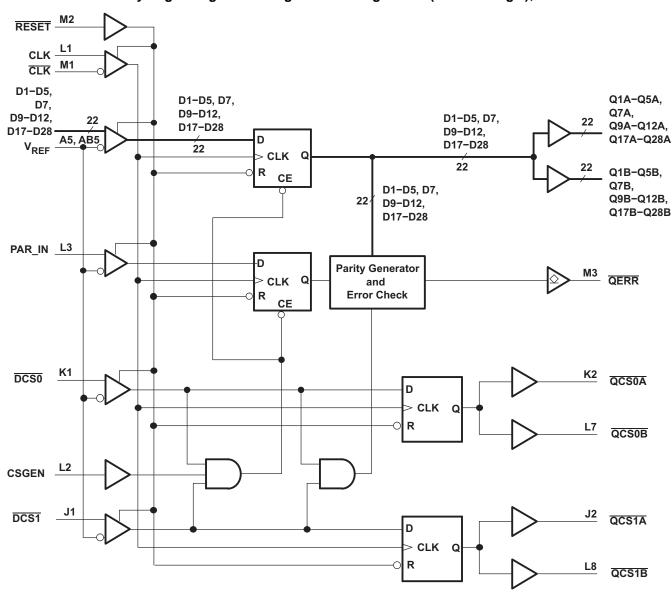


Logic Diagram for Register-A Configuration (Positive Logic); C = 0





Parity Logic Diagram for Register-A Configuration (Positive Logic); C = 0



8



7

	PACKAGE
((TOP VIEW)

Terminal Assignment for Register-B (C = 1)

5

2

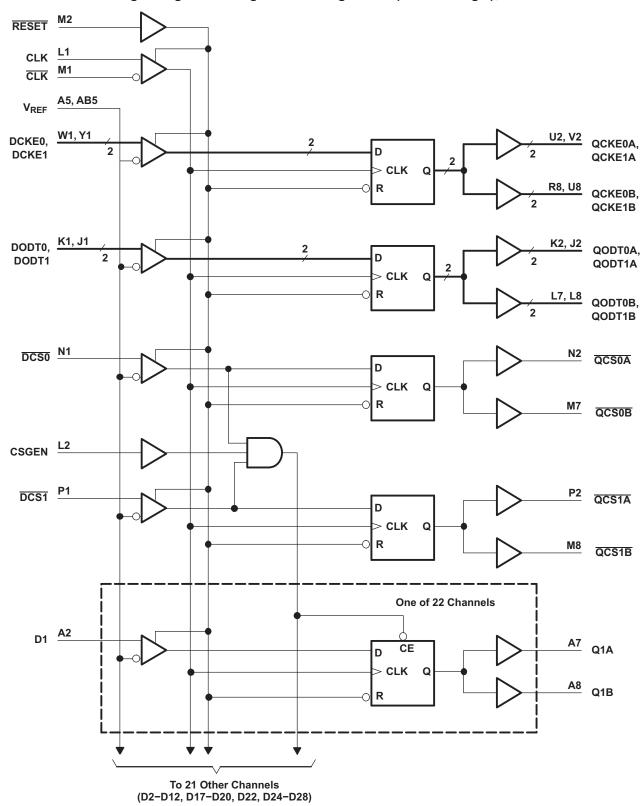
1

A B C C C C C C C C C C C C C C C C C C		1	2	3	4	5	6	7	8
G 000000000000000000000000000000000000	Α	(0	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	0
E 000000000000000000000000000000000000	В	()	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	()	\bigcirc
E 000000000000000000000000000000000000	С								
F 000000000000000000000000000000000000	D	()					\bigcirc	\bigcirc	\bigcirc
G 000000000000000000000000000000000000	Е						_	_	
H 000000000000000000000000000000000000	F								
	G			_					
K 000000000000000000000000000000000000									
L 000000000000000000000000000000000000									
M 000000000000000000000000000000000000									
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		•	-	•	•	-	•
D2	D1	С	GND	V _{REF}	GND	Q1A	Q1B
D4	D3	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q2A	Q2B
D6	D5	GND	GND	GND	GND	Q3A	Q3B
D8	D7	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q4A	Q4B
D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
D10	Q8A	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q7A	Q6B
D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
D12	Q12A	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q11A	Q8B
D13 (DODT1)	Q13A (DODT1A)	GND	GND	GND	GND	Q10B	Q9B
D14 (DODT0)	Q14A (QODT0A)	v _{cc}	v_{cc}	v _{cc}	v _{cc}	Q12B	Q11B
CLK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
CLK	RESET	QERR	v _{cc}	v _{cc}	v _{cc}	Q15B (QCS0B)	Q16B (QCS1B)
D15 (DCS0)	Q15A (QCS0A)	GND	GND	GND	GND	Q17B	Q18B
D16 (DCS1)	Q16A (QCS1A)	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q19B	Q20B
D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
D18	Q19A	v _{cc}	v_{cc}	v _{cc}	v _{cc}	Q20A	Q22B
D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
D20	Q23A (QCKE1A)	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q24A	Q24B
D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
D23 (DCKE1)	D24	v _{cc}	v _{cc}	v _{cc}	v _{cc}	Q26A	Q26B
D25	D26	GND	GND	GND	GND	Q27A	Q27B
D27	D28	NC	v _{cc}	V _{REF}	v _{cc}	Q28A	Q28B
	D4 D6 D8 D9 D10 D11 D12 D13 (DODT1) D14 (DODT0) CLK CLK D15 (DCS0) D16 (DCS1) D17 D18 D19 D20 D21 (DCKE0) D23 (DCKE1) D25	D4 D3 D6 D5 D8 D7 D9 Q6A D10 Q8A D11 Q10A D12 Q12A D13 Q00DT1A D0DT1) Q14A Q0DT0A) Q15A CLK RESET D15 Q15A QCS0A) Q16A QCS1A) Q17A D17 Q17A D18 Q19A D19 Q21A QCKE0A) Q23A QCKE1A) D22 D23 DCKE1) D22 D23 DCKE1) D24 D25 D26	D4 D3 V _{CC} D6 D5 GND D8 D7 V _{CC} D9 Q6A GND D10 Q8A V _{CC} D11 Q10A GND D12 Q12A V _{CC} D13 Q13A GND D14 Q14A QODTOA) V _{CC} CLK CSGEN PAR_IN CLK RESET QERR D15 Q15A GND QCS0A) GND D16 Q16A V _{CC} D17 Q17A GND D18 Q19A V _{CC} D19 Q21A GND D20 Q23A V _{CC} D21 QCKE1A) V _{CC} D22 GND D23 D24 V _{CC} D25 D26 GND	D4 D3 V _{CC} V _{CC} D6 D5 GND GND D8 D7 V _{CC} V _{CC} D9 Q6A GND GND D10 Q8A V _{CC} V _{CC} D11 Q10A GND GND D12 Q12A V _{CC} V _{CC} D13 (DODT1) GND GND GDT1) (QODT0A) V _{CC} V _{CC} CLK CSGEN PAR_IN GND GND GND GND GND D15 Q15A QERR V _{CC} D15 Q15A QCS V _{CC} D16 QCS0A) GND GND D17 Q17A GND GND D18 Q19A V _{CC} V _{CC} D19 QCXEOA GND GND D20 QCXEOA GND GND D21 QCXEOA QCX V _{CC} QCX	D4 D3 V _{CC} V _{CC} V _{CC} D6 D5 GND GND GND D8 D7 V _{CC} V _{CC} V _{CC} D9 Q6A GND GND GND D10 Q8A V _{CC} V _{CC} V _{CC} D11 Q10A GND GND GND D12 Q12A V _{CC} V _{CC} V _{CC} D13 Q13A GND GND GND GD13 Q13A GND GND GND D14 Q14A QCO V _{CC} V _{CC} CLK CSGEN PAR_IN GND GND GLK RESET QERR V _{CC} V _{CC} VCC V _{CC} V _{CC} V _{CC} D15 Q15A QCSAA QCC V _{CC} V _{CC} D17 Q17A GND GND GND D18 Q19A V _{CC} V _{CC} V _{CC}	D4 D3 V _{CC} V _{CC} V _{CC} V _{CC} D6 D5 GND GND GND GND D8 D7 V _{CC} V _{CC} V _{CC} V _{CC} V _{CC} D9 Q6A GND GND GND GND GND D10 Q8A V _{CC} V _{CC} V _{CC} V _{CC} V _{CC} D11 Q10A GND GND GND GND GND D12 Q12A V _{CC} V _{CC} V _{CC} V _{CC} V _{CC} D13 (DODT1) GND GND GND GND GND D14 (DODT1) Q15A GND GND GND GND CLK CSGEN PAR_IN GND GND GND GND CLK RESET QERR V _{CC} V _{CC} V _{CC} V _{CC} D15 Q15A QCS0A GND GND GND GND D16	D4 D3 V _{CC} V _{CC} V _{CC} V _{CC} Q2A D6 D5 GND GND GND GND Q3A D8 D7 V _{CC} V _{CC} V _{CC} V _{CC} Q4A D9 Q6A GND GND GND GND Q5A D10 Q8A V _{CC} V _{CC} V _{CC} V _{CC} Q7A D11 Q10A GND GND GND GND Q9A D12 Q12A V _{CC} V _{CC} V _{CC} V _{CC} Q11A D13 Q13A GND GND GND GND Q10B D14 Q12A V _{CC} V _{CC} V _{CC} V _{CC} Q10B CLK CSGEN PAR_IN GND GND GND GND Q14B Q15A Q15A QRR V _{CC} V _{CC} V _{CC} V _{CC} Q17B D15 Q15A QRR GND GND

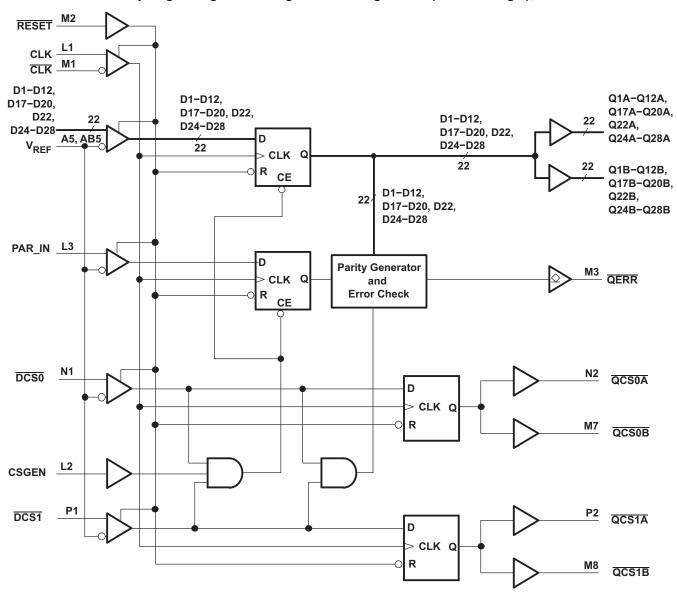


Logic Diagram for Register-B Configuration (Positive Logic); C = 1



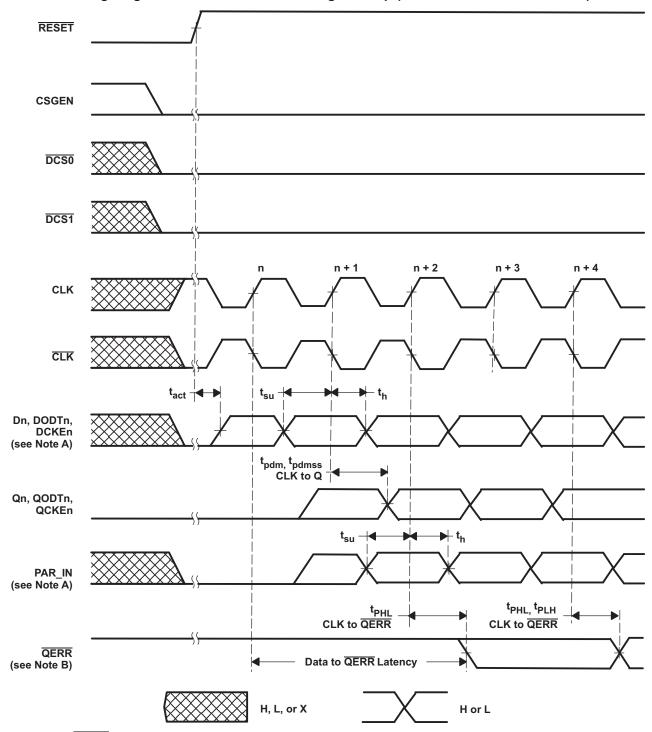


Parity Logic Diagram for Register-B Configuration (Positive Logic); C = 1



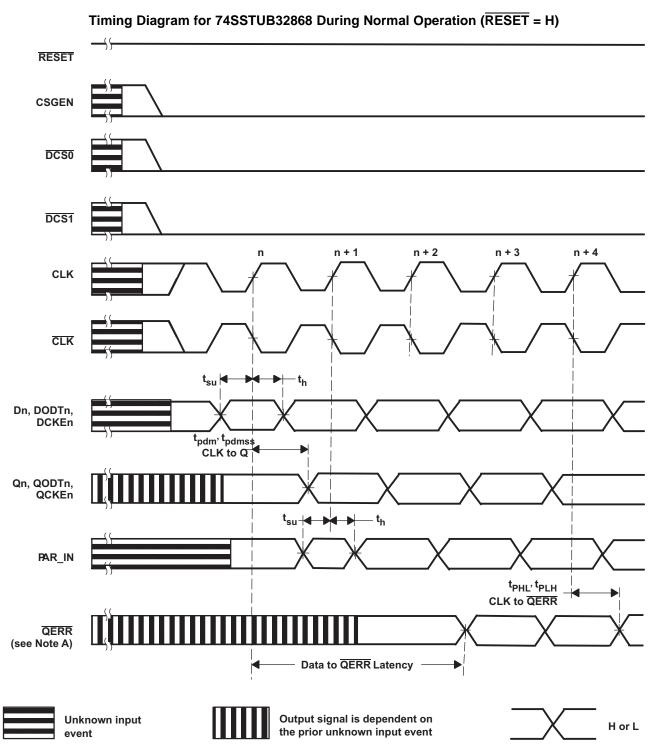


Timing Diagram for 74SSTUB32868 During Start-Up (RESET Switches From L to H)



- A. After RESET is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid a false error.
- B. If the data is clocked in on the n-clock pulse, the $\overline{\text{QERR}}$ output signal is generated on the n + 2 clock pulse, and it is valid on the n + 3 clock pulse.





A. If the data is clocked in on the n-clock pulse, the QERR output signal is generated on the n + 2 clock pulse, and it is valid on the n + 3 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.



Timing Diagram for 74SSTUB32868 During Shut-Down (RESET Switches From H to L) RESET t_{inact} **CSGEN** (see Note A) DCS0 (see Note A) DCS1 (see Note A) CLK (see Note A) CLK (see Note A) Dn, DODTn, **DCKEn** (see Note A) t_{RPHL} RESET to Q Qn, QODTn, **QCKEn** PAR_IN (see Note A) **QERR** ^tRPHL RESET to QERR

A. After RESET is switched from high to low, all data and clock input signals must be held at logic levels (not floating) for a minimum time of t_{inact} max, to avoid a false error.

H, L, or X



TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V _{CC}	Power supply voltage	1.8 V nominal
V _{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
CLK	Negative master clock input	Differential input
С	Configuration control input - Register A or Register B	LVCMOS input
RESET	Asynchronous reset input – resets registers and disables V _{REF} , data and clock differential-input receivers. When RESET is low, all the Q outputs are forced low and the QERR output is forced high.	LVCMOS input
CSGEN	Chip select gate enable – When high, D1–D28 ⁽¹⁾ inputs are latched only when at least one chip select input is low during the rising edge of the clock. When low, the D1–D28 ⁽¹⁾ inputs are latched and redriven on every rising edge of the clock.	LVCMOS input
D1-D28	Data input - clocked in on the crossing of the rising edge of CLK and the falling edge of CLK	SSTL_18 input
DCS0, DCS1	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to redrive all D inputs (CSGEN high) only when at least one chip select input is low. If CSGEN, DCSO, and DCS1 inputs are high, D1–D28 ⁽²⁾ inputs will be disabled.	SSTL_18 input
DODT0, DODT1	The outputs of this register bit will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	SSTL_18 input
DCKE0, DEKE1	The outputs of this register bit will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	SSTL_18 input
PAR_IN	Parity input – arrives one clock cycle after the corresponding data input. Pulldown resistor of typical $150k\Omega$ to GND.	SSTL_18 input with pulldown
Q1-Q28 ⁽³⁾	Data outputs that are suspended by the DCS0 and DCS1 control.	1.8 V CMOS output
QCS0, QCS1	Data output that will not be suspended by the DCS0 and DCS1 control.	1.8 V CMOS output
QODT0, QODT1	Data output that will not be suspended by the DCS0 and DCS1 control.	1.8 V CMOS output
QCKE0, QEKE1	Data output that will not be suspended by the DCS0 and DCS1 control.	1.8 V CMOS output
QERR	Output error bit – generated two clock cycles after the corresponding data is registered.	Open-drain output
NC	No internal connection	

⁽¹⁾ Data inputs = D1-D5, D7, D9-D12, D17-D28 when C = 0. Data inputs = D1-D12, D17-D20, D22, D24-D28 when C = 1. Data inputs = D1-D5, D7, D9-D12, D17-D28 when C = 0.

Data inputs = D1-D12, D17-D20, D22, D24-D28 when C = 1.

Data outputs = Q1-Q5, Q7, Q9-Q12, Q17-Q28 when C = 0. Data outputs = Q1-Q12, Q17-Q20, Q22, Q24-Q28 when C = 1.



FUNCTION TABLE

			INPUTS					OUT	PUTS	
RESET	DCS0	DCS1	CSGEN	CLK	CLK	dn, DODTn, DCKEn	Qn	QCS0	QCS1	QODT, QCKE
Н	L	L	Х	↑	↓	L	L	L	L	L
Н	L	L	Χ	↑	\downarrow	Н	Н	L	L	Н
Н	L	L	Χ	L or H	L or H	Χ	Q_0	Q_0	Q_0	Q_0
Н	L	Н	Χ	↑	\downarrow	L	L	L	Н	L
Н	L	Н	Χ	↑	\downarrow	Н	Н	L	Н	Н
Н	L	Н	Χ	L or H	L or H	Χ	Q_0	Q_0	Q_0	Q_0
Н	Н	L	Χ	↑	\downarrow	L	L	Н	L	L
Н	Н	L	Χ	↑	\downarrow	Н	Н	Н	L	Н
Н	Н	L	Χ	L or H	L or H	Χ	Q_0	Q_0	Q_0	Q_0
Н	Н	Н	L	↑	\downarrow	L	L	Н	Н	L
Н	Н	Н	L	↑	\downarrow	Н	Н	Н	Н	Н
Н	Н	Н	L	L or H	L or H	Χ	Q_0	Q_0	Q_0	Q_0
Н	Н	Н	Н	↑	\downarrow	L	Q_0	Н	Н	L
Н	Н	Н	Н	↑	\downarrow	Н	Q_0	Н	Н	Н
Н	Н	Н	Н	L or H	L or H	Χ	Q_0	Q_0	Q_0	Q_0
L	X or floating	L	L	L	L	L				

PARITY AND STANDBY FUNCTION

			INPUTS				OUTPUTS
RESET	CLK	CLK	DCS0	DCS1	Σ OF INPUTS = H D1 - D22	PAR_IN ⁽¹⁾	QERR (2)
Н	↑	\downarrow	L	Х	Even	L	Н
Н	↑		L	X	Odd	L	L
Н	↑	\downarrow	L	X	Even	Н	L
Н	↑	\downarrow	L	X	Odd	Н	Н
Н	↑	\downarrow	X	L	Even	L	Н
Н	↑	\downarrow	X	L	Odd	L	L
Н	↑	\downarrow	X	L	Even	Н	L
Н	↑	\downarrow	X	L	Odd	Н	Н
Н	↑	\downarrow	Н	Н	X	X	QERR ₀ (3)
Н	L or H	L or H	X	X	X	X	QERR 0
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	Н

(3) If DCSO, DCS1 and CSGEN are driven high, the device is placed in a low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the QERR output is driven low, it stays latched low for the LPM duration plus two clock cycles or until RESET is driven low.

 ⁽¹⁾ PAR_IN arrives one clock cycle after the data to which it applies.
 (2) This transition assumes that QERR is high at the crossing of CLK going high and CLK going low. If QERR goes low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity error duration or until RESET is driven low. For QERR computation, CSGEN is a "don't care".



TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature (see Figure 1 and Note (1))

			V _{CC} = 1.8 V :	<u>+</u> 0.1 V	
			MIN	MAX	UNIT
f _(clock)	Clock frequency			410	MHz
t _w	Pulse duration, CL	Pulse duration, CLK, CLK high or low Differential inputs active time (see Note ⁽²⁾)			ns
t _{act}	Differential inputs a	active time (see Note (2))		10	ns
t _{inact}	Differential inputs in	nactive time (see Note (3))		15	ns
	<u>, </u>	DCSn before CLK↑, CLK↓, CSGEN high	600		
	Catua tima	DCSn before CLK↑, CLK↓, CSGEN low	500		
t _{su}	Setup time	DODTn, DCKEn, and Data before CLK↑, CLK↓	500		ps
		PAR_IN before CLK↑, CLK↓	500		
	Hald time a	DCSn, DODTn, DCKEn, and Data after CLK↑, CLK↓			20
ι _h	Hold time	PAR_IN after CLK↑, CLK↓	400		ps

All inputs slew rate is 1 V/ns ±20%

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage, load, and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 1.8 \text{ V} \pm$		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f _{max} (see Figure 2)			410		MHz
t _{pdm} ⁽¹⁾ (production test, see Figure 1)	CLK and CLK	Q	0.5	1.0	ns
t _{PLH} (see Figure 4)	CLK and CLK	QERR	1.2	3	ns
t _{PHL} (see Figure 4)	CLK and CLK	QERK	1	2.4	
t _{RPHL} (2) (see Figure 2)	RESET	Q		3	ns
t _{RPLH} (see Figure 4)	RESET	QERR		3	ns

The typical difference between min and max does not exceed 400 ps.

OUTPUT SLEW RATES

over operating free-air temperature range (unless otherwise noted) (see Figure 3)

			V _{CC} = 1.8 V ±0.1 V		
PARAMETER	FROM	TO (OUTPUT)	MIN	MAX	UNIT
dV/dt_r	20%	80%	1	5	V/ns
dV/dt_f	80%	20%	1	5	V/ns
$dV/dt_\Delta^{(1)}$	20% to 80%	20% to 80%		1	V/ns

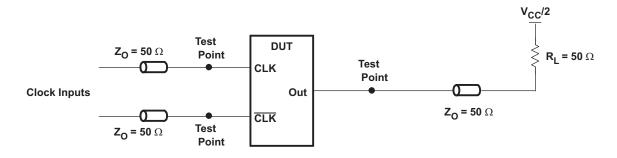
(1) The difference between dV/dr_r (rising edge rate) and dV/dt_f (falling edge).

 V_{REF} must be held at a valid input level and data inputs must be held low for a minimum time of t_{act} max, after \overline{RESET} is taken high. V_{REF} , data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after \overline{RESET} is taken low.

Includes 350-ps test-load transmission line delay.



PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

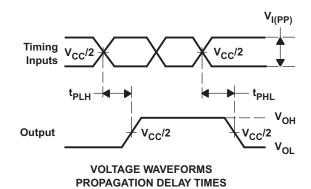


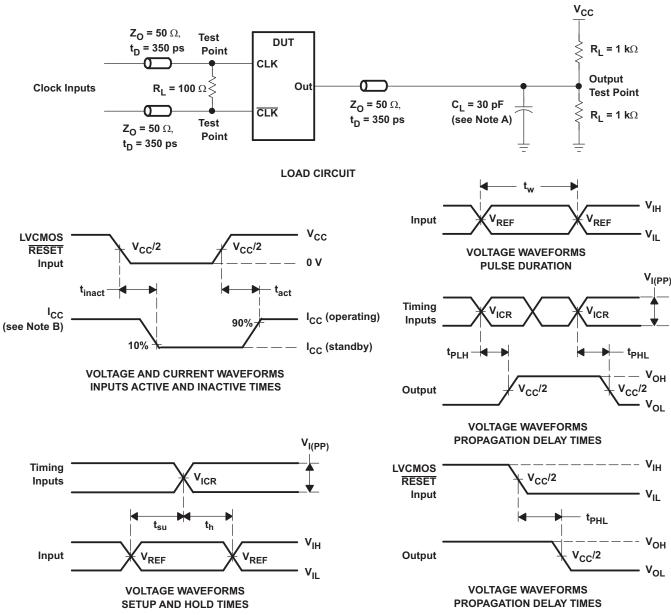
Figure 1. Output Load Circuit for Production Test

Propagation Delay (Design Goal as per JEDEC Specification)

			V _{CC} = 1.8 V ±0		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pdm} ⁽¹⁾	CLK and CLK	Q	1.1	1.5	ns
t _{pdmss} ⁽¹⁾	CLK and CLK	Q		1.6	ns

(1) Includes 350-ps test-load transmission line delay.

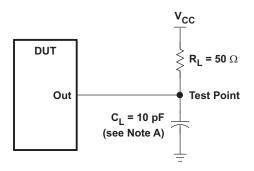




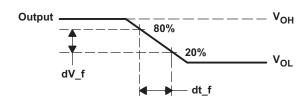
- A. C_L includes probe and jig capacitance.
- B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_{O} = 0$ mA.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, input slew rate = 1 V/ns \pm 20% (unless otherwise noted).
- D. The outputs are measured one at a time with one transition per measurement.
- E. $V_{REF} = V_{CC}/2$
- F. $V_{IH} = V_{REF} + 250$ mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
- G. $V_{IL} = V_{REF}$ 250 mV (ac voltage levels) for differential inputs. $V_{IL} = GND$ for LVCMOS input.
- H. $V_{I(PP)} = 600 \text{ mV}.$
- I. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Data Output Load Circuit and Voltage Waveforms

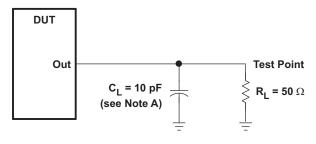




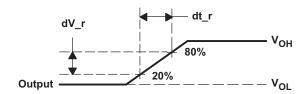
LOAD CIRCUIT
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT





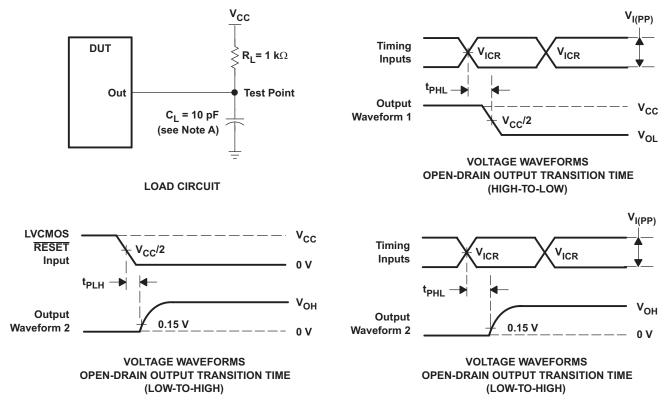


VOLTAGE WAVEFORMS LOW-TO-HIGH SLEW-RATE MEASUREMENT

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \le 10 \text{ MHz}, Z_O = 50 \Omega$, input slew rate = 1 V/ns ±20% (unless otherwise specified).

Figure 3. Data Output Slew-Rate Measurement Information





- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \le 10 \text{ MHz}$, $Z_0 = 50 \Omega$, input slew rate = 1 V/ns ±20% (unless otherwise specified).
- C. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Error Output Load Circuit and Voltage Waveforms



PACKAGE OPTION ADDENDUM

24-.lan-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	U		Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
74SSTUB32868ZRHR	ACTIVE	NFBGA	ZRH	176	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	SB868	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74SSTUB32868ZRHR	NFBGA	ZRH	176	1000	330.0	24.4	6.3	15.3	1.65	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

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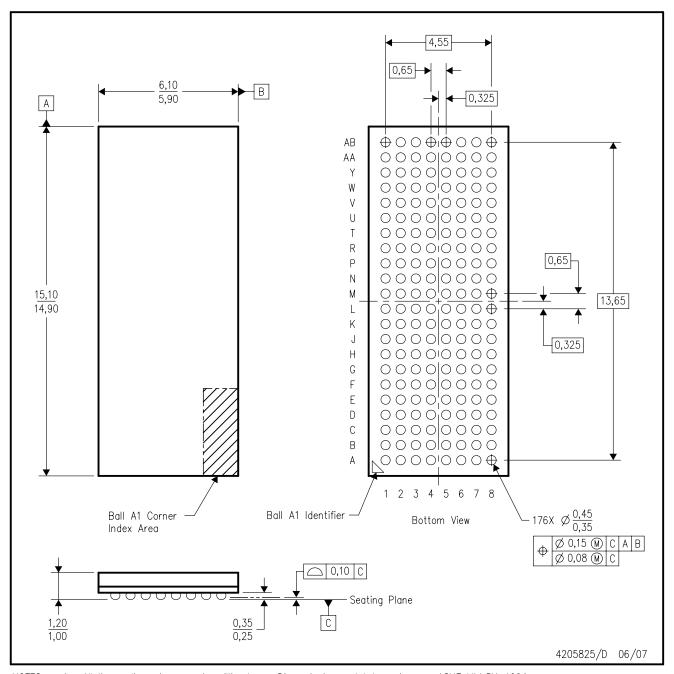


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74SSTUB32868ZRHR	NFBGA	ZRH	176	1000	336.6	336.6	31.8

ZRH (R-PBGA-N176)

PLASTIC BALL GRID ARRAY



NOTES: A. All

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Complies to JEDEC MO-246 variation B.
- D. This package is lead-free. Refer to the 176 GRH package (drawing 4205824) for tin-lead (SnPb).



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