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RAD-TOLERANT CLASS V OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 7.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial Power-Down-Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Rad Tolerant: 50kRad (Si) TID (1)
 - TID Dose Rate 0.10 rad/s
- QML-V Qualified, SMD 5962-97626
- Radiation tolerance is a typical value based upon initial device qualification. Radiation Lot Acceptance Testing is available – contact factory for details.

W PACKAGE (TOP VIEW) CLKAB ∏ 24 V_{CC} SAB [23 CLKBA DIR [SBA 3 22∏ 21 OE A1 A2 [20 B1 5 АЗ П 6 19∏ B2 18**∏** B3 A4 [] 17 B4 A5 🛮 8 A6 9 16∏ B5 Α7 15∏ B6 10 14 B7 А8 П 11 B8 GND II 12 13**|**|

DESCRIPTION/ORDERING INFORMATION

The SN54LVC646A octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

This device consists of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 shows the four fundamental bus-management functions that are performed with the SN54LVC646A device.

ORDERING INFORMATION

	T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-5	55°C to 125°C	CFP – W	Tube of 85	5962-9762601VKA	5962-9762601VKA	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Output-enable (\overline{OE}) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.

The select-control (SAB and SBA) inputs <u>can</u> multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

		INP	UTS			DAT	A I/O	OPERATION OR	
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	FUNCTION	
Х	Х	1	Х	Х	Х	Input	Unspecified ⁽¹⁾	Store A, B unspecified ⁽¹⁾	
Х	X	Χ	↑	X	X	Unspecified ⁽¹⁾	Input	Store B, A unspecified ⁽¹⁾	
Н	Х	1	↑	Х	Х	Input	Input	Store and B data	
Н	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage	
L	L	Χ	Χ	Χ	L	Output	Input	Real-time B data to A bus	
L	L	Χ	H or L	X	Н	Output	Input	Stored B data to A bus	
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus	
L	Н	H or L	Χ	Н	Х	Input	Output	Stored A data to B bus	

⁽¹⁾ The data-output functions can be enabled or disabled by various signals at $\overline{\text{OE}}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

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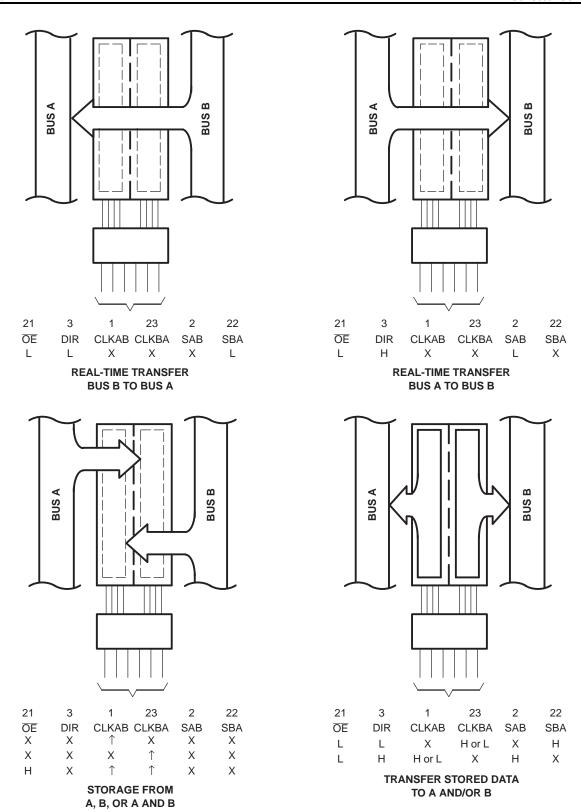
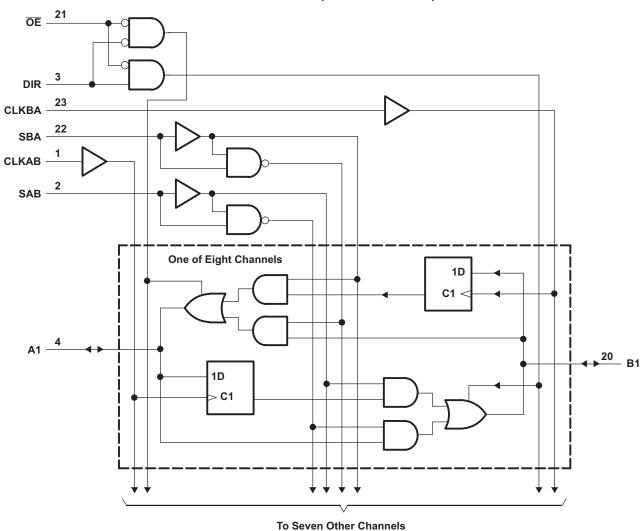


Figure 1. Bus-Management Functions

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LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V _{CC}	Supply voltage range			-0.5	6.5	V
VI	Input voltage range ⁽²⁾			-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance	ce or power-off state ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2)(3)				V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0			-50	mA
I _{OK}	Output clamp current	V _O < 0			-50	mA
Io	Continuous output current				±50	mA
	Continuous current through V _{CC} or GND				±100	mA
T _{stg}	Storage temperature range				150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.



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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
\/	Cupply voltage	Operating	2	3.6	V
V_{CC}	Supply voltage	Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
VI	Input voltage		0	5.5	V
V-	Output voltage	High or low state	0	V _{CC}	V
Vo	Output voltage	3-state	0	5.5	v
	High lovel output ourrent	V _{CC} = 2.7 V		-12	A
I _{OH}	High-level output current	V _{CC} = 3 V		-24	mA
	Low lovel output ourrent	V _{CC} = 2.7 V		12	A
I _{OL}	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-55	125	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT			
		100 4		1.65 V to 3.6 V							
		$I_{OH} = -100 \mu A$		2.7 V to 3.6 V	V _{CC} - 0.2						
		$I_{OH} = -4 \text{ mA}$		1.65 V							
V_{OH}		$I_{OH} = -8 \text{ mA}$		2.3 V				V			
		1 12 mA		2.7 V	2.2						
		$I_{OH} = -12 \text{ mA}$		3 V	2.4						
		$I_{OH} = -24 \text{ mA}$		3 V	2.2						
		1. 100 4		1.65 V to 3.6 V							
V		I _{OL} = 100 μA		2.7 V to 3.6 V			0.2				
		I _{OL} = 4 mA		1.65 V				V			
V _{OL}		I _{OL} = 8 mA		2.3 V				V			
		I _{OL} = 12 mA		2.7 V			0.4				
		I _{OL} = 24 mA		3 V			0.55				
I	Control inputs	V _I = 0 to 5.5 V		3.6 V			±5	μΑ			
I _{off}		V_I or $V_O = 5.5 \text{ V}$		0				μΑ			
I _{OZ} ⁽²⁾		V _O = 0 to 5.5 V		3.6 V			±15	μΑ			
		V _I = V _{CC} or GND	0	2.6.1/			10	^			
I _{CC}		$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(3)}$	= 0	3.6 V			10	μΑ			
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μΑ			
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V		4.5		pF			
C _{io}	A or B port	$V_O = V_{CC}$ or GND		3.3 V		7.5		pF			

All typical values are at V $_{CC}$ = 3.3 V, T $_{A}$ = 25°C. For I/O ports, the parameter I $_{OZ}$ includes the input leakage current. This applies in the disabled state only.



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Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		V _{CC} = 2	2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT	
		MIN MAX		MIN	MAX		
f _{clock}	Clock frequency		150		150	MHz	
t _w	Pulse duration	3.3		3.3		ns	
t _{su}	Setup time, data before CLK↑	1.6		1.5		ns	
t _h	Hold time, data after CLK↑	1.7		1.7		ns	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
	A or B	B or A		7.9	1	7.4	
t _{pd}	CLK	A or B		8.8	1	8.4	ns
	SBA or SAB	AOIB		9.9	1	8.6	
t _{en}	ŌĒ	A		10.2	1	8.2	ns
t _{dis}	ŌĒ	A		8.9	1	7.5	ns
t _{en}	DIR	В		10.4	1	8.3	ns
t _{dis}	DIR	В		8.7	1	7.9	ns

Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V_{CC} = 2.5 V	$V_{CC} = 3.3 \text{ V}$	UNIT
			TYP	TYP	TYP		
Cnd	Power dissipation capacitance	Outputs enabled	f = 10 MHz	(1)	(1)	75	pF
Cpd	per transceiver	Outputs disabled		(1)	(1)	9	

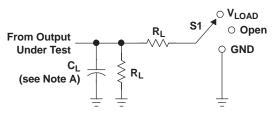
⁽¹⁾ This information was not available at the time of publication.

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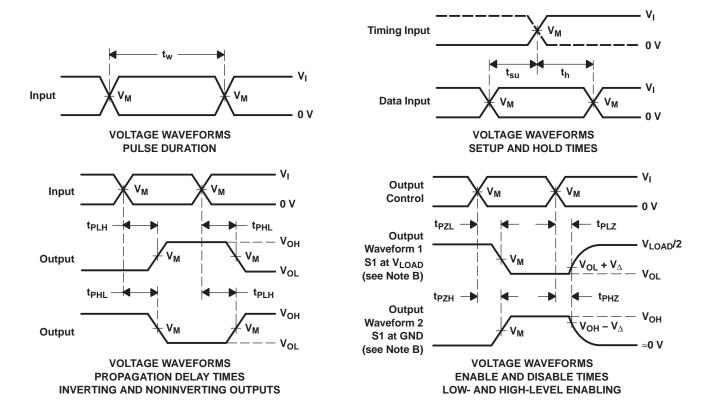
PARAMETER MEASUREMENT INFORMATION



TEST	S1		
t _{PLH} /t _{PHL}	Open		
t _{PLZ} /t _{PZL}	V _{LOAD}		
t _{PHZ} /t _{PZH}	GND		

1	0	ΔΙ	ח	CI	R	CI	Ш	т

V	INPUTS		V	V		Б	V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9762601VKA	ACTIVE	CFP	W	24 1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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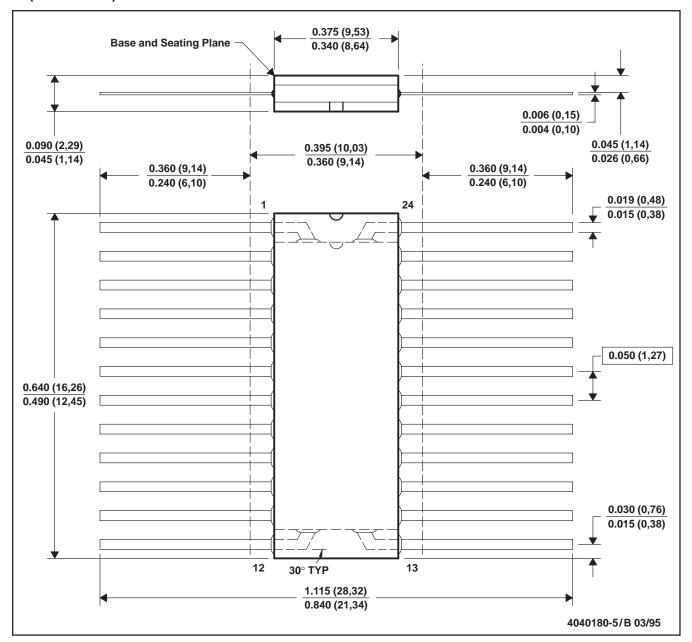
Catalog: SN54LVC646A

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.



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