

## 12 LVPECL Output, High-Performance Clock Buffer

Check for Samples: [CDCLVP2106](#)

### FEATURES

- Dual 1:6 Differential Buffer
- Two Clock Inputs
- Universal Inputs Can Accept LVPECL, LVDS, LVCMOS/LVTTL
- 12 LVPECL Outputs
- Maximum Clock Frequency: 2 GHz
- Maximum Core Current Consumption: 92 mA
- Very Low Additive Jitter: <100 fs,rms in 10-kHz to 20-MHz Offset Range
- 2.375-V to 3.6-V Device Power Supply
- Maximum Propagation Delay: 550 ps
- Maximum Within Bank Output Skew: 20 ps
- LVPECL Reference Voltage,  $V_{AC\_REF}$ , Available for Capacitive-Coupled Inputs
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in 6-mm  $\times$  6-mm QFN-40 (RHA) Package
- ESD Protection Exceeds 2 kV (HBM)

### APPLICATIONS

- Wireless Communications
- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment

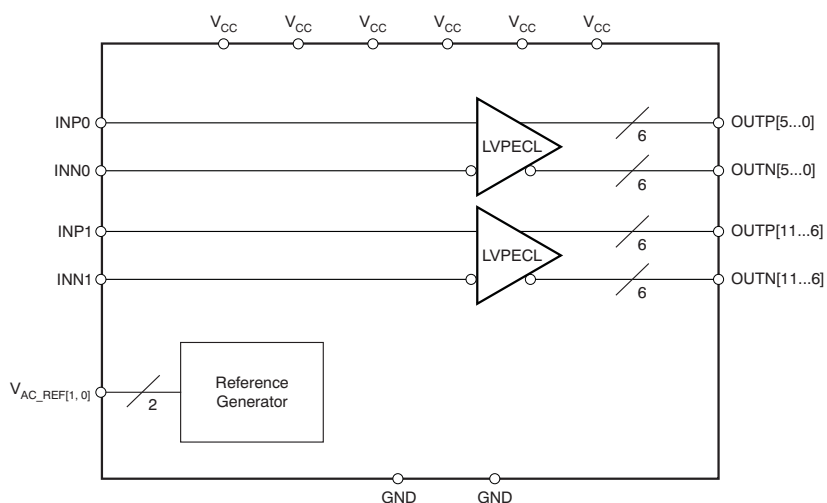
### DESCRIPTION

The CDCLVP2106 is a highly versatile, low additive jitter buffer that can generate 12 copies of LVPECL clock outputs from two LVPECL, LVDS, or LVCMOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2 GHz. Each buffer block consists of one input that feeds two LVPECL outputs. The overall additive jitter performance is less than 0.1 ps, RMS from 10 kHz to 20 MHz, and overall output skew is as low as 20 ps, making the device a perfect choice for use in demanding applications.

The CDCLVP2106 clock buffer distributes two clock inputs (IN0, IN1) to 12 pairs of differential LVPECL clock outputs (OUT0, OUT11) with minimum skew for clock distribution. Each buffer block consists of one input that feeds two LVPECL clock outputs. The inputs can be LVPECL, LVDS, or LVCMOS/LVTTL.

The CDCLVP2106 is specifically designed for driving 50- $\Omega$  transmission lines. When driving the inputs in single-ended mode, the LVPECL bias voltage ( $V_{AC\_REF}$ ) should be applied to the unused negative input pin. However, for high-speed performance up to 2 GHz, differential mode is strongly recommended.

The CDCLVP2106 is characterized for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and is available in a QFN-40, 6-mm  $\times$  6-mm package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**AVAILABLE OPTIONS<sup>(1)</sup>**

T <sub>A</sub>	PACKAGED DEVICES	FEATURES
-40°C to +85°C	CDCLVP2106RHAT	40-pin QFN (RHA) package, small tape and reel
	CDCLVP2106RHAR	40-pin QFN (RHA) package, tape and reel

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS**

Over operating free-air temperature range (unless otherwise noted).<sup>(1)</sup>

		CDCLVP2106	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.5 to 4.6	V
V <sub>IN</sub>	Input voltage range <sup>(3)</sup>	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	Output voltage range <sup>(3)</sup>	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IN</sub>	Input current	20	mA
I <sub>OUT</sub>	Output current	50	mA
T <sub>A</sub>	Specified free-air temperature range (no airflow)	-40 to +85	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+125	°C
ESD	Electrostatic discharge (HBM)	2	kV

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All supply voltages must be supplied simultaneously.
- (3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	CDCLVP2106			UNIT
	MIN	TYP	MAX	
V <sub>CC</sub> Supply voltage	2.375	2.50/3.30	3.60	V
T <sub>A</sub> Ambient temperature	-40		+85	°C

**PACKAGE DISSIPATION RATINGS<sup>(1) (2)</sup>**

PARAMETER	TEST CONDITIONS	VALUE	UNIT
		4 × 4 VIAS ON PAD	
θ <sub>JA</sub> Thermal resistance, junction-to-ambient	0 LFM	36.1	°C/W
	150 LFM	30.2	°C/W
	400 LFM	28.2	°C/W
θ <sub>JP</sub> <sup>(3)</sup> Thermal resistance, junction-to-pad		3.58	°C/W

- (1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
- (2) Connected to GND with 16 thermal vias (0.3-mm diameter).
- (3) θ<sub>JP</sub> (junction-to-pad) is used for the QFN package, because the primary heat flow is from the junction to the GND pad of the QFN package.

**ELECTRICAL CHARACTERISTICS: LVCMOS Input<sup>(1)</sup>**

 At  $V_{CC} = 2.375\text{ V}$  to  $3.6\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	CDCLVP2106			UNIT
		MIN	TYP	MAX	
$f_{IN}$ Input frequency				200	MHz
$V_{th}$ Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.8	V
$V_{IH}$ Input high voltage		$V_{th} + 0.1$		$V_{CC}$	V
$V_{IL}$ Input low voltage		0		$V_{th} - 0.1$	V
$I_{IH}$ Input high current	$V_{CC} = 3.6\text{ V}$ , $V_{IH} = 3.6\text{ V}$			40	$\mu\text{A}$
$I_{IL}$ Input low current	$V_{CC} = 3.6\text{ V}$ , $V_{IL} = 0\text{ V}$			-40	$\mu\text{A}$
$\Delta V/\Delta T$ Input edge rate	20% to 80%	1.5			V/ns
$I_{CAP}$ Input capacitance			5		pF

 (1) [Figure 3](#) and [Figure 4](#) show dc test setup.

**ELECTRICAL CHARACTERISTICS: Differential Input<sup>(1)</sup>**

 At  $V_{CC} = 2.375\text{ V}$  to  $3.6\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	CDCLVP2106			UNIT
		MIN	TYP	MAX	
$f_{IN}$ Input frequency	Clock input			2000	MHz
$V_{IN, DIFF, PP}$ Differential input peak-peak voltage	$f_{IN} \leq 1.5\text{ GHz}$	0.1		1.5	V
	$1.5\text{ GHz} \leq f_{IN} \leq 2\text{ GHz}$	0.2		1.5	V
$V_{ICM}$ Input common-mode level		1.0		$V_{CC} - 0.3$	V
$I_{IH}$ Input high current	$V_{CC} = 3.6\text{ V}$ , $V_{IH} = 3.6\text{ V}$			40	$\mu\text{A}$
$I_{IL}$ Input low current	$V_{CC} = 3.6\text{ V}$ , $V_{IL} = 0\text{ V}$			-40	$\mu\text{A}$
$\Delta V/\Delta T$ Input edge rate	20% to 80%	1.5			V/ns
$I_{CAP}$ Input capacitance			5		pF

 (1) [Figure 5](#) and [Figure 6](#) show dc test setup. [Figure 7](#) shows ac test setup.

**ELECTRICAL CHARACTERISTICS: LVPECL Output<sup>(1)</sup>**At  $V_{CC} = 2.375\text{ V}$  to  $2.625\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCLVP2106			UNIT
			MIN	TYP	MAX	
$V_{OH}$	Output high voltage		$V_{CC} - 1.26$		$V_{CC} - 0.9$	V
$V_{OL}$	Output low voltage		$V_{CC} - 1.7$		$V_{CC} - 1.3$	V
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	$f_{IN} \leq 2\text{ GHz}$	0.5		1.35	V
$V_{AC, REF}$	Input bias voltage <sup>(2)</sup>	$I_{AC, REF} = 2\text{ mA}$	$V_{CC} - 1.6$		$V_{CC} - 1.1$	V
$t_{PD}$	Propagation delay	$V_{IN, DIFF, PP} = 0.1\text{ V}$			550	ps
		$V_{IN, DIFF, PP} = 0.3\text{ V}$			550	ps
$t_{SK, PP}$	Part-to-part skew				150	ps
$t_{SK, O, WB}$	Within bank output skew				20	ps
$t_{SK, O, BB}$	Bank-to-bank output skew	Both inputs have equal skew			25	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, $f_{OUT} = 100\text{ MHz}$	-50		50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = V_{CC}$ , $V_{th} = 1.25\text{ V}$ , 10 kHz to 20 MHz		0.124		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = 0.9\text{ V}$ , $V_{th} = 1.1\text{ V}$ , 10 kHz to 20 MHz		0.178		ps, RMS
		$f_{OUT} = 2\text{ GHz}$ , $V_{IN, DIFF, PP} = 0.2\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz		0.061		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, DIFF, PP} = 0.15\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz		0.119		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, DIFF, PP} = 1\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz		0.104		ps, RMS
$P_{SPUR}$	Coupling on differential OUT6 from OUT5 in the frequency spectrum of $f_{OUT, 8} \pm (f_{OUT, 8}/2)$ with synchronous inputs	$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$		-45.5		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, DIFF, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$		-47.9		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$		-57.8		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, DIFF, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$		-63.4		dBc
$t_R/t_F$	Output rise/fall time	20% to 80%			200	ps
$I_{EE}$	Supply internal current	Outputs unterminated			92	mA
$I_{CC}$	Output and internal supply current	All outputs terminated, 50 $\Omega$ to $V_{CC} - 2$			477	mA

(1) [Figure 8](#) and [Figure 9](#) show dc and ac test setup.(2) Internally generated bias voltage ( $V_{AC, REF}$ ) is for 3.3-V operation only. It is recommended to apply externally generated bias voltage for  $V_{CC} < 3.0\text{ V}$ .

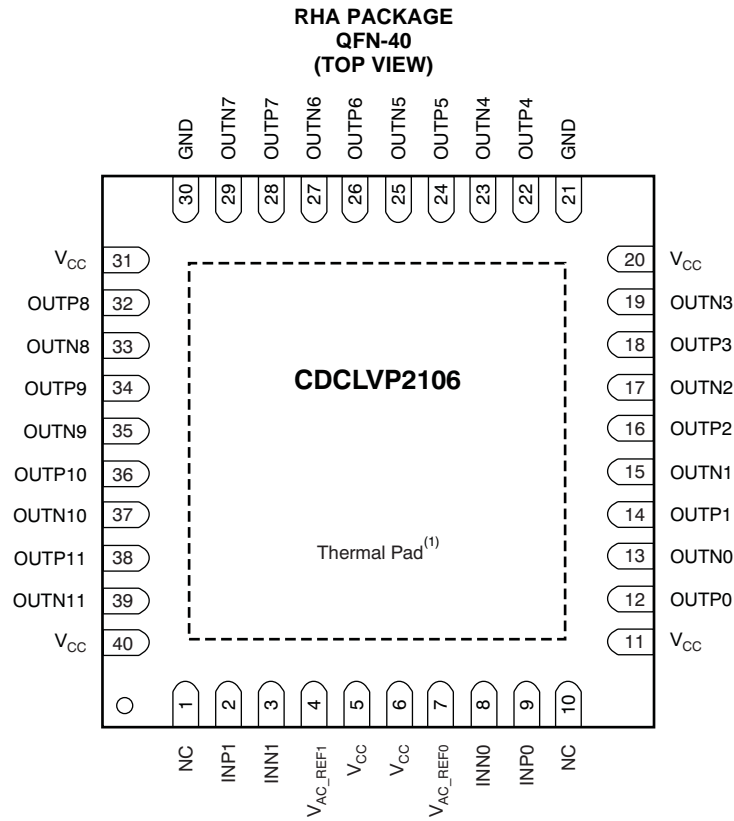
**ELECTRICAL CHARACTERISTICS: LVPECL Output<sup>(1)</sup>**

 At  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$  and  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	CDCLVP2106			UNIT
			MIN	TYP	MAX	
$V_{OH}$	Output high voltage		$V_{CC} - 1.26$		$V_{CC} - 0.9$	V
$V_{OL}$	Output low voltage		$V_{CC} - 1.7$		$V_{CC} - 1.3$	V
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	$f_{IN} \leq 2\text{ GHz}$	0.65		1.35	V
$V_{AC, REF}$	Input bias voltage	$I_{AC, REF} = 2\text{ mA}$	$V_{CC} - 1.6$		$V_{CC} - 1.1$	V
$t_{PD}$	Propagation delay	$V_{IN, DIFF, PP} = 0.1\text{ V}$			550	ps
		$V_{IN, DIFF, PP} = 0.3\text{ V}$			550	ps
$t_{SK, PP}$	Part-to-part skew				150	ps
$t_{SK, O, WB}$	Within bank output skew				20	ps
$t_{SK, O, BB}$	Bank-to-bank output skew	Both inputs have equal skew			25	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, $f_{OUT} = 100\text{ MHz}$	-50		50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = V_{CC}$ , $V_{th} = 1.65\text{ V}$ , 10 kHz to 20 MHz		0.121		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, SE} = 0.9\text{ V}$ , $V_{th} = 1.1\text{ V}$ , 10 kHz to 20 MHz		0.185		ps, RMS
		$f_{OUT} = 2\text{ GHz}$ , $V_{IN, DIFF, PP} = 0.2\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz		0.077		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, DIFF, PP} = 0.15\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz		0.122		ps, RMS
		$f_{OUT} = 100\text{ MHz}$ , $V_{IN, DIFF, PP} = 1\text{ V}$ , $V_{ICM} = 1\text{ V}$ , 10 kHz to 20 MHz		0.105		ps, RMS
$P_{SPUR}$	Coupling on differential OUT6 from OUT5 in the frequency spectrum of $f_{OUT, 8} \pm (f_{OUT, 8}/2)$ with synchronous inputs	$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$		-48.4		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 62.5\text{ MHz}$ , $V_{IN, SIFF, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$		-52.6		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, SE, 1} = V_{CC}$ , $V_{th, 1} = V_{CC}/2$		-65.4		dBc
		$f_{OUT, 8} = 500\text{ MHz}$ , $V_{IN, DIFF, PP, 0} = 0.15\text{ V}$ , $V_{ICM, 0} = 1\text{ V}$ , $f_{OUT, 7} = 15.625\text{ MHz}$ , $V_{IN, DIFF, PP, 1} = 1\text{ V}$ , $V_{ICM, 1} = 1\text{ V}$		-67.1		dBc
$t_R/t_F$	Output rise/fall time	20% to 80%			200	ps
$I_{EE}$	Supply internal current	Outputs unterminated			92	mA
$I_{CC}$	Output and internal supply current	All outputs terminated, 50 $\Omega$ to $V_{CC} - 2$			477	mA

 (1) [Figure 8](#) and [Figure 9](#) show dc and ac test setup.

**PIN CONFIGURATION**



(1) Thermal pad must be soldered to ground.

**PIN DESCRIPTIONS**
**CDCLVP2106 Pin Descriptions**

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
V <sub>CC</sub>	5, 6, 11, 20, 31, 40	Power	2.5-V/3.3-V supplies for the device
GND1, GND2	21, 30	Ground	Device grounds
INP0, INN0	9, 8	Input	Differential input pair or single-ended input no. 0
INP1, INN1	2, 3	Input	Differential input pair or single-ended input no. 1
OUTP11, OUTN11	38, 39	Output	Differential LVPECL output pair no. 11
OUTP10, OUTN10	36, 37	Output	Differential LVPECL output pair no. 10
OUTP9, OUTN9	34, 35	Output	Differential LVPECL output pair no. 9
OUTP8, OUTN8	32, 33	Output	Differential LVPECL output pair no. 8
OUTP7, OUTN7	28, 29	Output	Differential LVPECL output pair no. 7
OUTP6, OUTN6	26, 27	Output	Differential LVPECL output pair no. 6
OUTP5, OUTN5	24, 25	Output	Differential LVPECL output pair no. 5
OUTP4, OUTN4	22, 23	Output	Differential LVPECL output pair no. 4
OUTP3, OUTN3	18, 19	Output	Differential LVPECL output pair no. 3
OUTP2, OUTN2	16, 17	Output	Differential LVPECL output pair no. 2
OUTP1, OUTN1	14, 15	Output	Differential LVPECL output pair no. 1
OUTP0, OUTN0	12, 13	Output	Differential LVPECL output pair no. 0
V <sub>AC_REF0</sub>	7	Output	Bias voltage output for capacitive coupled input pair no. 0. Do not use V <sub>AC_REF</sub> at V <sub>CC</sub> < 3.0 V. If used, it is recommended to use a 0.1-μF capacitor to GND on this pin. The output current is limited to 2 mA.
V <sub>AC_REF1</sub>	4	Output	Bias voltage output for capacitive coupled input pair no. 1. Do not use V <sub>AC_REF</sub> at V <sub>CC</sub> < 3.0 V. If used, it is recommended to use a 0.1-μF capacitor to GND on this pin. The output current is limited to 2 mA.
NC	1, 10	—	Do not connect

**TYPICAL CHARACTERISTICS**

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted).

**DIFFERENTIAL OUTPUT PEAK-TO-PEAK VOLTAGE vs FREQUENCY**

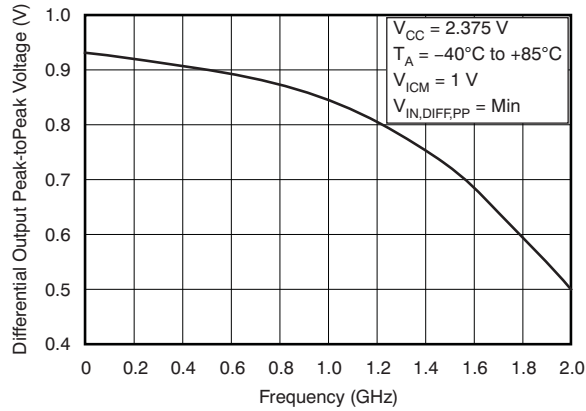


Figure 1.

**DIFFERENTIAL OUTPUT PEAK-TO-PEAK VOLTAGE vs FREQUENCY**

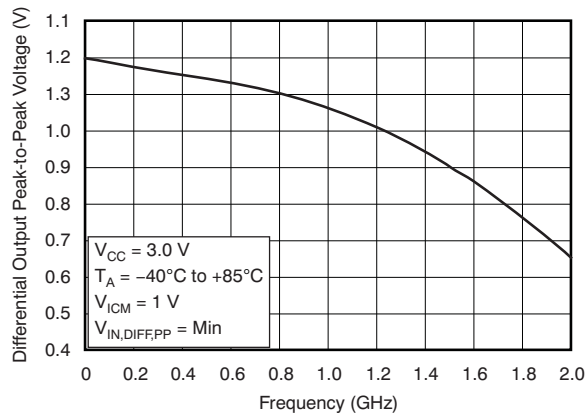


Figure 2.



### TEST CONFIGURATIONS

This section describes the function of each block for the CDCLVP2106. Figure 3 through Figure 9 illustrate how the device should be setup for a variety of test configurations.

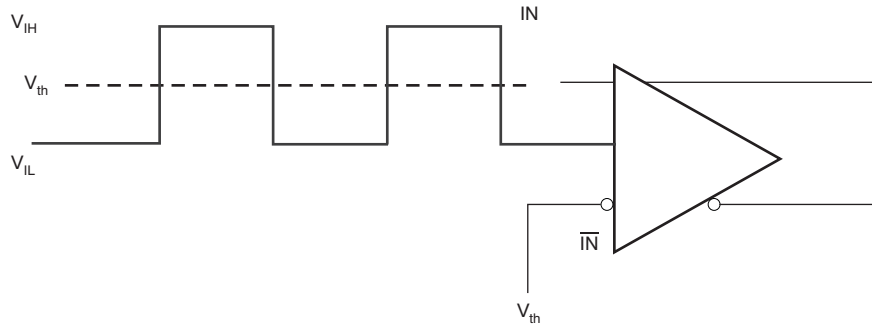


Figure 3. DC-Coupled LVCMOS Input During Device Test

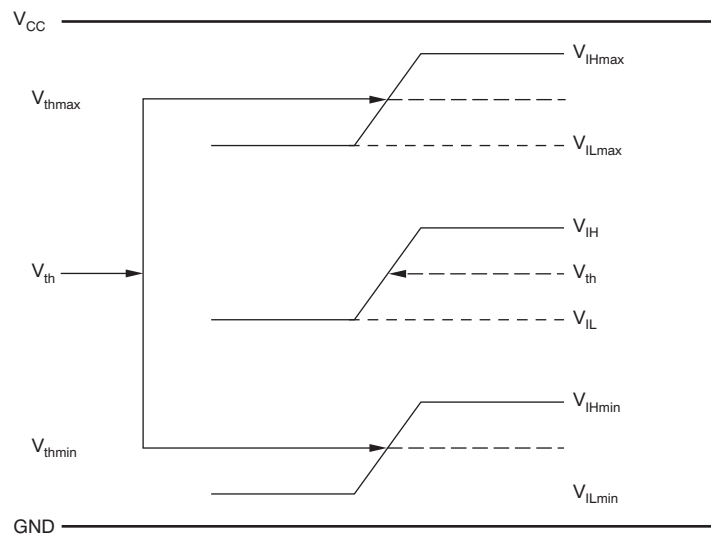


Figure 4.  $V_{th}$  Variation over LVCMOS Levels

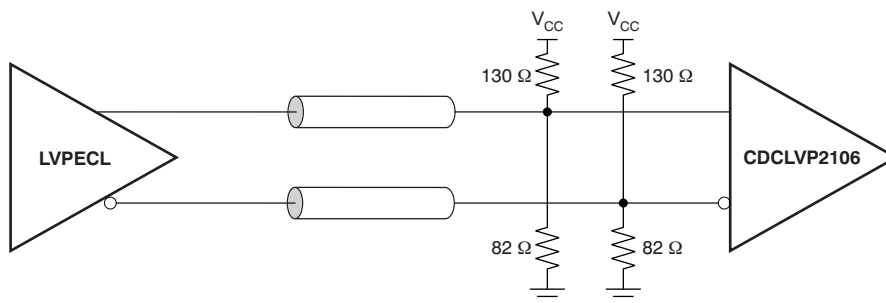


Figure 5. DC-Coupled LVPECL Input During Device Test

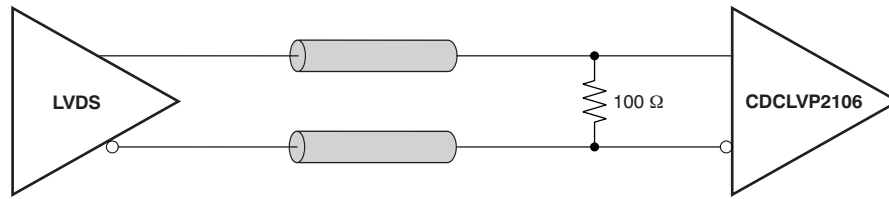


Figure 6. DC-Coupled LVDS Input During Device Test

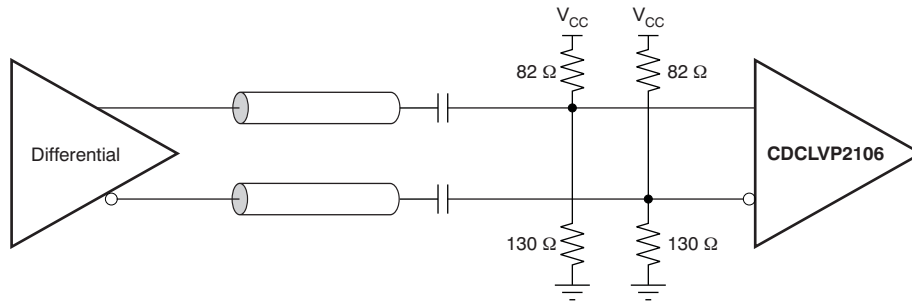


Figure 7. AC-Coupled Differential Input to Device

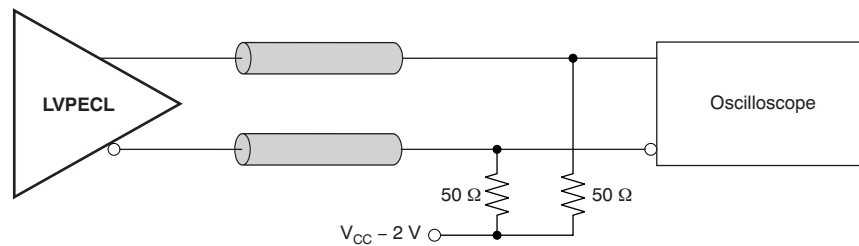


Figure 8. LVPECL Output DC Configuration During Device Test

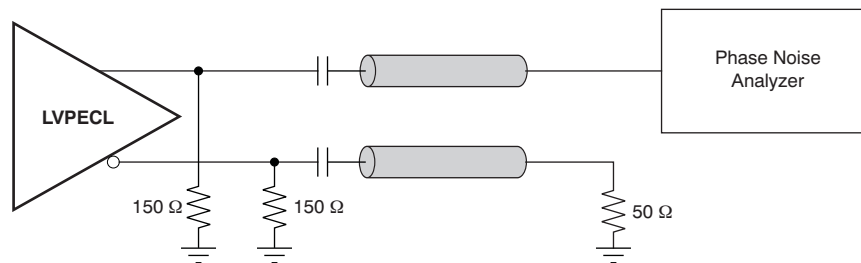


Figure 9. LVPECL Output AC Configuration During Device Test

Figure 10 shows the output voltage and rise/fall time. Output and part-to-part skew are shown in Figure 11.

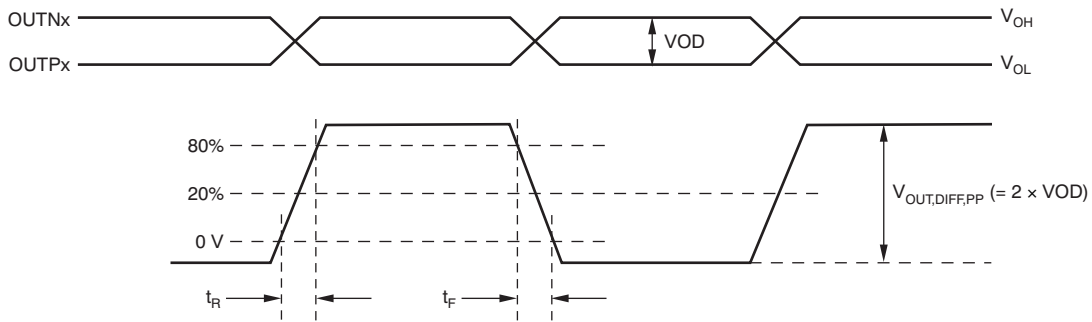
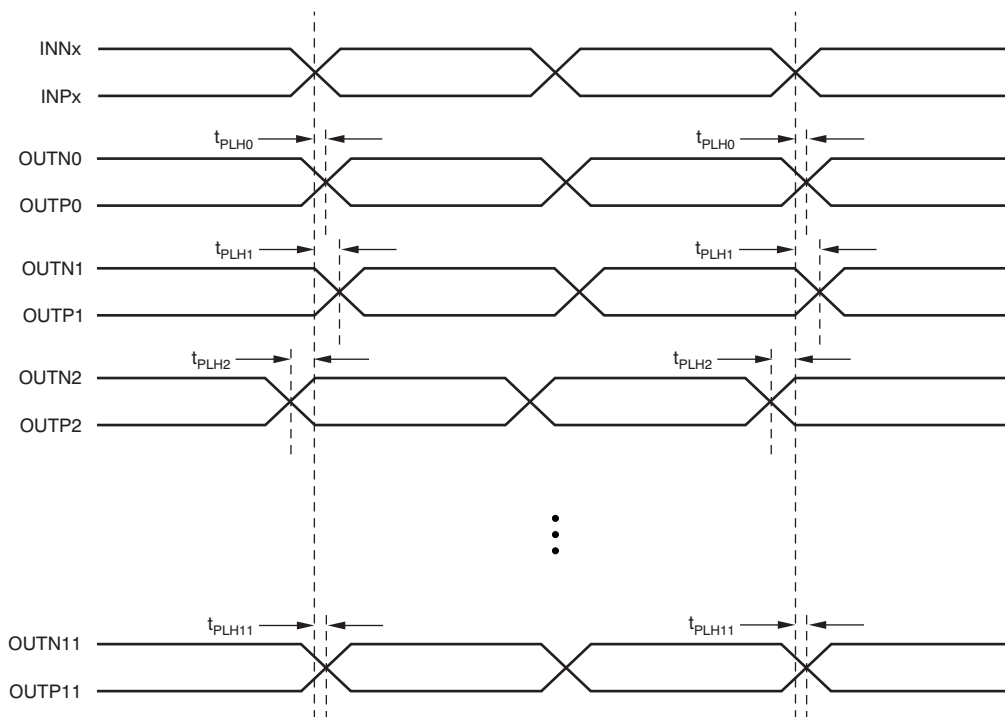


Figure 10. Output Voltage and Rise/Fall Time



- (1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, 2, \dots, 11$ ), or as the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 11$ ).
- (2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, 2, \dots, 11$ ) across multiple devices, or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 11$ ) across multiple devices.

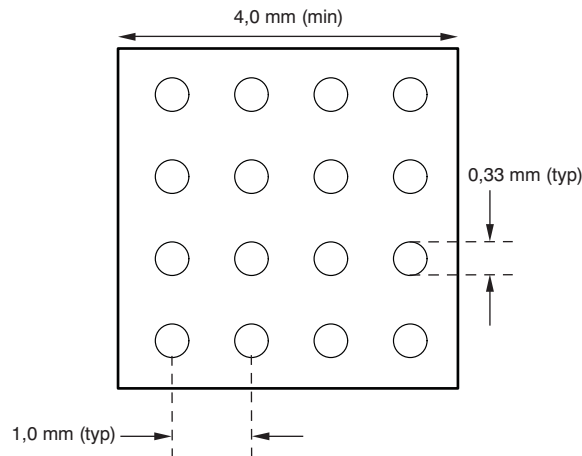
Figure 11. Output and Part-to-Part Skew

## APPLICATION INFORMATION

### Thermal Management

Power consumption of the CDCLVP2106 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +125°C. That is, as an estimate, ambient temperature ( $T_A$ ) plus device power consumption times  $\theta_{JA}$  should not exceed +125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. Figure 12 shows a recommended land and via pattern.



**Figure 12. Recommended PCB Layout**

### Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1- $\mu$ F) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 13 illustrates this recommended power-supply decoupling method.

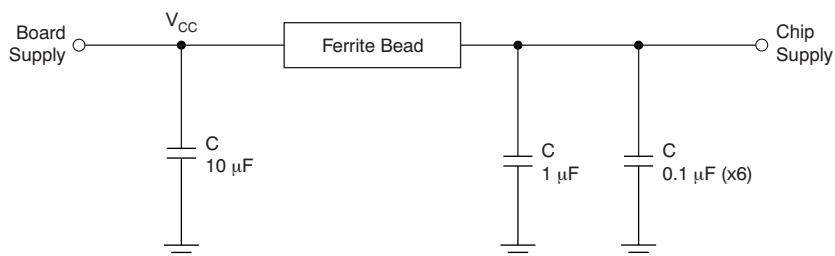
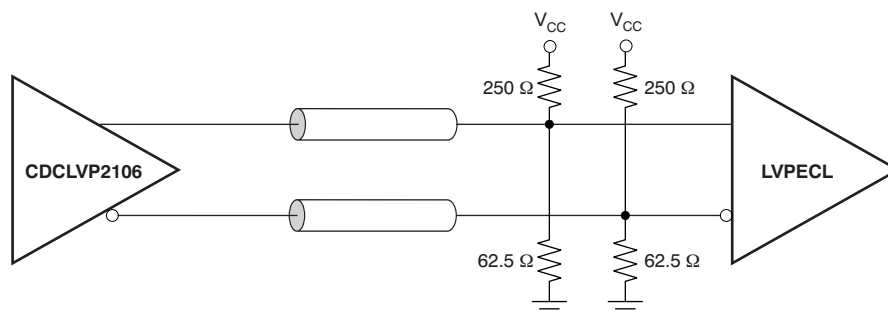


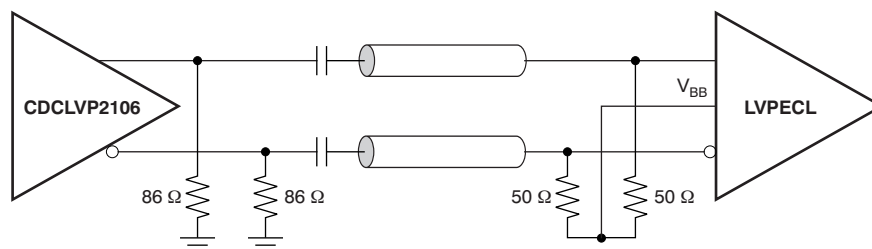
Figure 13. Power-Supply Decoupling

### LVPECL Output Termination

The CDCLVP2106 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is a  $50\ \Omega$  to  $(V_{CC} - 2)$  V, but this dc voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (dc) and ac-coupled configurations. These configurations are shown in Figure 14a and b for  $V_{CC} = 2.5$  V and Figure 15a and b for  $V_{CC} = 3.3$  V, respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, ac coupling is required.

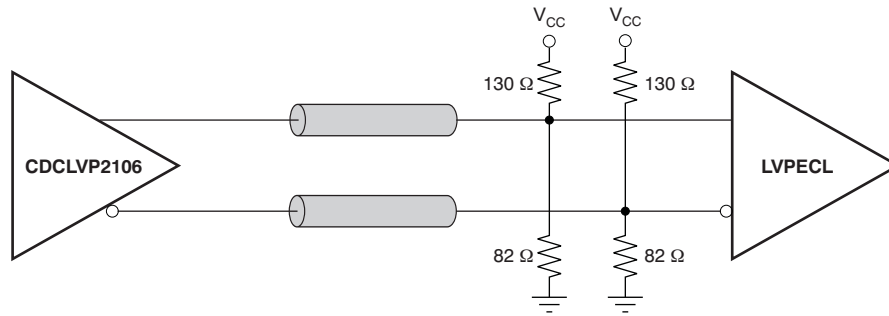


(a) Output DC Termination

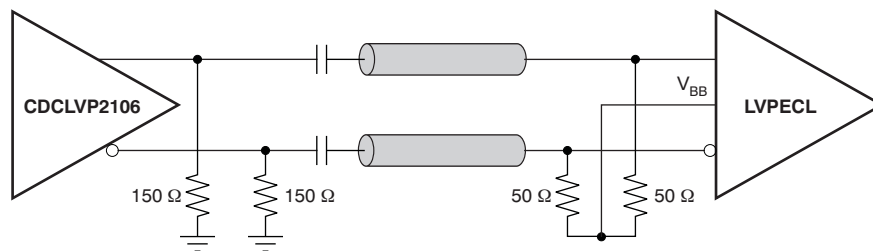


(b) Output AC Termination

Figure 14. LVPECL Output DC and AC Termination for  $V_{CC} = 2.5$  V



(a) Output DC Termination



(b) Output AC Termination

Figure 15. LVPECL Output DC and AC Termination for  $V_{CC} = 3.3\text{ V}$

### Input Termination

The CDCLVP2106 inputs can be interfaced with LVPECL, LVDS, or LVCMOS drivers. Figure 16 illustrates how to dc couple an LVCMOS input to the CDCLVP2106. The series resistance ( $R_S$ ) should be placed close to the LVCMOS driver; its value is calculated as the difference between the transmission line impedance and the driver output impedance.

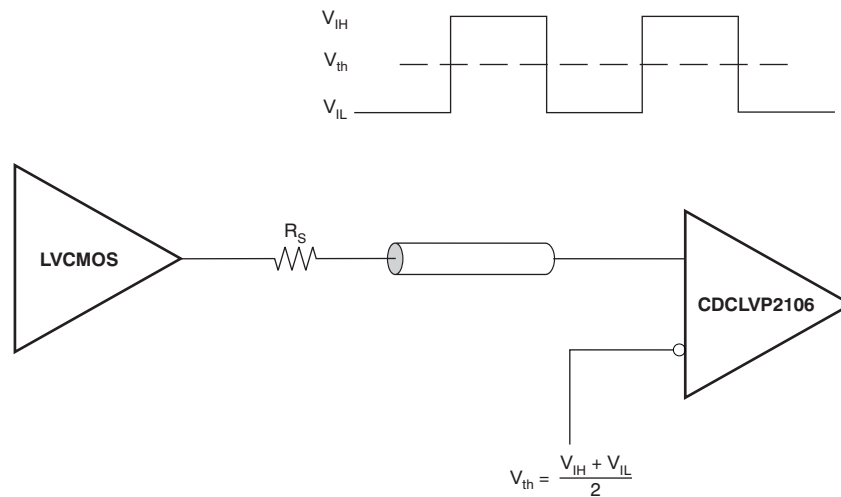


Figure 16. DC-Coupled LVCMOS Input to CDCLVP2106

Figure 17 shows how to dc couple LVDS inputs to the CDCLVP2106. Figure 18 and Figure 19 describe the method of dc coupling LVPECL inputs to the CDCLVP2106 for  $V_{CC} = 2.5\text{ V}$  and  $V_{CC} = 3.3\text{ V}$ , respectively.

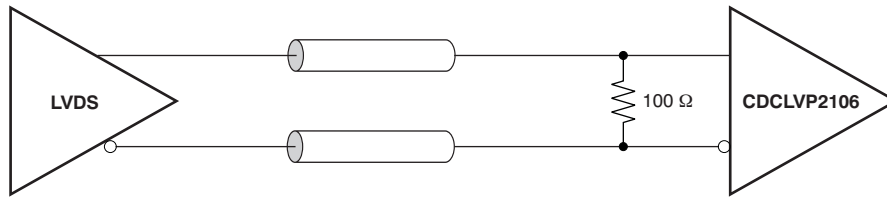


Figure 17. DC-Coupled LVDS Inputs to CDCLVP2106

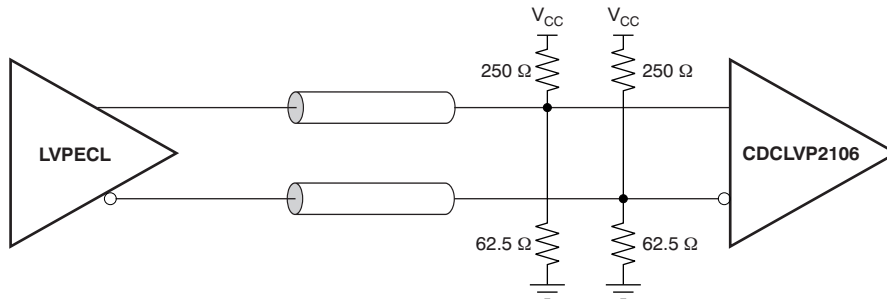


Figure 18. DC-Coupled LVPECL Inputs to CDCLVP2106 ( $V_{CC} = 2.5\text{ V}$ )

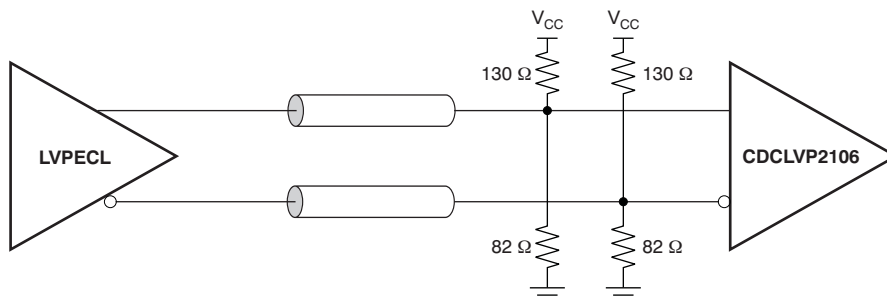


Figure 19. DC-Coupled LVPECL Inputs to CDCLVP2106 ( $V_{CC} = 3.3\text{ V}$ )

Figure 20 and Figure 21 show the technique of ac coupling differential inputs to the CDCLVP2106 for  $V_{CC} = 2.5\text{ V}$  and  $V_{CC} = 3.3\text{ V}$ , respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac coupling is required.

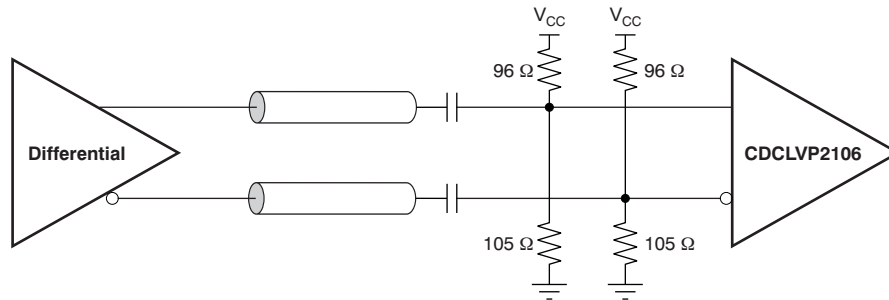


Figure 20. AC-Coupled Differential Inputs to CDCLVP2106 ( $V_{CC} = 2.5\text{ V}$ )

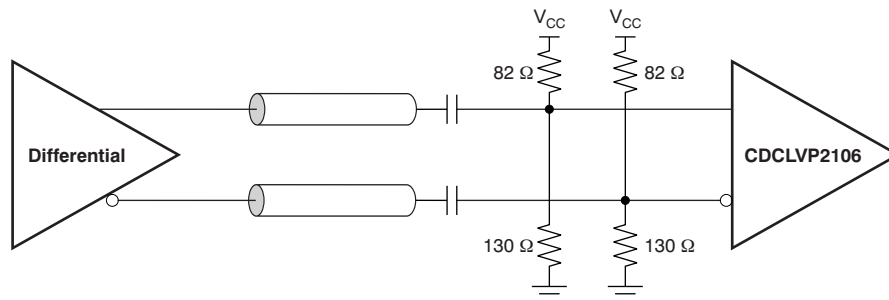


Figure 21. AC-Coupled Differential Inputs to CDCLVP2106 ( $V_{CC} = 3.3\text{ V}$ )

### REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September, 2009) to Revision A	Page
• Corrected $V_{IL}$ parameter description in <i>Electrical Characteristics</i> table for LVCMOS input .....	3
• Added footnote (2) to <i>Electrical Characteristics</i> table for LVPECL Output, $V_{CC} = 2.375\text{ V}$ to $2.625\text{ V}$ .....	4
• Revised descriptions of pins 7 and 4 .....	7
• Changed recommended resistor values in Figure 14(a) .....	13
• Changed recommended resistor values in Figure 18 .....	15



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CDCLVP2106RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCLVP2106RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP2106RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
CDCLVP2106RHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP2106RHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
CDCLVP2106RHAT	VQFN	RHA	40	250	336.6	336.6	28.6

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Package complies to JEDEC MO-220 variation VJJD-2.

## THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

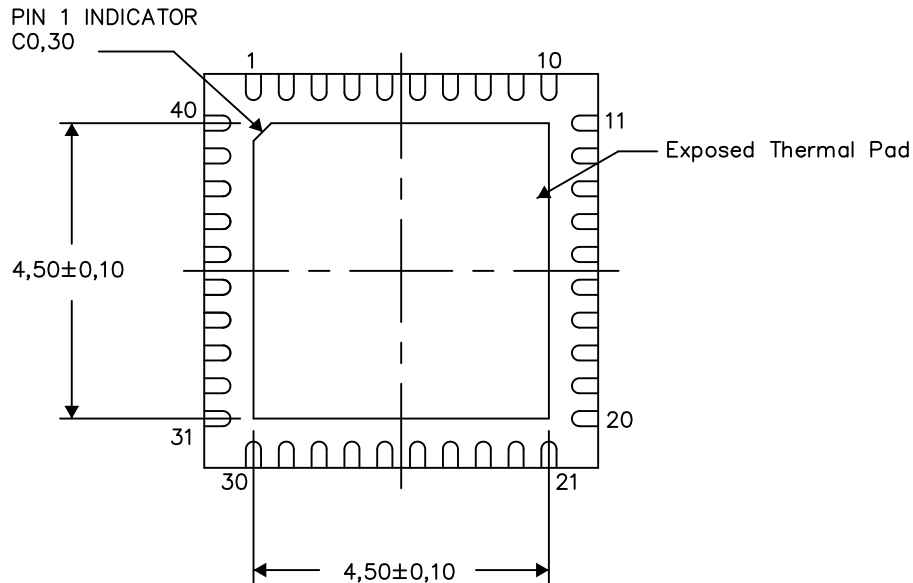
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

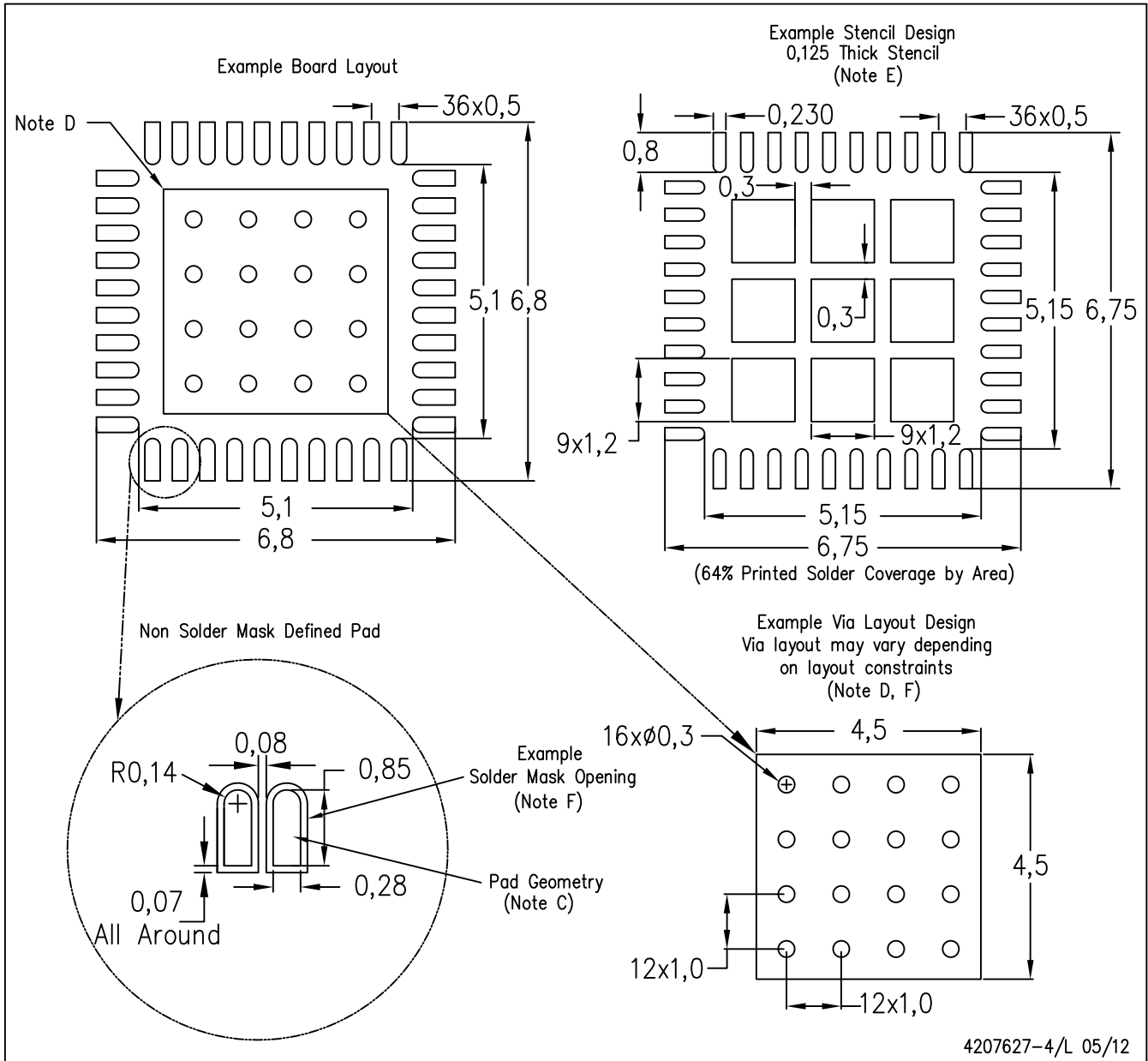
Exposed Thermal Pad Dimensions

4206355-4/Q 05/12

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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