2:12 Low Additive Jitter LVDS Buffer

Check for Samples: CDCLVD1212

FEATURES

- **2:12 Differential Buffer**
- **Low Additive Jitter: <300 fs RMS in 10 kHz to 20 MHz**
- **Low Output Skew of 50 ps (Max)**
- **Universal Inputs Accept LVDS, LVPECL, LVCMOS**
- **Selectable Clock Inputs Through Control Pin**
- **12 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible**
- **Clock Frequency up to 800 MHz**
- **2.375–2.625 V Device Power Supply**
- **LVDS Reference Voltage, V_{AC_REF}, Available for Capacitive Coupled Inputs**
- **Industrial Temperature Range –40°C to 85°C**
- **Packaged in 6mm × 6mm 40-Pin QFN (RHA)**
- **ESD Protection Exceeds 3 kV HBM, 1 kV CDM**

APPLICATIONS

- **Telecommunications/Networking**
- **Medical Imaging**
- **Test and Measurement Equipment**
- **Wireless Communications**
- **General Purpose Clocking**

DESCRIPTION

The CDCLVD1212 clock buffer distributes one of two selectable clock inputs (IN0, IN1) to 12 pairs of differential LVDS clock outputs (OUT0, OUT11) with minimum skew for clock distribution. The CDCLVD1212 can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD1212 is specifically designed for driving 50 Ω transmission lines. If driving the inputs in single ended mode, the appropriate bias voltage (V_{AC_REF}) should be applied to the unused negative input pin.

The IN_SEL pin selects the input which is routed to the outputs. If this pin is left open it disables the outputs (static). The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal.

The device operates in 2.5 V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD1212 is packaged in small 40-pin, 6mm × 6mm QFN package.

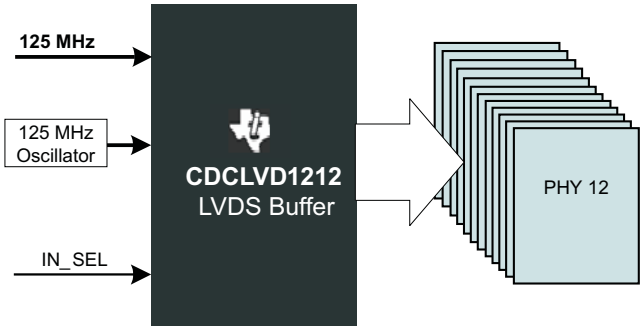


Figure 1. Application Example

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

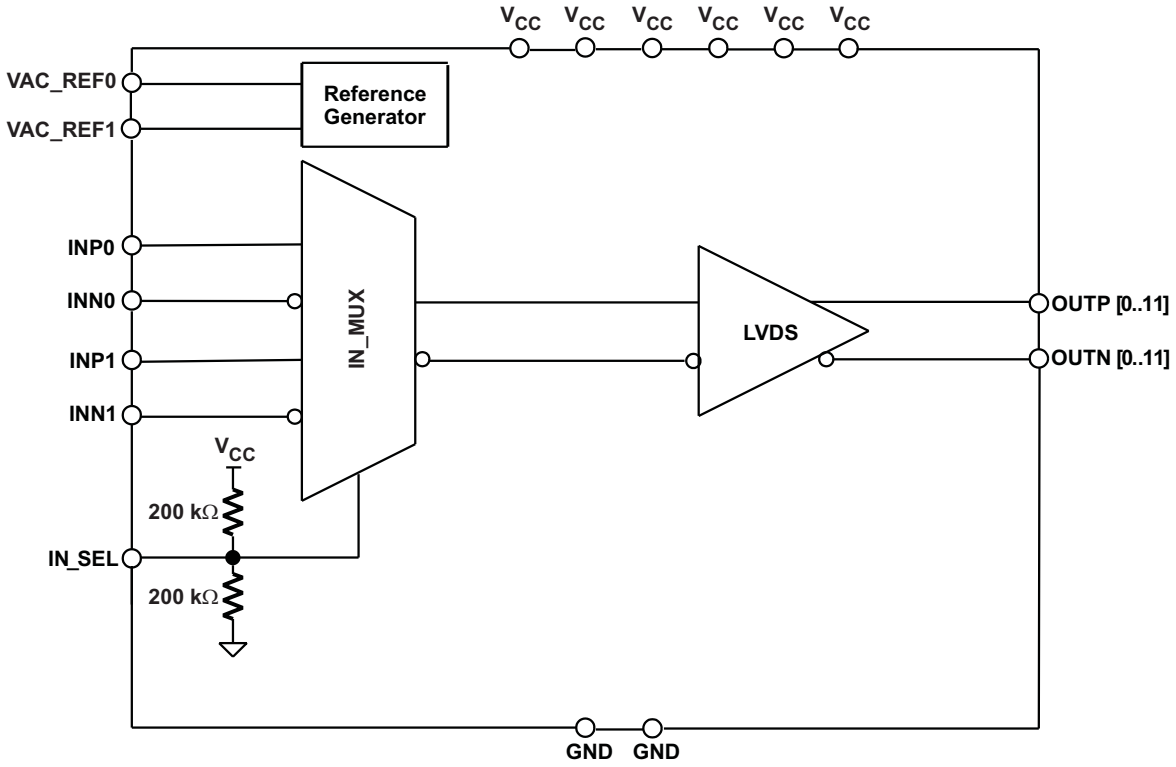
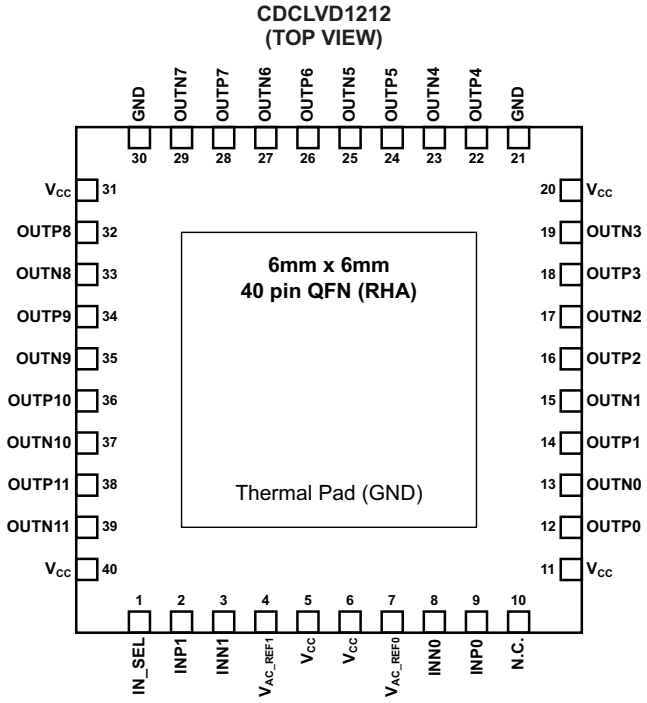


Figure 2. CDCLVD1212 Block Diagram



PIN FUNCTIONS

PIN			
NAME	NO.	TYPE	DESCRIPTION
V_{CC}	5, 6, 11, 20, 31, 40	Power	2.5V supplies for the device
GND	21, 30	Ground	Device ground
INP0, INN0	9, 8	Input	Differential input pair or single ended input
INP1, INN1	2, 3	Input	Differential redundant input pair or single ended input
OUTP0, OUTN0	12, 13	Output	Differential LVDS output pair no. 0
OUTP1, OUTN1	14, 15	Output	Differential LVDS output pair no. 1
OUTP2, OUTN2	16, 17	Output	Differential LVDS output pair no. 2
OUTP3, OUTN3	18, 19	Output	Differential LVDS output pair no. 3
OUTP4, OUTN4	22, 23	Output	Differential LVDS output pair no. 4
OUTP5, OUTN5	24, 25	Output	Differential LVDS output pair no. 5
OUTP6, OUTN6	26, 27	Output	Differential LVDS output pair no. 6
OUTP7, OUTN7	28, 29	Output	Differential LVDS output pair no. 7
OUTP8,OUTN8	32, 33	Output	Differential LVDS output pair no. 8
OUTP9,OUTN9	34, 35	Output	Differential LVDS output pair no. 9
OUTP10,OUTN10	36, 37	Output	Differential LVDS output pair no. 10
OUTP11,OUTN11	38, 39	Output	Differential LVDS output pair no. 11
V_{AC_REF0}	7	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin
V_{AC_REF1}	4	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.
N.C.	10		No connect
IN_SEL	1	Input with an internal 200kΩ pull-up and pull-down	Input selection – selects input port; (See Table 1)
Thermal Pad		Ground	Device ground. Thermal pad must be soldered to ground. See thermal management recommendations

Table 1. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	INP0, INN0
1	INP1, INN1
Open	None(1)

(1) The input buffers are disabled and the outputs are static.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE	UNIT
Supply voltage range, V_{CC}	–0.3 to 2.8	V
Input voltage range, V_I	–0.2 to (V_{CC} + 0.2)	V
Output voltage range, V_O	–0.2 to (V_{CC} + 0.2)	V
Driver short circuit current, I_{OSD}	See Note (2)	
Electrostatic discharge (Human Body Model, 1.5 kΩ, 100 pF)	>3000	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The outputs can handle permanent short.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Device supply voltage, V_{CC}	2.375	2.5	2.625	V
Ambient temperature, T_A	–40		85	°C

THERMAL INFORMATION

THERMAL METRIC(1)		CDCLVD1212 RHA (40 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	31.0	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	28.7	
θ_{JB}	Junction-to-board thermal resistance	9.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	9.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At V_{CC} = 2.375V to 2.625V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN_SEL CONTROL INPUT CHARACTERISTICS						
V_{dI3}	3 State	Open		0.5×V_{CC}		V
V_{dIH}	Input high voltage		0.7×V_{CC}			V
V_{dIL}	Input low voltage				0.2×V_{CC}	V
I_{dIH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			30	µA
I_{dIL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–30	µA
$R_{pull(IN\_SEL)}$	Input pull-up/ pull-down resistor			200		kΩ
2.5V LVCMOS (see Figure 7) INPUT CHARACTERISTICS						
f_{IN}	Input frequency				200	MHz
V_{th}	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
V_{IH}	Input high voltage		V_{th} + 0.1		V_{CC}	V
V_{IL}	Input low voltage		0		V_{th} – 0.1	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20%–80%	1.5			V/ns
C_{IN}	Input capacitance			2.5		pF
DIFFERENTIAL INPUT CHARACTERISTICS						
f_{IN}	Input frequency	Clock input			800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	V_{ICM} = 1.25 V	0.3		1.6	V_{PP}
V_{ICM}	Input common mode voltage range	$V_{IN, DIFF, PP}$ > 0.4 V	1.0		V_{CC} – 0.3	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20%–80%	0.75			V/ns
C_{IN}	Input capacitance			2.5		pF

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 2.375V to 2.625V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS OUTPUT CHARACTERISTICS						
$\|V_{OD}\|$	Differential output voltage magnitude	$V_{IN, DIFF, PP}$ = 0.3V, R_L = 100 Ω	250		450	mV
ΔV_{OD}	Change in differential output voltage magnitude		–15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP}$ = 0.6V, R_L = 100 Ω	–15		15	mV
V_{ring}	Output overshoot and undershoot	Percentage of output amplitude V_{OD}			10%	
V_{OS}	Output ac common mode	$V_{IN, DIFF, PP}$ = 0.6V, R_L = 100 Ω		40	70	mV_{PP}
I_{OS}	Short-circuit output current	V_{OD} = 0 V			±24	mA
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.3 V		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
$t_{SK, O}$	Output skew				50	ps
$t_{SK,P}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	Edge speed 0.75 V/ns, 10 kHz – 20 MHz			0.3	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%, 100 Ω, 5 pF	50		300	ps
I_{CCSTAT}	Static supply current	Outputs unterminated, f = 0 Hz		17	28	mA
I_{CC100}	Supply current	All outputs, R_L = 100 Ω, f = 100 MHz		85	110	mA
I_{CC800}	Supply current	All outputs, R_L = 100 Ω, f = 800 MHz		117	146	mA
V_{AC_REF} CHARACTERISTICS						
V_{AC_REF}	Reference output voltage	V_{CC} = 2.5 V, I_{load} = 100 µA	1.1	1.25	1.35	V

Typical Additive Phase Noise Characteristics for 100 MHz Clock

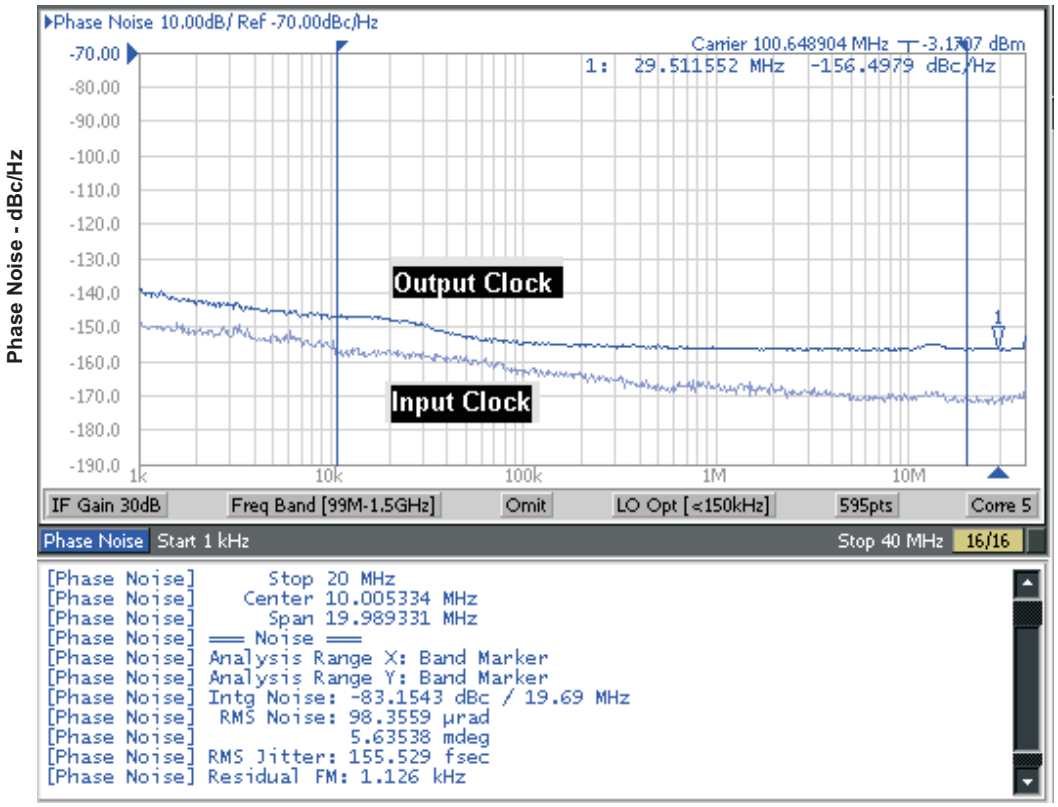
PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		-138		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

TYPICAL CHARACTERISTICS

INPUT- AND OUTPUT-CLOCK PHASE NOISES
vs
FREQUENCY FROM the CARRIER
(T_A = 25°C and V_{CC} = 2.5V)



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

Figure 3. 100 MHz Input and Output Phase Noise Plot

TYPICAL CHARACTERISTICS (continued)

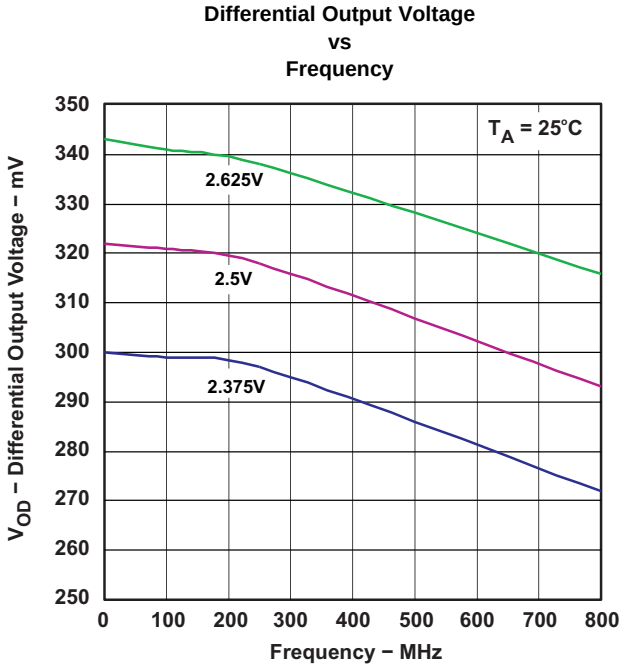


Figure 4.

TEST CONFIGURATIONS

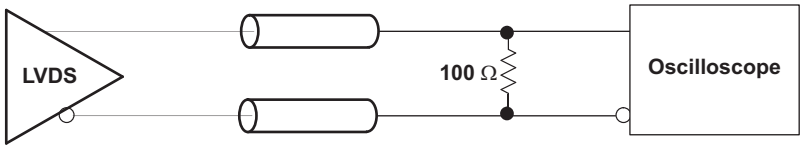


Figure 5. LVDS Output DC Configuration During Device Test

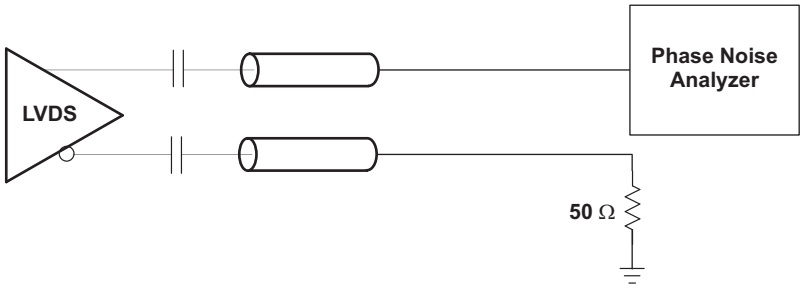


Figure 6. LVDS Output AC Configuration During Device Test

TYPICAL CHARACTERISTICS (continued)

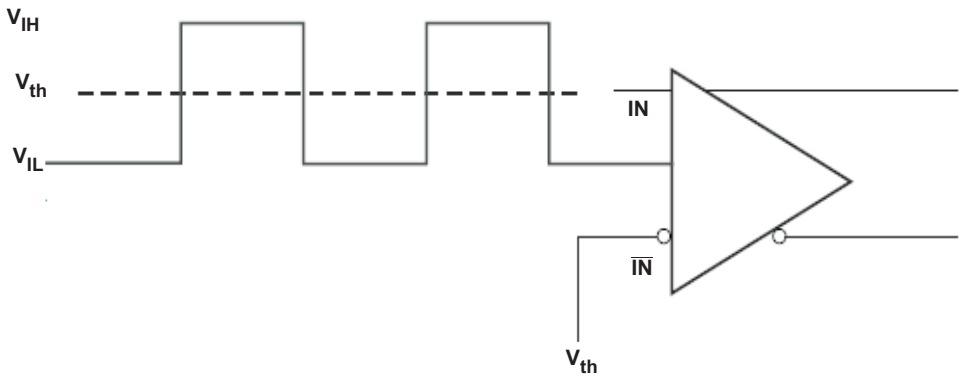


Figure 7. DC Coupled LVCMOS Input During Device Test

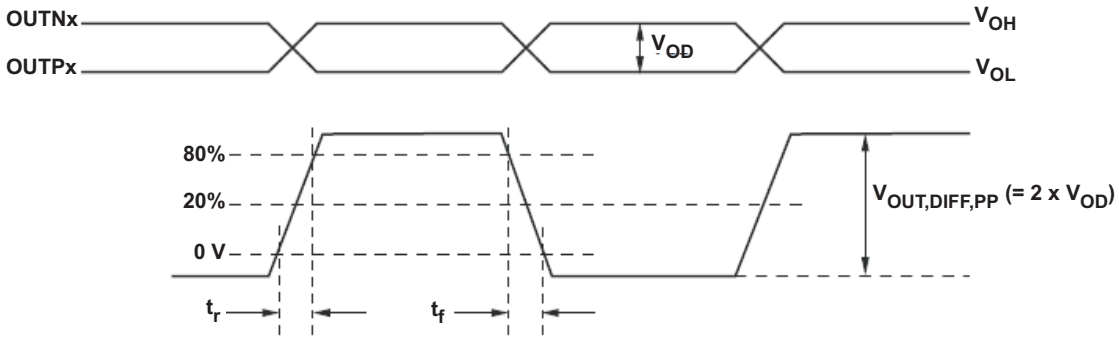
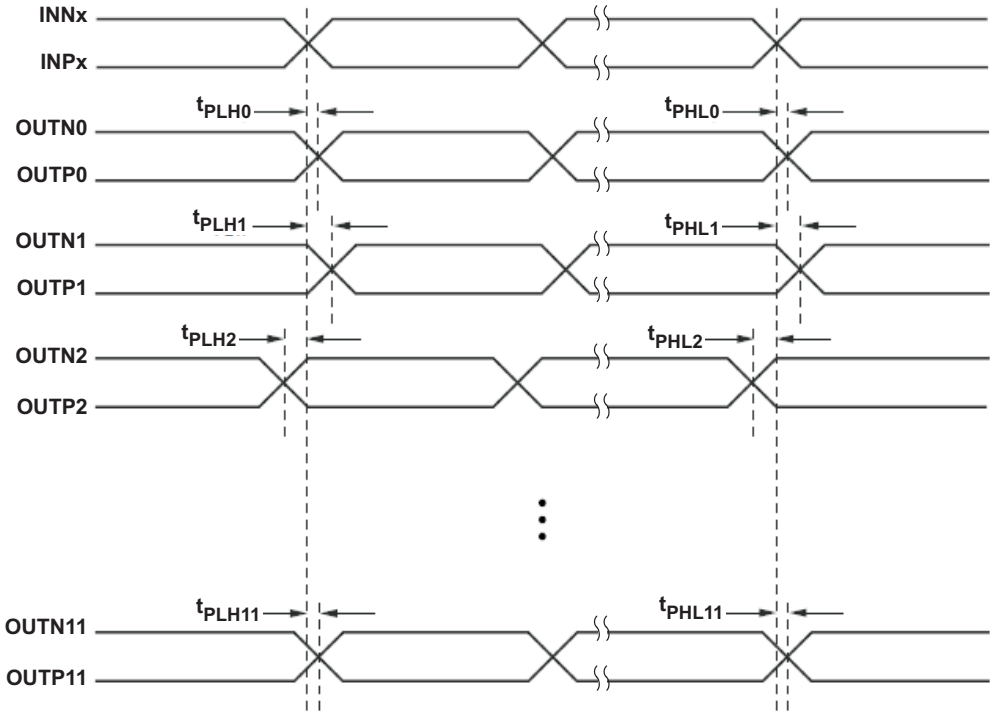


Figure 8. Output Voltage and Rise/Fall Time

TYPICAL CHARACTERISTICS (continued)



A. Output skew is calculated as the greater of the following: As of the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..11)

B. Part to part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..11)

Figure 9. Output Skew and Part-to-Part Skew

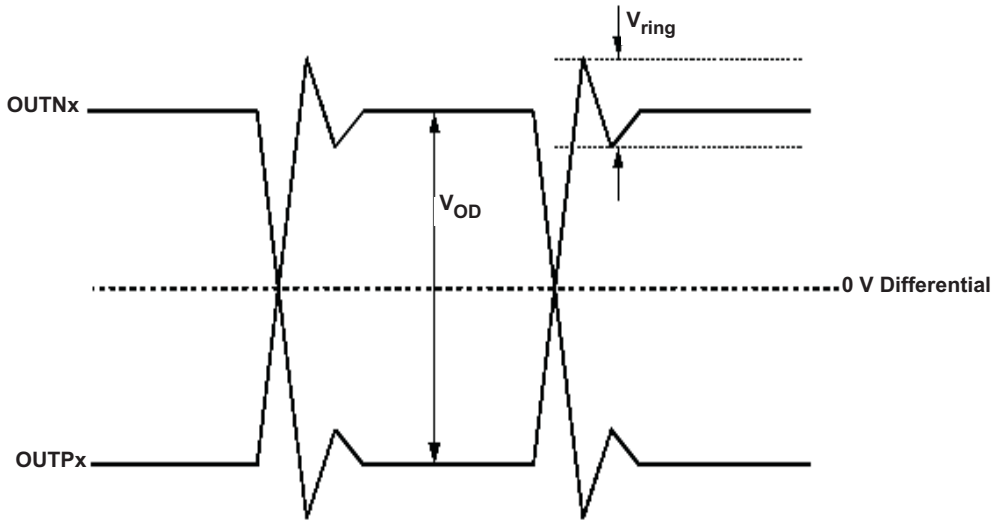


Figure 10. Output Overshoot and Undershoot

TYPICAL CHARACTERISTICS (continued)

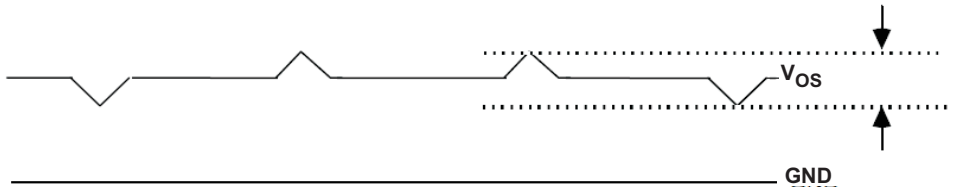


Figure 11. Output AC Common Mode

APPLICATION INFORMATION

THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Check the mechanical data at the end of the data sheet for land and via pattern examples.

POWER SUPPLY FILTERING

High-performance clock buffers are sensitive to noises on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to the application.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1 μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

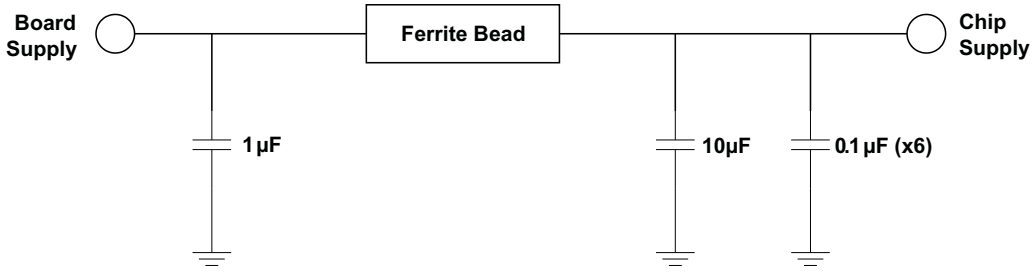


Figure 12. Power Supply Filtering

LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resister close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD1212, ac-coupling should be used. If the LVDS receiver has internal 100 Ω termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.

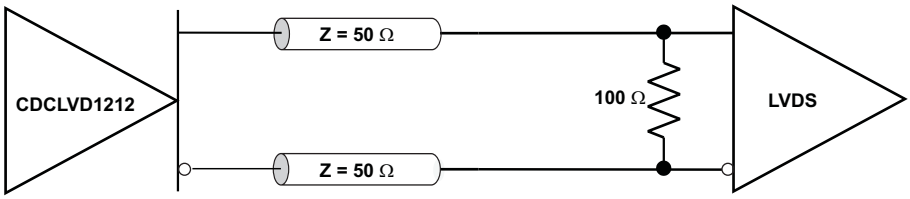


Figure 13. LVDS Output DC Termination

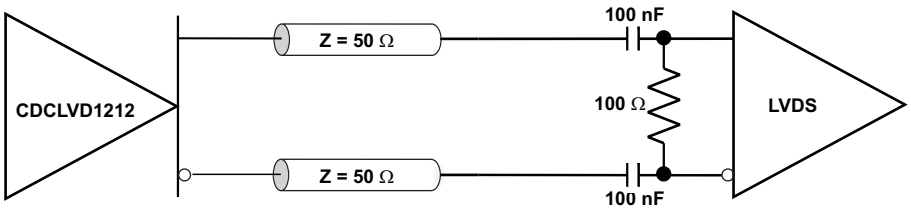


Figure 14. LVDS Output AC Termination with Receiver Internally Biased

INPUT TERMINATION

The CDCLVD1212 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD1212 inputs with dc or ac coupling as shown Figure 15 and Figure 16 respectively.

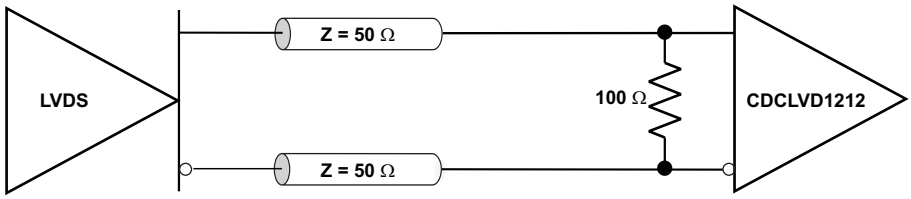


Figure 15. LVDS Clock Driver Connected to CDCLVD1212 Input (DC coupled)

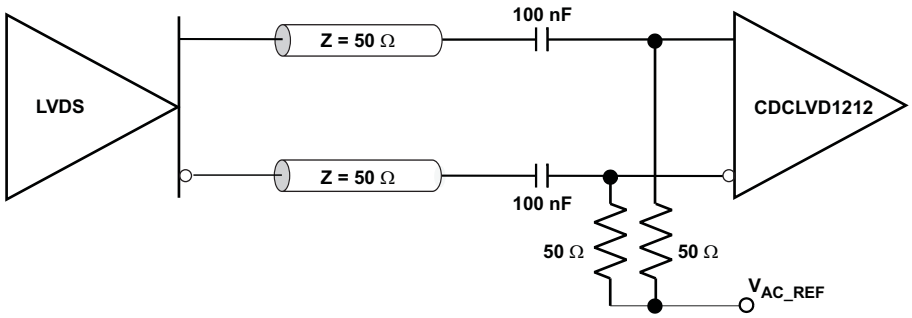


Figure 16. LVDS Clock Driver Connected to CDCLVD1212 Input (AC coupled)

Figure 17 shows how to connect LVPECL inputs to the CDCLVD1212. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

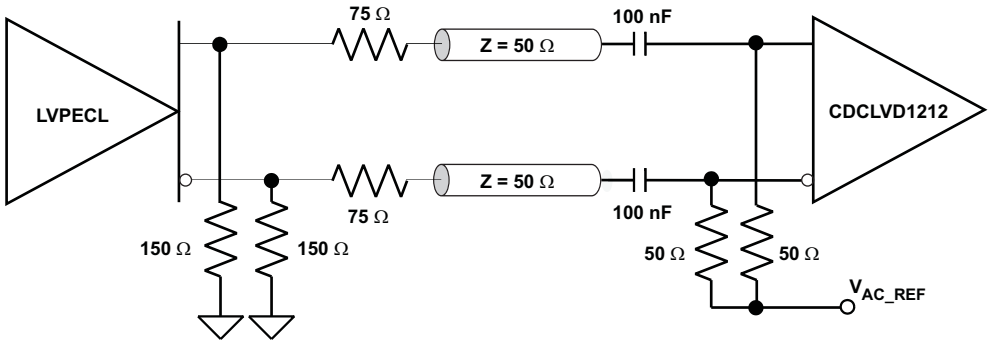


Figure 17. LVPECL Clock Driver Connected to CDCLVD1212 Input

Figure 18 illustrates how to couple a 2.5 V LVCMOS clock input to the CDCLVD1212 directly. The series resistance (R_S) should be placed close to the LVCMOS driver if needed. 3.3 V LVCMOS clock input swing needs to be limited to $V_{IH} \leq V_{CC}$.

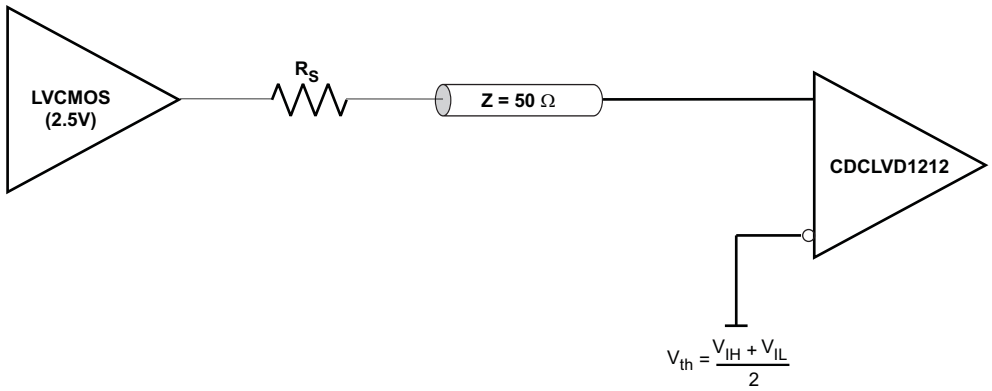


Figure 18. 2.5V LVCMOS Clock Driver Connected to CDCLVD1212 Input

For unused inputs, it is recommended to ground both input pins (INP, INN) using 1 kΩ resistors.

REVISION HISTORY

Changes from Original (September 2010) to Revision A	Page
• Deleted the Recommended PCB Layout illustration	10

Changes from Revision A (November 2010) to Revision B	Page
• Changed the device status From: Product Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CDCLVD1212RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CDCLVD1212RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

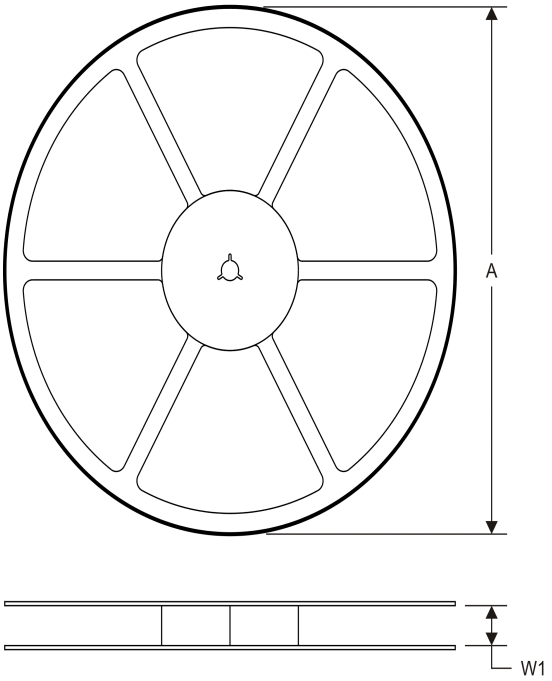
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

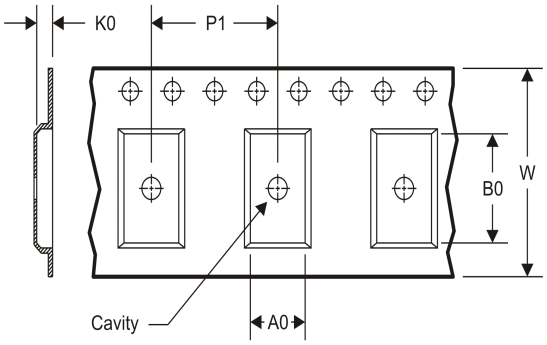
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



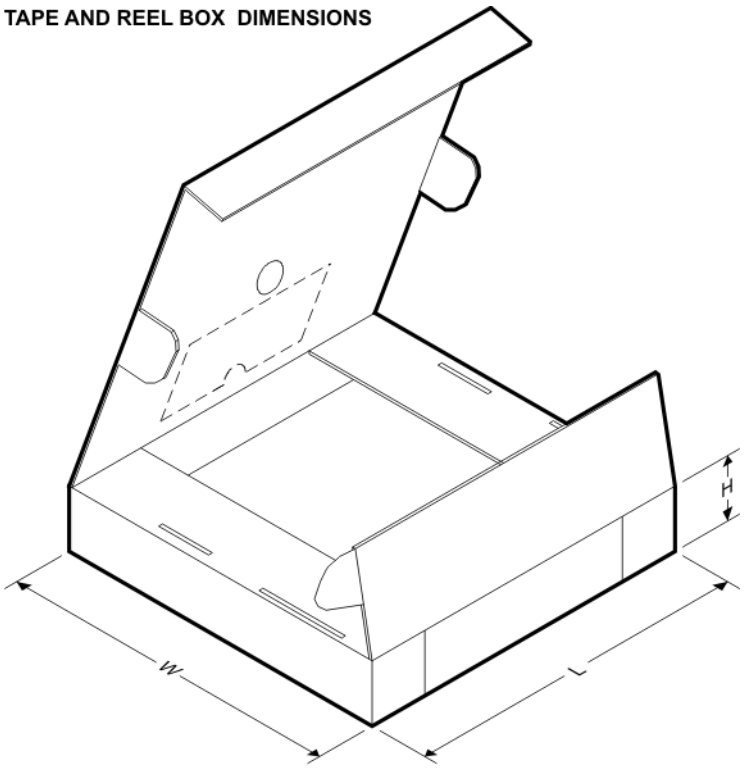
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD1212RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
CDCLVD1212RHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

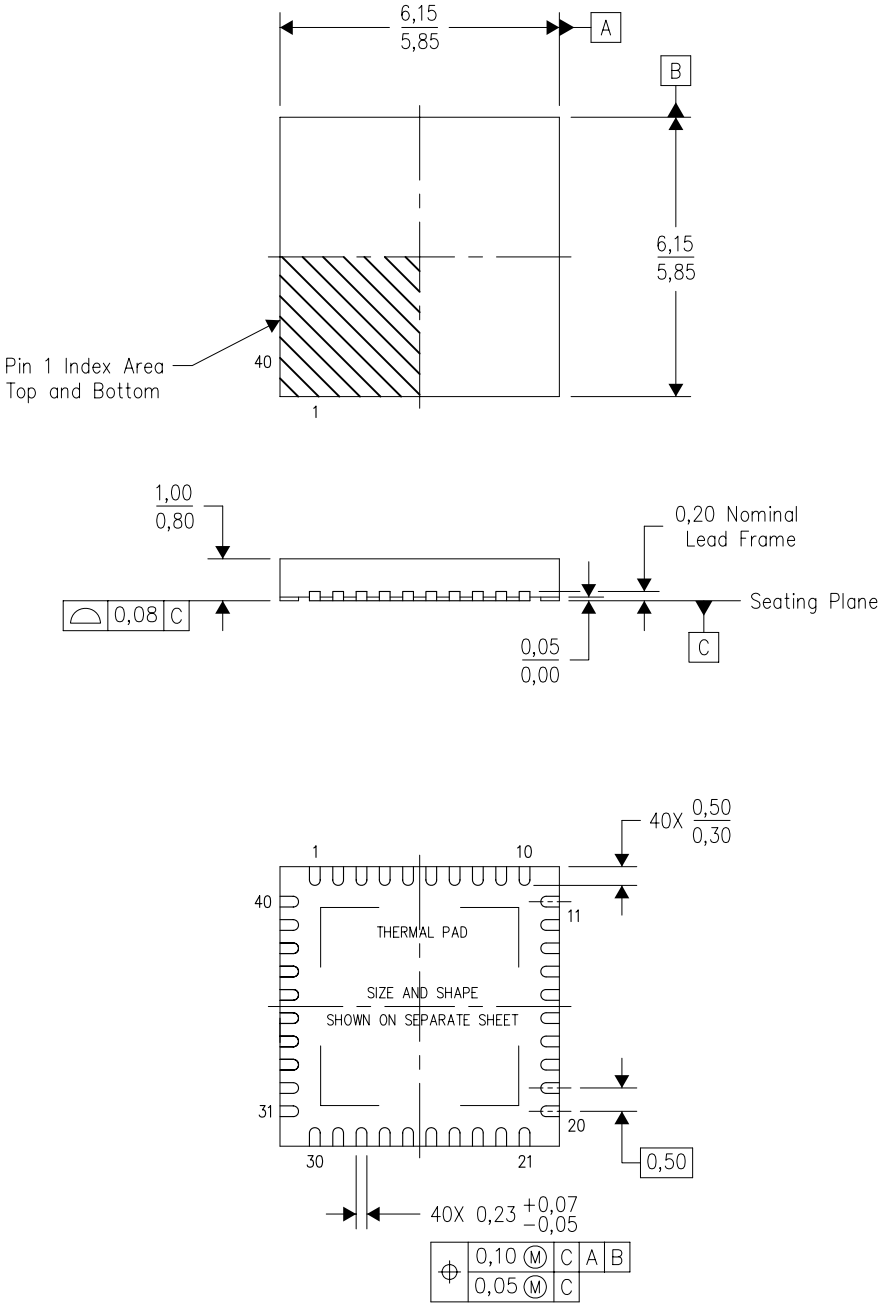
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD1212RHAR	VQFN	RHA	40	2500	336.6	336.6	28.6
CDCLVD1212RHAT	VQFN	RHA	40	250	336.6	336.6	28.6

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

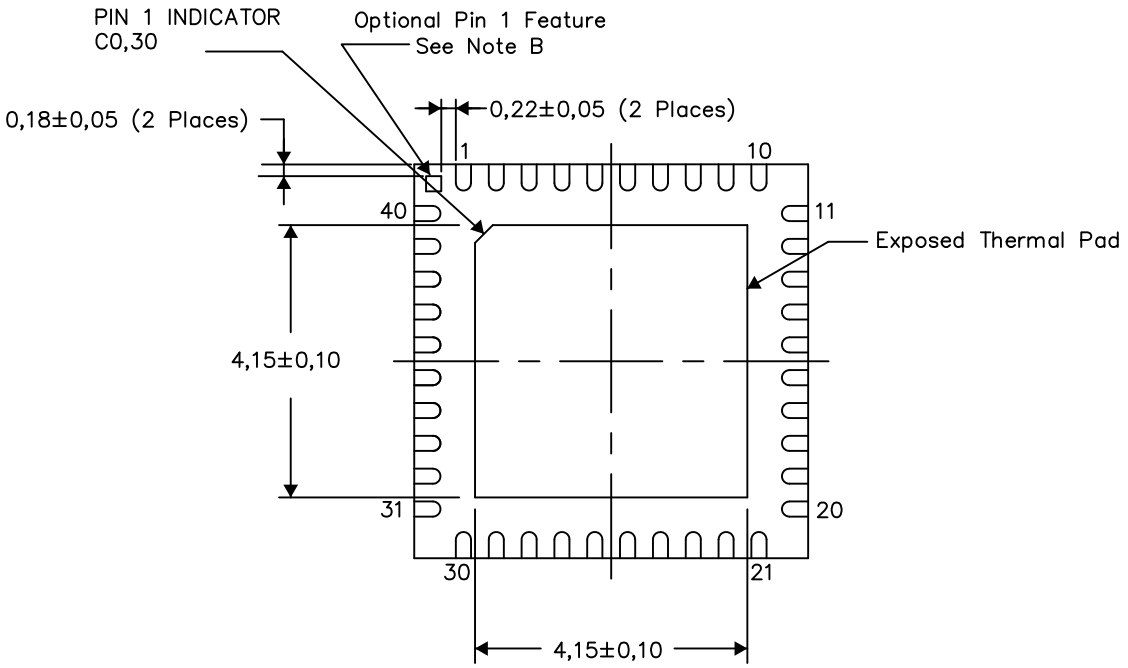
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

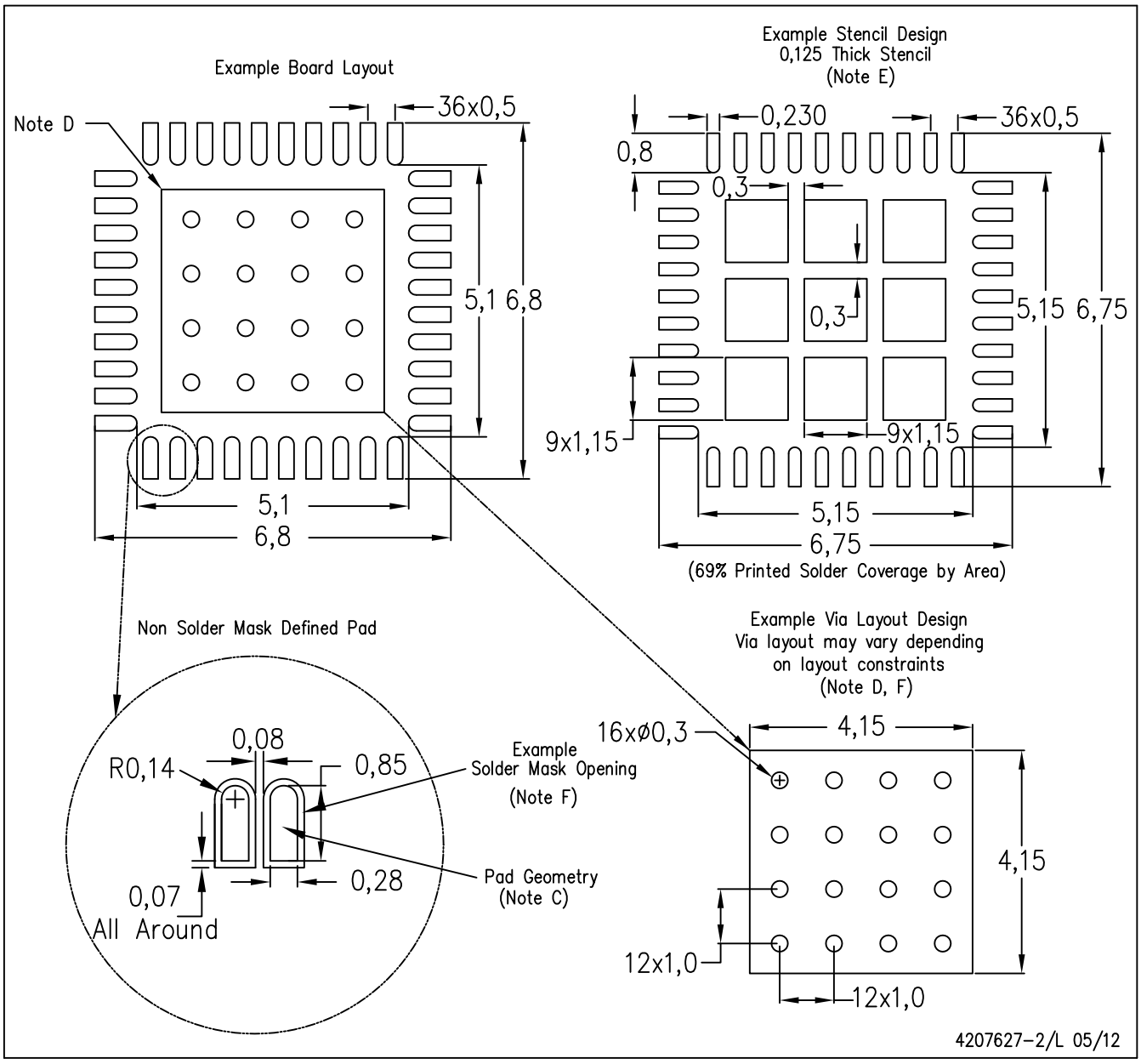
Exposed Thermal Pad Dimensions

4206355–2/Q 05/12

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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