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 Members of the Texas Instruments Widebus™ Family 	SN54LVTH16500 WD PACKAGE SN74LVTH16500 DGG OR DL PACKAGE (TOP VIEW)
 UBT [™] Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode 	OEAB [1 56] GND LEAB [2 55] CLKAB A1 [3 54] B1
 Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC}) 	GND [] 4 53] GND A2 [] 5 52] B2
 Support Unregulated Battery Operation Down to 2.7 V 	A3 [] 6 51 [] B3 V _{CC} [] 7 50 [] V _{CC}
 Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	A4 8 49 B4 A5 9 48 B5 A6 10 47 B6
 I_{off} and Power-Up 3-State Support Hot Insertion 	GND 11 46 GND A7 12 45 B7
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	A8 0 13 44 0 B8 A9 0 14 43 0 B9
 Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise 	A10 15 42 B10 A11 16 41 B11 A12 17 40 B12
 Flow-Through Architecture Optimizes PCB Layout 	GND [] 18 39 [] GND A13 [] 19 38 [] B13
 Latch-Up Performance Exceeds 500 mA Per JESD 17 	A14 20 37 B14 A15 21 36 B15
 ESD Protection Exceeds JESD 22 2000-V Human-Body Model (A114-A) 200 V Machine Model (A115 A) 	V _{CC}
 200-V Machine Model (A115-A) 1000-V Charged-Device Model (C101) 	GND 25 32 GND A18 26 31 B18
description/ordering information	ОЕВА [] 27 30 [] СLКВА LEBA [] 28 29 [] GND
The 21/THICEOO devices are 10 bit universal bus	

(

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

TA	PACKAGE	-	ORDERABLE PART NUMBER	TOP-SIDE MARKING
		Tube	SN74LVTH16500DL	
	SSOP – DL	Tape and reel	SN74LVTH16500DLR	LVTH16500
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74LVTH16500DGGR	LVTH16500
	VFBGA – GQL	Tana and so al	SN74LVTH16500GQLR	11.500
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74LVTH16500ZQLR	LL500
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16500WD	SNJ54LVTH16500WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information (continued)

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)

	_	1	2	3	4	5	6
A		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\odot
в		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
С		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
D		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
Е		\bigcirc	\bigcirc			\bigcirc	\bigcirc
F		\bigcirc	\bigcirc			\bigcirc	\bigcirc
G		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
н		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
J		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc
κ		\bigcirc	С	С	С	\bigcirc	С

terminal assignments

	1	2	3	4	5	6
Α	A1	LEAB	OEAB	GND	CLKAB	B1
в	A3	A2	GND	GND	B2	B3
С	A5	A4	VCC	VCC	B4	B5
D	A7	A6	GND	GND	B6	B7
Е	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
н	A14	A15	VCC	VCC	B15	B14
J	A16	A17	GND	GND	B17	B16
к	A18	OEBA	LEBA	GND	CLKBA	B18



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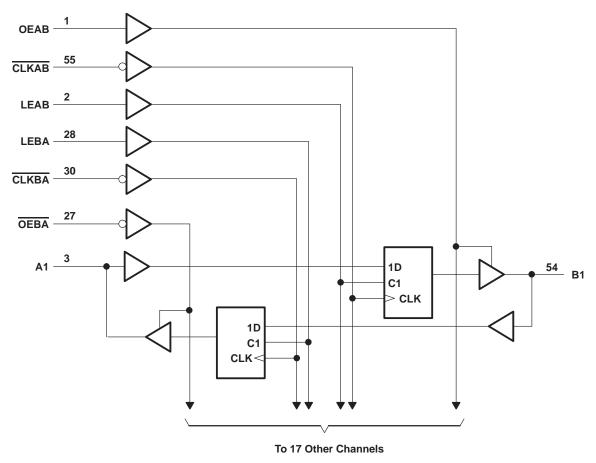
	FUNCTION TABLE [†]											
	INPUTS											
OEAB	OEAB LEAB <mark>CLKAB</mark> A											
L	Х	Х	Х	Z								
н	Н	Х	L	L								
н	Н	Х	Н	н								
н	L	\downarrow	L	L								
н	L	\downarrow	Н	н								
н	L	Н	Х	в ₀ ‡ в ₀ §								
Н	L	L	Х	в ₀ §								

[†] A-to-B data flow is shown: B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

[‡]Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)	7 V
Voltage range applied to any output in the high state, V _O (see Note 1)0.5 V to V _{CC} + 0.5	5 V
Current into any output in the low state, I _O : SN54LVTH16500	nA
SN74LVTH16500	nA
Current into any output in the high state, I _O (see Note 2): SN54LVTH16500	
SN74LVTH16500 64 m	nA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	nA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	
DL package	
GQL/ZQL package	
Storage temperature range, T _{stg} 65°C to 150°	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH	116500	SN74LVTI	H16500	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	M	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage		5	5.5		5.5	V
IOH	High-level output current		4	-24		-32	mA
IOL	Low-level output current		200	48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	201	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		Q 200		200		μs/V
Т _А	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN5	4LVTH16	500	SN74	4LVTH16	6500			
PA	RAMETER	TEST C	ONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT		
VIK		V _{CC} = 2.7 V,	l _l = –18 mA			-1.2			-1.2	V		
		V_{CC} = 2.7 V to 3.6 V,	I _{OH} = –100 μA	V _{CC} -0	.2		V _{CC} -0.	.2				
		V _{CC} = 2.7 V,	IOH = -8 mA	2.4			2.4					
VOH			I _{OH} = -24 mA	2						V		
		$V_{CC} = 3 V$	I _{OH} = -32 mA				2					
			I _{OL} = 100 μA			0.2			0.2			
		$V_{CC} = 2.7 V$	I _{OL} = 24 mA			0.5			0.5			
			I _{OL} = 16 mA			0.4			0.4			
VOL			I _{OL} = 32 mA			0.5			0.5	V		
		$V_{CC} = 3 V$	I _{OL} = 48 mA			0.55						
			I _{OL} = 64 mA						0.55			
	Constructions when	V _{CC} = 3.6 V,	$V_I = V_{CC} \text{ or } GND$			±1			±1			
	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V		1	10			10			
lj -	A or B ports‡		V _I = 5.5 V		PEL	20			20	μA		
		V _{CC} = 3.6 V	$V_I = V_{CC}$		2	1			1			
			$V_{I} = 0$		5	-5			-5			
loff		$V_{CC} = 0,$	$V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5 \text{ V}$	0	2				±100	μΑ		
			V _I = 0.8 V	75			75					
ll(hold)	A or B ports	$V_{CC} = 3 V$	V _I = 2 V	-75		-75			μA			
()		V _{CC} = 3.6 V§,	V _I = 0 to 3.6 V						±500			
IOZPU		$\frac{V_{CC}}{OE/OE} = 0$ to 1.5 V, V _O = OE/OE = don't care	0.5 V to 3 V,			±100*			±100	μΑ		
IOZPD		$\frac{V_{CC}}{OE/OE} = 1.5 \text{ V to 0, V}_{O} = 0$	0.5 V to 3 V,			±100*			±100	μΑ		
	V _{CC} = 3.6 V,		Outputs high			0.19			0.19			
ICC		$I_{O} = 0,$	Outputs low			5			5	mA		
V _I = V		$V_{I} = V_{CC}$ or GND	Outputs disabled			0.19			0.19			
∆ICC¶		V_{CC} = 3 V to 3.6 V, On Other inputs at V _{CC} or				0.2			0.2	mA		
Ci		V _I = 3 V or 0			4			4		pF		
Cio		V _O = 3 V or 0			10			10	10 p			

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				5	SN54LV	TH16500		5	SN74LV	TH16500		
			V _{CC} = 3.3 V ± 0.3 V V _{CC} = 2.7 V				2.7 V	= V _{CC} ± 0.		V _{CC} =	2.7 V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			150		150		150		150	MHz	
	Dules duration	LE high		3.3		3.3		3.3		3.3		
tw	Pulse duration	CLK high or low		3.3		3.3		3.3		3.3		ns
		A before CLKAB↓		3.1		3.1		2.9		2.9		
	O	B before CLKBA↓		3.1		3.1		2.9		2.9		
^t su	Setup time		CLK high	1.5	202	0.6		1.4		0.5		ns
		A or B before LE \downarrow	CLK low	3.1	0	2.5		2.9		2.3		
		A or B after $\overline{CLK}\downarrow$	-	0.4	2	0.4		0.4		0.4		
th	_h Hold time	A or B after LE \downarrow		1.7		1.7		1.6		1.6		ns

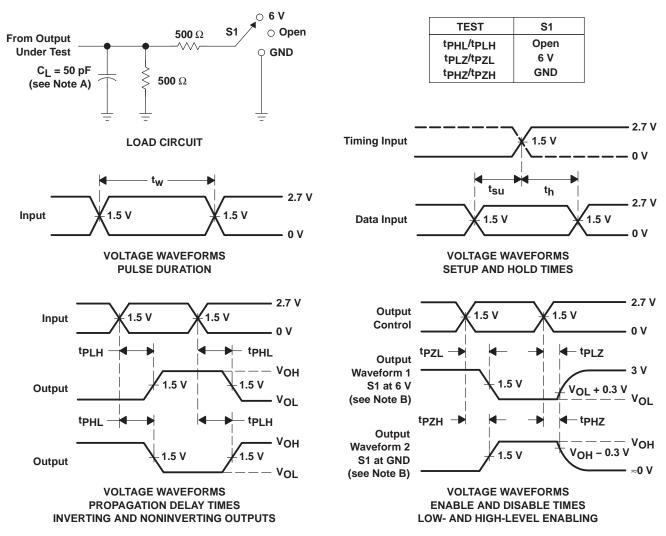
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

			5	SN54LV	TH16500			SN74	LVTH1	6500		
PARAMETER	FROM (INPUT)	TO (OUTPUT)			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f _{max}			150		150		150			150		MHz
^t PLH	B or A	A an D	1.2	3.9		4.1	1.3	2.8	3.7		4	
^t PHL	BOIA	A or B	1.2	3.9	M	4.1	1.3	2.6	3.7		4	ns
^t PLH	LEBA or LEAB	A	1.4	5.5	M	5.9	1.5	3.8	5.1		5.7	
^t PHL	LEDA OI LEAD	A or B	1.4	5.5	J'Y'	5.9	1.5	3.8	5.1		5.7	ns
^t PLH	CLKBA or	A D	1.2	5.3	1.	6.1	1.3	3.6	5		5.9	
^t PHL	CLKAB	A or B	1.2	5.3		6.1	1.3	3.5	5		5.9	ns
^t PZH		A an D	1.2	5.1		5.8	1.3	3.6	4.8		5.5	
^t PZL	OEBA or OEAB	A or B	1.2	Q 5.1		5.8	1.3	3.6	4.8		5.5	ns
^t PHZ	OEBA or OEAB	A or B	1.6	6.1		6.6	1.7	4.5	5.8		6.3	
^t PLZ	OEDA UI ÜEAD	AUB	1.6	6.1		6.6	1.7	4.1	5.8		6.3	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25° C.



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	0	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
74LVTH16500DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples
74LVTH16500DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples
SN74LVTH16500DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples
SN74LVTH16500DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples
SN74LVTH16500DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples
SN74LVTH16500GQLR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	LL500	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.



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11-Apr-2013

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OTHER QUALIFIED VERSIONS OF SN74LVTH16500 :

Enhanced Product: SN74LVTH16500-EP

NOTE: Qualified Version Definitions:

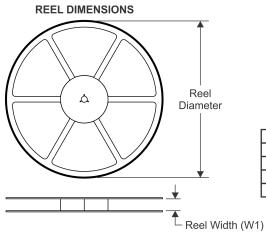
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

26-Jan-2013



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



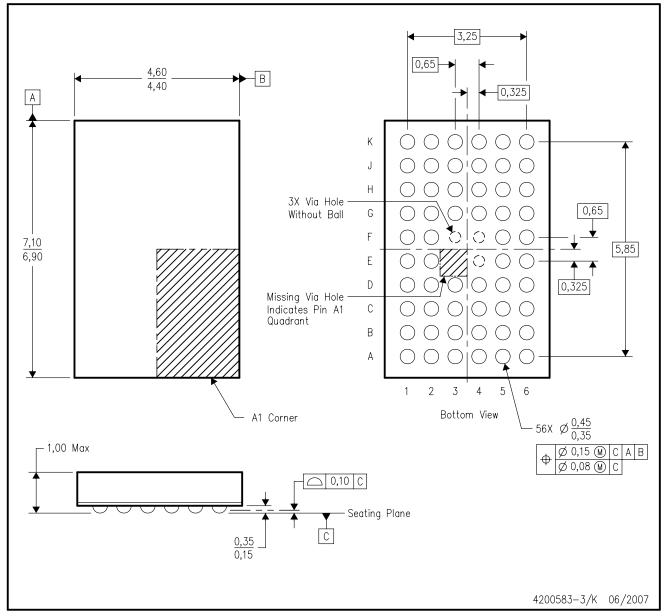
- A. All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice. В.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15). C.
 - D. Falls within JEDEC MO-118

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GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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