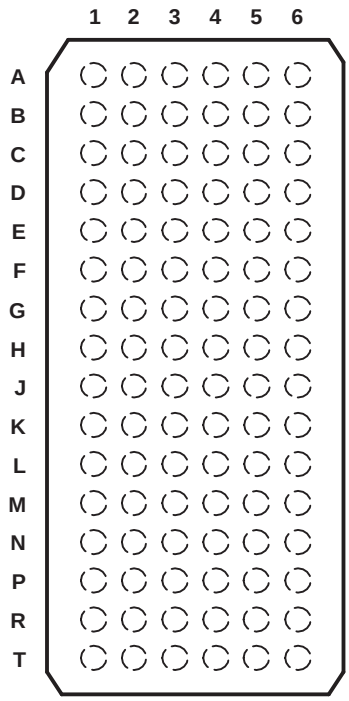
SN74LVTH32374
3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS752D–SEPTEMBER 2000–REVISED AUGUST 2007

FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Supports Unregulated Battery Operation Down to 2.7 V**

GKE OR ZKE PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1Q2	1Q1	1$\overline{OE}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	1V_{CC}	1V_{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	1V_{CC}	1V_{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	2$\overline{OE}$	2CLK	2D8	2D7
J	3Q2	3Q1	3$\overline{OE}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	2V_{CC}	2V_{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	2V_{CC}	2V_{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4$\overline{OE}$	4CLK	4D8	4D7

DESCRIPTION/ORDERING INFORMATION

The SN74LVTH32374 is a 32-bit edge-triggered D-type flip-flop designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Reel of 1000	SN74LVTH32374GKER	HV374
	LFBGA – ZKE (Pb-free)		SN74LVTH32374ZKER	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

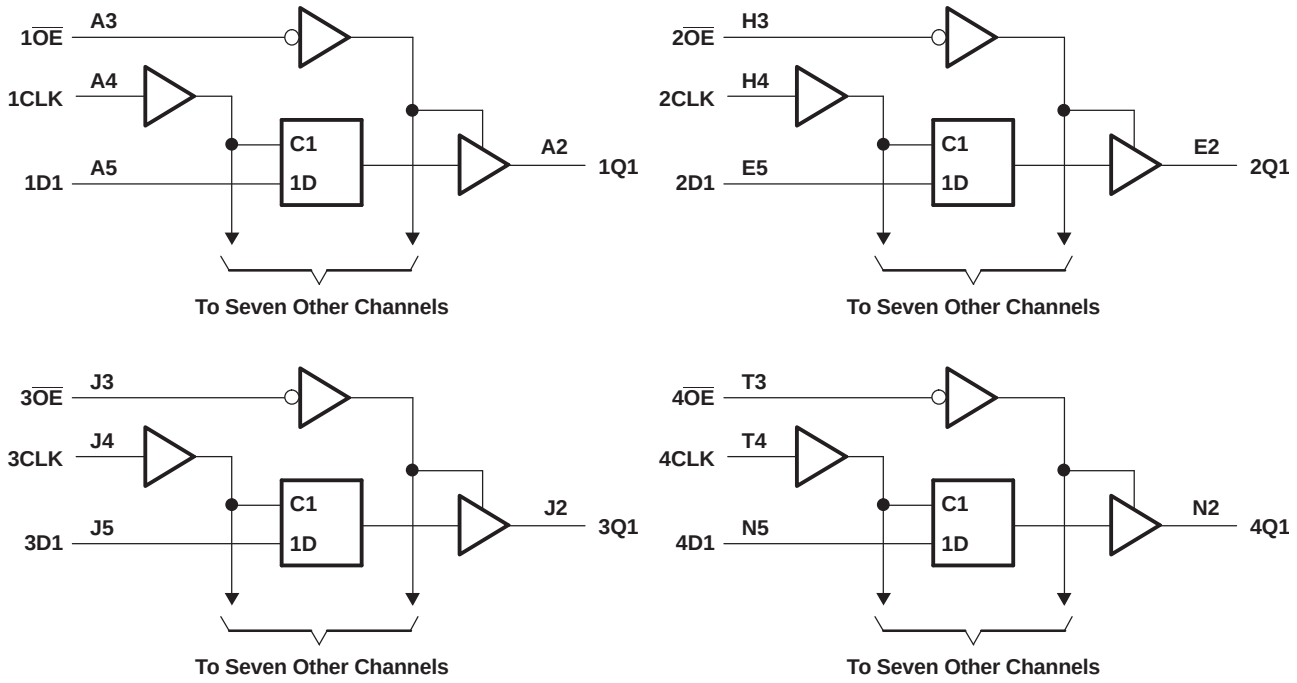
This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

FUNCTION TABLE
(each 8-bit flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Voltage range applied to any output int he high state(2)		–0.5	V_{CC} + 0.5	V
I_O	Current into any output in the low state			128	mA
I_O	Current into any output in the high state(3)			64	mA
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
θ_{JA}	Package thermal impedance(4)	GKE/ZKE package		40	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		μs/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			
		V_{CC} = 3 V,	I_{OH} = –32 mA	2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
I_I		V_{CC} = 3.6 V,	V_I = 5.5 V			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
	Data inputs	V_{CC} = 0 or 3.6 V	V_I = V_{CC}			1	
			V_I = 0			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
		V_{CC} = 3.6 V,(2)	V_I = 0 to 3.6 V			500 –750	
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			–5	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.38	mA
			Outputs low			10	
			Outputs disabled			0.38	
ΔI_{CC}(3)		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2	mA
C_i		V_I = 3 V or 0			4		pF
C_o		V_O = 3 V or 0			9		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			160		160	MHz
t_w	Pulse duration, CLK high or low		3		3		ns
t_{su}	Setup time, data before CLK↑	High or low	1.8		2		ns
t_h	Hold time, data after CLK↑	High or low	0.8		0.1		ns

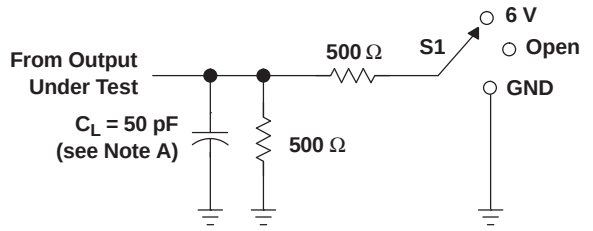
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP(1)	MAX	MIN	MAX	
f_{max}			160			160		MHz
t_{PLH}	A	Q	1.9	3	4.5		5.2	ns
t_{PHL}			2.1	2.9	4		4.2	
t_{PZH}	$\overline{OE}$	Q	1.5	2.8	4.5		5.4	ns
t_{PZL}			1.5	2.8	4.4		5	
t_{PHZ}	$\overline{OE}$	Q	2.4	3.5	5		5.4	ns
t_{PLZ}			2	3.2	4.6		4.8	
$t_{sk(LH)}$					0.5			ns
$t_{sk(HL)}$					0.5			

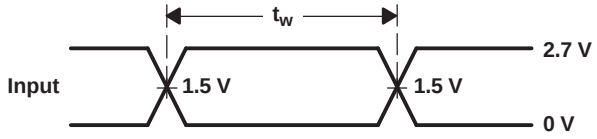
(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

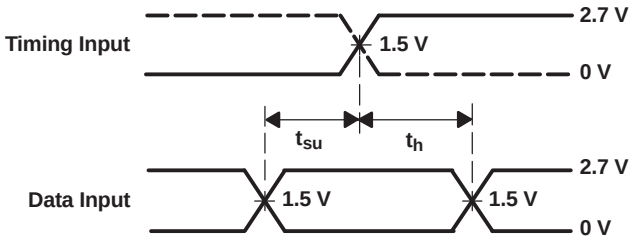


LOAD CIRCUIT

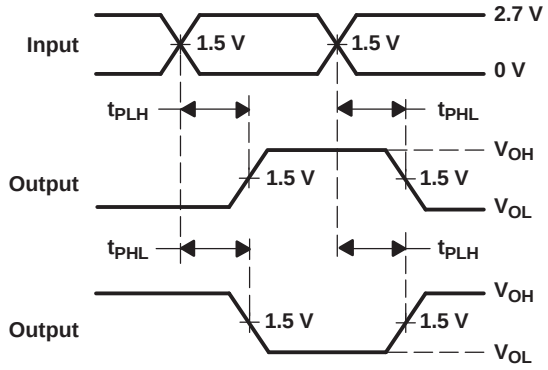
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



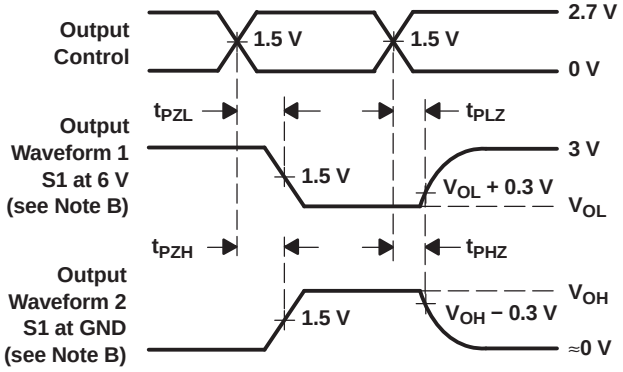
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVTH32374GKER	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	HV374	
SN74LVTH32374ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	HV374	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

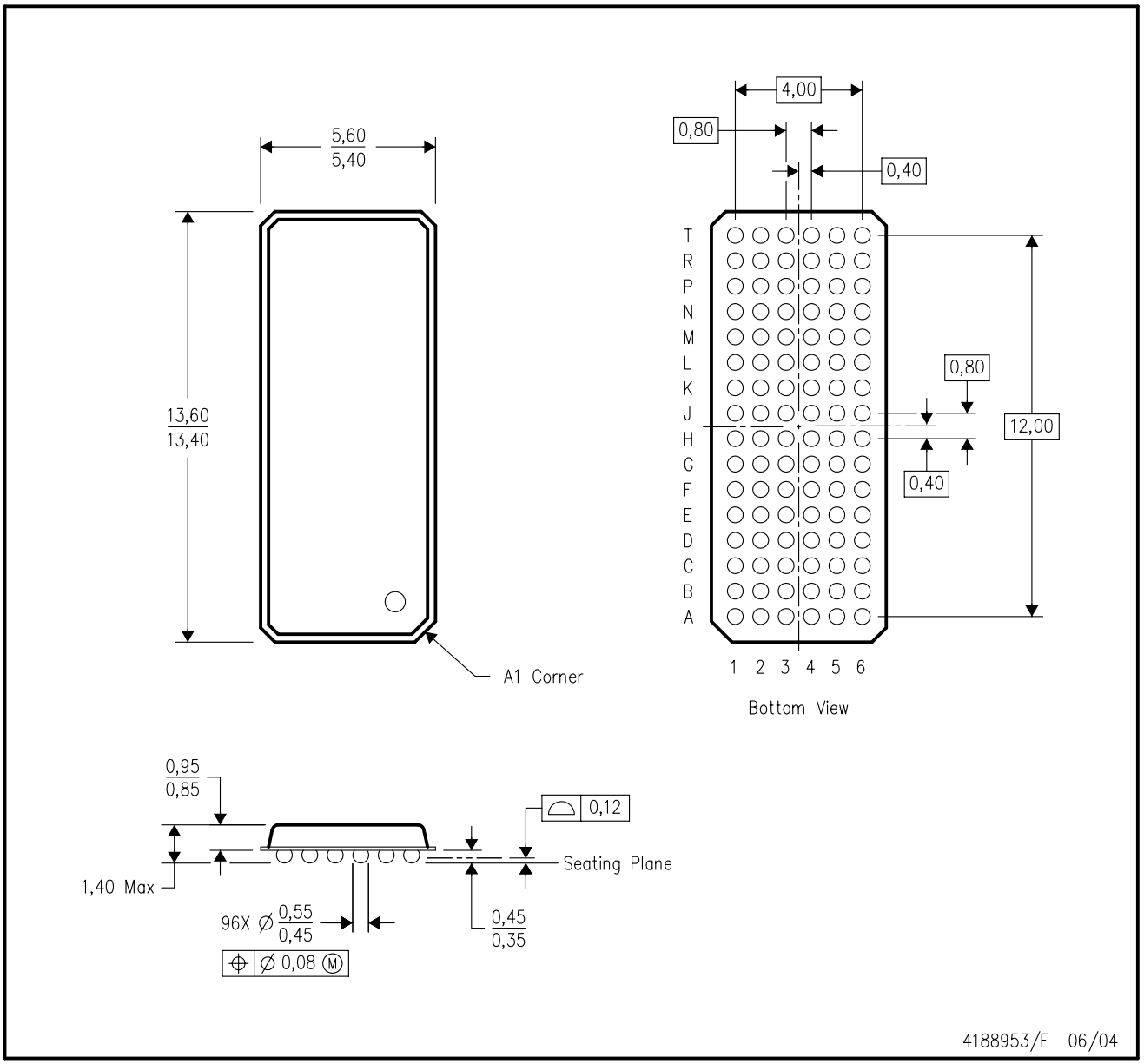
OTHER QUALIFIED VERSIONS OF SN74LVTH32374 :

- Enhanced Product: SN74LVTH32374-EP

NOTE: Qualified Version Definitions:

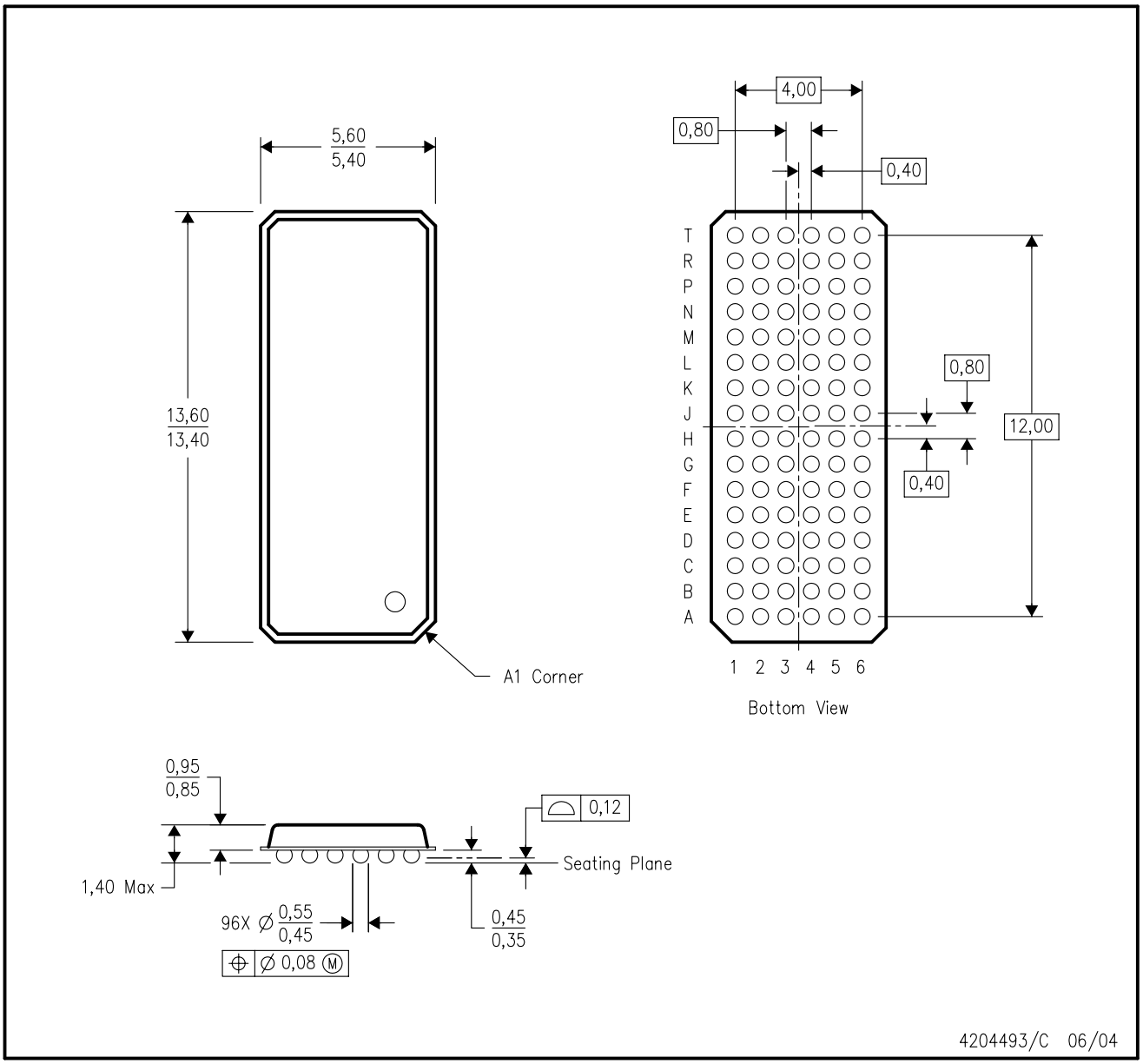
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).

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