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# REMOTE ACCESS IDENTIFICATION DEVICE WITH INTEGRATED 3D WAKEUP RECEIVER AND IMMOBILIZER INTERFACE

Check for Samples: TMS37126

### **FEATURES**

- Low-Frequency (LF) Immobilizer Interface
  - Integrated Batteryless Immobilizer Interface
  - Half Duplex (HDX) Immobilizer
     Communication Achieves up to 4 inch (10 cm) Read Range
  - Special Selective Addressing Mode Allows Reliable Learn-In Sequence
  - 80-Bit Authentication Key Length
  - 80-Bit DST80 Security Authentication Coprocessor
  - Up to 8-kbit/s Uplink Data Rate
  - 5-/3-Byte Challenge/Response Algorithm
  - Fast Authentication Within 42 ms
  - Fast Mutual Authentication Within 65 ms
  - 133-Byte EEPROM
    - 91-Byte Available EEPROM User Memory
    - 32-Bit Unique Serial Number
    - High EEPROM Security and Flexibility
    - Write-Only Authentication Keys
    - Pages Are Irreversibly Lockable and Protectable
    - Protected Pages Programmable Only Through Mutual Authentication
  - Battery Check and Charge Functions
  - Each User Page is Lockable
  - Resonant Frequency: 134.2 kHz
  - Integrated Resonant Frequency Trimming

- Low-Frequency 3D Wakeup Receiver
  - Highest Communication Range of More Than Three Meters
    - High Input Sensitivity: 3.7 mV<sub>pp</sub> (Typ)
    - High Q System
  - Integrated Resonant Circuit Trimming Compensates for Component Offsets
  - Received Signal Strength Indicator (RSSI)
     Output for Each Channel
  - Resonant Circuit Usable as Clock
     Reference for Microcontroller (134.2 kHz)
  - Frequency Range: 120 kHz to 140 kHz
  - Ultra-Low Standby Current: 3.8 μA (Typ)
  - Interface to up to Three External Antennas
  - Two Different Programmable Wake Patterns
  - Selectable Wake Pattern Length:
     0, 4, 8 or 16 Bits
  - Two Separate Adjustable Wake-Up Levels
  - Digital Channel Sensitivity Adjustment for Each Antenna

#### DESCRIPTION

The TMS37126 Remote Access Identification Device (RAID) IC combines two functions in one device:

- 3D wakeup receiver
- DST80 immobilizer interface

The RAID has an SPI interface to connect it to an external microcontroller. RAID is ideally suited for passive entry applications. The 3D low-frequency (LF) wakeup receiver offers high sensitivity to receive LF signals between 120 kHz and 140 kHz and has several other features such as received signal strength indicator (RSSI) measurement and bidirectional LF signaling.



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The embedded DST80 immobilizer interface offers a high level of security through its hardware encryption coprocessor and can also handle mutual authentication schemes. It operates without a battery and can be accessed in terms of its memory and encryption through the SPI interface. Power management features include battery charge and check as well as a battery backup function, which allows operation of all functions with low or even no battery as long as there is sufficient energy from the LF field.

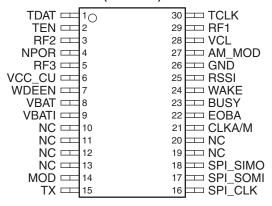
The Passive Entry (PE) device manages the immobilizer communication and LF wake reception. The special high-Q design achieves communication ranges up to 3 m for the PE link with outstanding low standby current on the receiver side. The front end offers flexible configuration of two different wake patterns of 0, 4, 8 or 16 bit length. Each channel can be adjusted in sensitivity and resonance frequency, which results in reproducible system designs. Security keys and rolling codes can be stored in the integrated EEPROM memory. This memory is accessible over the LF interface without support from the battery in the key fob and over the SPI interface. The PE device offers a special battery backup mode to operate the microcontroller without battery support. The external resonant circuit with an LF coil and a resonant capacitor can be trimmed to the correct resonant frequency with the integrated trimming capability, eliminating part tolerances.

## Ordering Information (1)

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER			
-40°C to 85°C	TSSOP - DBT	TMS37126D3XDBTRG4			

- For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI
  web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## DBT PACKAGE (TOP VIEW)





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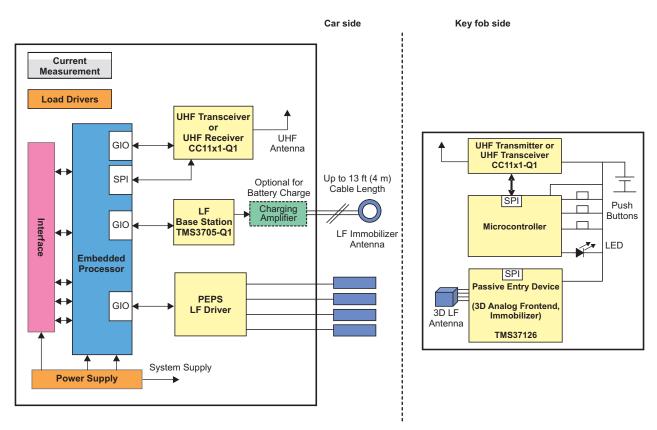


Figure 1. Application Diagram

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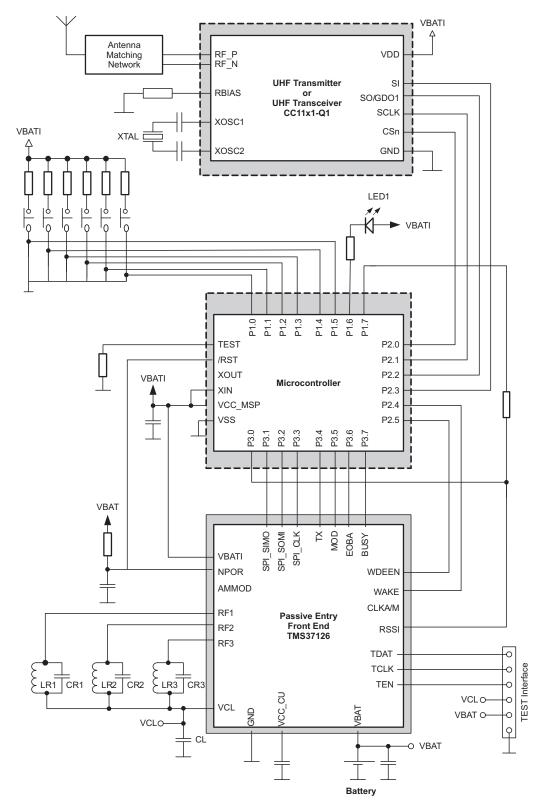


Figure 2. Application Schematic



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## **Operating Characteristics**

Part Number	TMS37126D3XD	DBTRG4					
Features	Immobilizer plus microcontroller with integrated power management						
DST80 authentication logic	80-bit key length, 5-byte challenge, 3-byte signature						
DST80 authentication time	Mutual authentication: 65 ms Fast authentication: 42 ms						
Supply voltage (VBAT)	1.8 V to 3.6 V	1.8 V to 3.6 V					
Standby current consumption	3.8 μA (typ) (thre	ee LF channels active)					
Transponder	,						
Transmission principle	HDX (half duple)	k telegram protocol)					
Operating frequency	134.2 kHz Integrated reson	ant frequency trimming capability via LF or Test interface					
Security	Challenge/respo	nse, mutual authentication					
Downlink	100% AM, PPM bit coding with 2 kbit/s (typ)						
Uplink	FSK modulation with 7.9 kbit/s (typ)						
EEDDOM moment	422 h. da a	91-byte free available EEPROM user memory					
EEPROM memory	133 bytes	32-bit unique serial number					
EEPROM endurance	200 000 cycles (min) (T <sub>A</sub> = 25°C)						
Clock reference for microcontroller	Resonant circuit can be used as clock reference for the microcontroller						
Battery check	Two free programmable voltage levels: 2.0 V to 3.6 V with 0.1-V steps						
Battery charge	Integrated battery charge functionality						
Key learn-in	Special selective	addressing to provide secure learn-in procedure					
3D Wakeup Receiver							
Sensitivity	3.7 mV <sub>pp</sub> (typ)						
Sensitivity tuning	Separate for each channel and each wake pattern						
Operating frequency	120 kHz to 140 kHz						
Resonant frequency trimming	Separate for each channel						
Wake pattern	Two independent wake pattern with selectable length: 0, 4, 8 or 16 Bit						
Operating temperature	-40°C to 85°C						
Package	30-pin TSSOP (DBT)						



## PACKAGE OPTION ADDENDUM

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#### PACKAGING INFORMATION

Orderable Device	Status	Package Type Package P				Eco Plan Lead/Ball Finish		MSL Peak Temp Op Temp (°C)		Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
TMS37126D3XDBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		37126D3	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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## PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



## \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS37126D3XDBTRG4	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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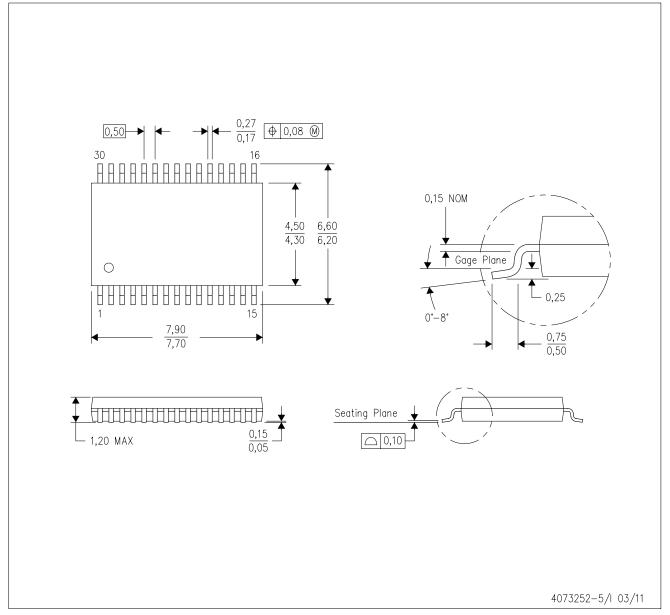


#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TMS37126D3XDBTRG4	TSSOP	DBT	30	2000	367.0	367.0	38.0	

DBT (R-PDSO-G30)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-153.



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