

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **B-Port Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages**

description

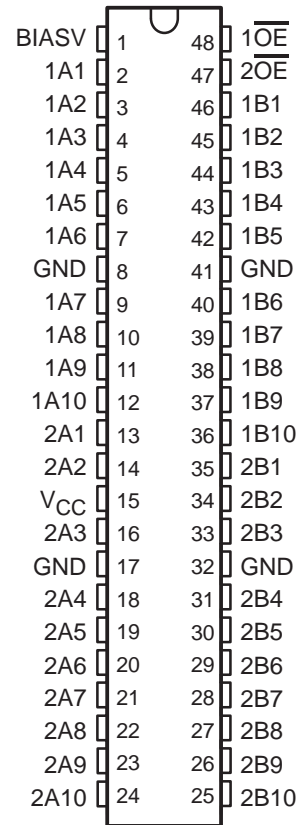
The SN74CBT16800 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, the high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBT16800 is characterized for operation from -40°C to 85°C.

DGG OR DGV PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 10-bit bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



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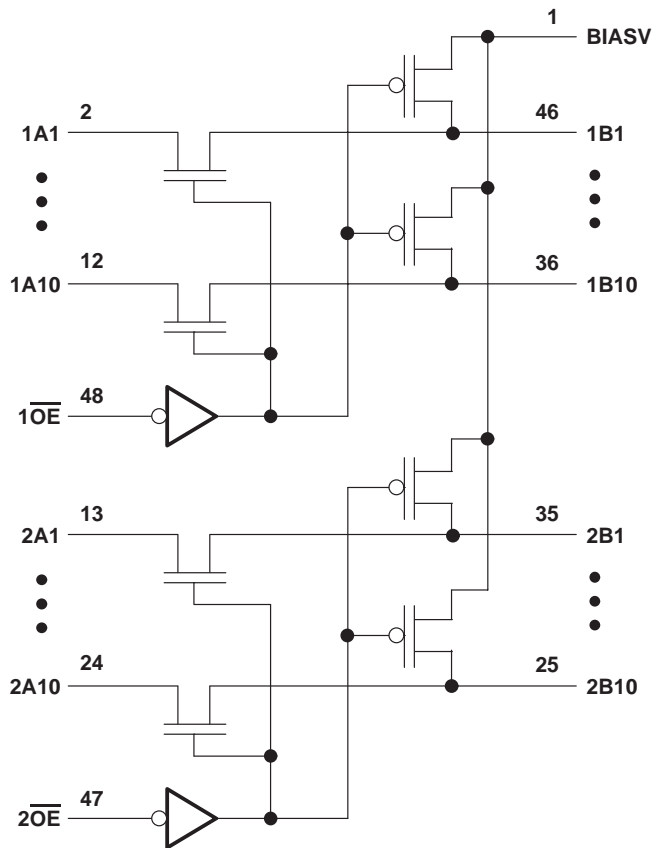
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SN74CBT16800
20-BIT FET BUS SWITCH
WITH PRECHARGED OUTPUTS

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logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Bias voltage range, BIASV	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
	DGV package	93°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V _{CC}	V
V _{IH}	High-level control input voltage	2		V
V _{IL}	Low-level control input voltage		0.8	V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
I _I		V _{CC} = 5.5 V,	V _I = 5.5 V or GND			±5	μA
I _O		V _{CC} = 4.5 V,	BIASV = 2.4 V, V _O = 0	0.25			mA
I _{CC}		V _{CC} = 5.5 V,	I _O = 0, V _I = V _{CC} or GND			50	μA
ΔI _{CC} ‡	Control inputs	V _{CC} = 3.6 V,	One input at 2.7 V, Other inputs at V _{CC} or GND			2.5	mA
C _i	Control inputs	V _I = 3 V or 0					pF
C _{io(OFF)}		V _O = 3 V or 0,	$\overline{OE} = V_{CC}$				pF
r _{on} §		V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA				Ω
		V _{CC} = 4.5 V	V _I = 0, I _I = 64 mA				
			V _I = 0, I _I = 30 mA				
			V _I = 2.4 V, I _I = 15 mA				

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t _{pd} ¶		A or B	B or A					ns
t _{PZH}	BIASV = GND	\overline{OE}	A or B					ns
t _{PZL}	BIASV = 3 V							
t _{PHZ}	BIASV = GND	\overline{OE}	A or B					ns
t _{PLZ}	BIASV = 3 V							

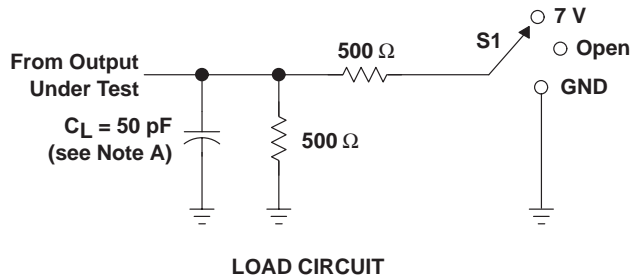
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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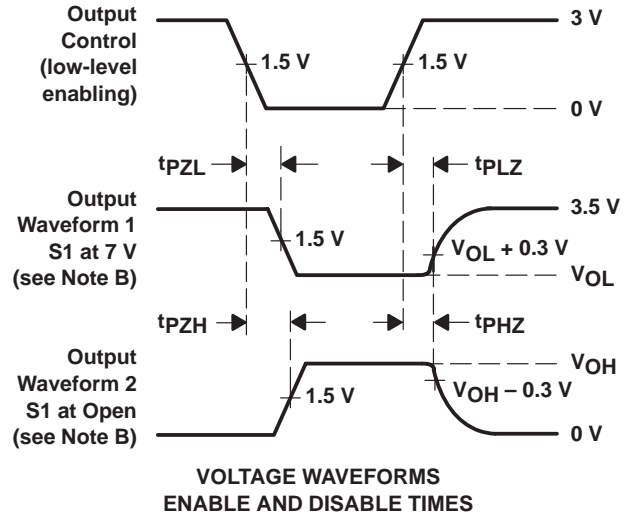
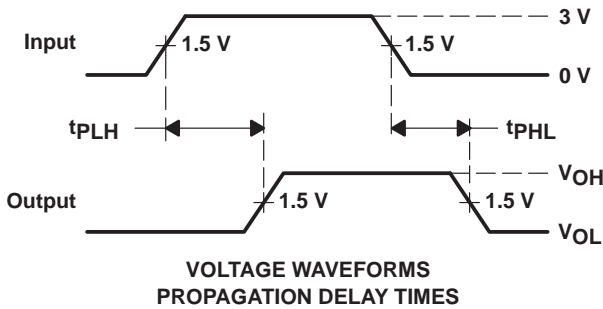
SN74CBT16800
20-BIT FET BUS SWITCH
WITH PRECHARGED OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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