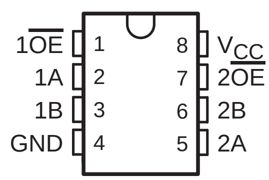
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Integrated Diode to $V_{CC}$ Provides 5-V Input Down To 3.3-V Output Level Shift**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance ($r_{on}$) Characteristics ($r_{on}$ = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **$V_{CC}$ Operating Range From 4.5 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

**D OR PW PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN74CBTD3306C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ($r_{on}$), allowing for minimal propagation delay. This device features an integrated diode in series with $V_{CC}$ to provide level shifting for 5-V input down to 3.3-V output levels. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3306C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBTD3306C is organized as two 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOIC − D | Tube | SN74CBTD3306CD | CC306C |
| | | Tape and reel | SN74CBTD3306CDR | |
| | TSSOP − PW | Tube | SN74CBTD3306CPW | CC306C |
| | | Tape and reel | SN74CBTD3306CPWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## description/ordering information (continued)

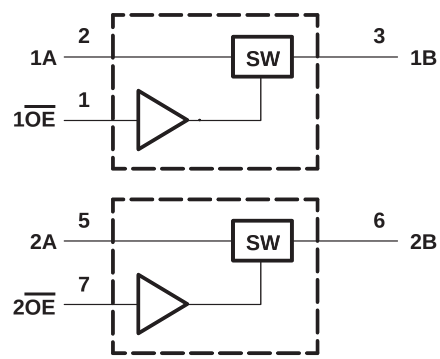
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

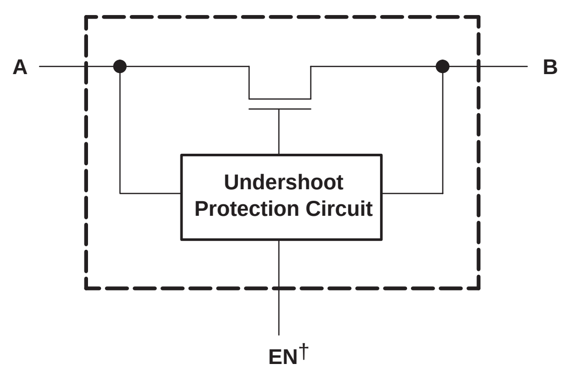
**FUNCTION TABLE**
**(each bus switch)**

| INPUT $\overline{OE}$ | INPUT/OUTPUT A | FUNCTION |
|---|---|---|
| L | B | A port = B port |
| H | Z | Disconnect |

## logic diagram (positive logic)




## simplified schematic, each FET switch (SW)




† EN is the internal enable signal applied to the switch.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . . . . . . −0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2) . . . . . . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . . . . . . −0.5 V to 7 V
Control input clamp current, $I_{IK}$ ($V_{IN} < 0$) . . . . . . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . . . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . . . . . . ±128 mA
Continuous current through $V_{CC}$ or GND terminals . . . . . . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package . . . . . . . . . . 97°C/W
PW package . . . . . . . . . . 149°C/W
Storage temperature range, $T_{stg}$ . . . . . . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
4. $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Notes 6 and 7)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level control input voltage | 2 | 5.5 | V |
| $V_{IL}$ | Low-level control input voltage | 0 | 0.8 | V |
| $V_{I/O}$ | Data input/output voltage | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | −40 | 85 | °C |

NOTES:
6. All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Control inputs | $V_{CC}$ = 4.5 V, | $I_{IN}$ = −18 mA | | | | −1.8 | V |
| $V_{IKU}$ | Data inputs | $V_{CC}$ = 5 V, | 0 mA > $I_I$ ≥ −50 mA, $V_{IN}$ = $V_{CC}$ or GND, | Switch OFF | | | −2 | V |
| $V_{OH}$ | | See Figures 4 and 5 | | | | | | |
| $I_{IN}$ | Control inputs | $V_{CC}$ = 5.5 V, | $V_{IN}$ = $V_{CC}$ or GND | | | | ±1 | µA |
| $I_{OZ}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 to 5.5 V, $V_I$ = 0, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | | ±10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0 | | | 10 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_{I/O}$ = 0, $V_{IN}$ = $V_{CC}$ or GND, | Switch ON or OFF | | | 1.5 | mA |
| $\Delta I_{CC}$§ | Control inputs | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 2.5 | mA |
| $C_{in}$ | Control inputs | $V_{IN}$ = 3 V or 0 | | | | 3.5 | | pF |
| $C_{io(OFF)}$ | | $V_{I/O}$ = 3 V or 0, | Switch OFF, | $V_{IN}$ = $V_{CC}$ or GND | | 5 | | pF |
| $C_{io(ON)}$ | | $V_{I/O}$ = 3 V or 0, | Switch ON, | $V_{IN}$ = $V_{CC}$ or GND | | 12.5 | | pF |
| $r_{on}$¶ | | $V_{CC}$ = 4.5 V | $V_I$ = 0 | $I_O$ = 64 mA | | 3 | 6 | Ω |
| | | | | $I_O$ = 30 mA | | 3 | 6 | |
| | | | $V_I$ = 2.4 V, | $I_O$ = −15 mA | | 9 | 20 | |

$V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
† All typical values are at $V_{CC}$ = 5 V (unless otherwise noted), $T_A$ = 25°C.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified voltage level, rather than $V_{CC}$ or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V ± 0.5 V MIN | $V_{CC}$ = 5 V ± 0.5 V MAX | UNIT |
|---|---|---|---|---|---|
| $t_{pd}$# | A or B | B or A | | 0.15 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 1.5 | 4.7 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1.5 | 4.7 | ns |

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## undershoot characteristics (see Figures 1 and 2)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OUTU}$ | $V_{CC}$ = 5.5 V, Switch OFF, $V_{IN} = V_{CC}$ or GND | 2 | $V_{OH}-0.3$ | | V |

† All typical values are at $V_{CC}$ = 5 V (unless otherwise noted), $T_A$ = 25°C.

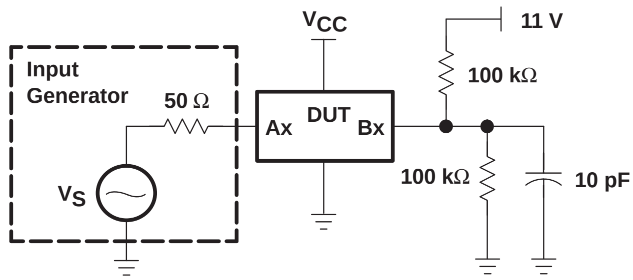



**Figure 1. Device Test Setup**

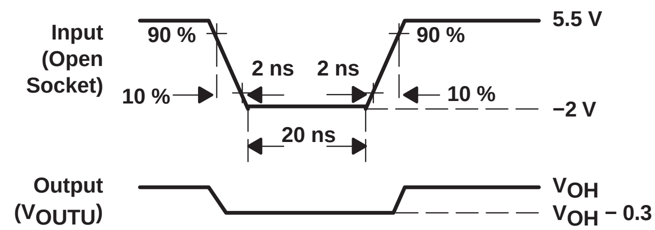
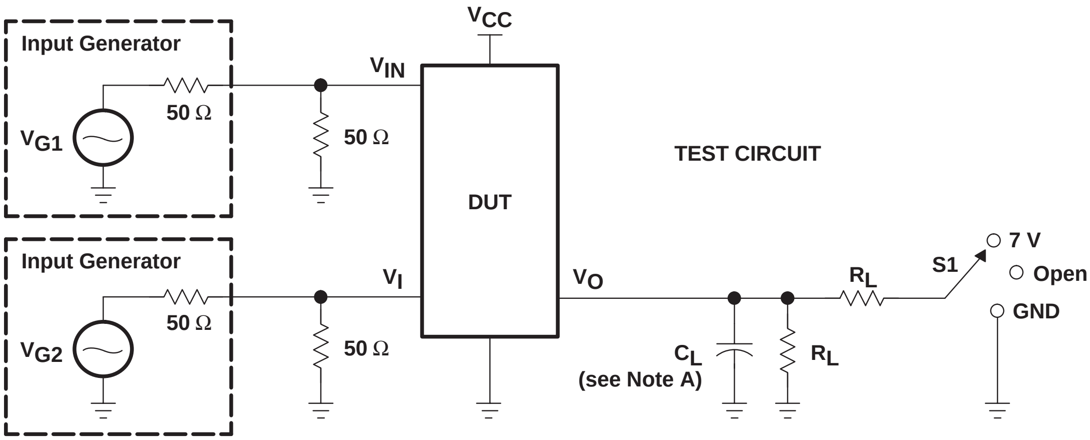
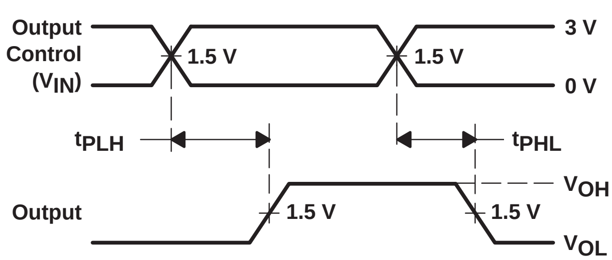



**Figure 2. Transient Input Voltage ($V_I$) and Output Voltage ($V_{OUTU}$) Waveforms (Switch OFF)**

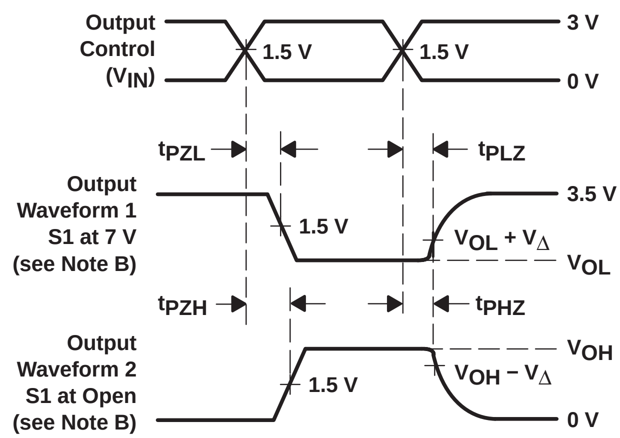
## PARAMETER MEASUREMENT INFORMATION FOR LEVEL SHIFTER




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_I$ | $C_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|
| $t_{pd(s)}$ | 5 V ± 0.5 V | Open | 500 Ω | $V_{CC}$ or GND | 50 pF | |
| $t_{PLZ}/t_{PZL}$ | 5 V ± 0.5 V | 7 V | 500 Ω | GND | 50 pF | 0.3 V |
| $t_{PHZ}/t_{PZH}$ | 5 V ± 0.5 V | Open | 500 Ω | $V_{CC}$ | 50 pF | 0.3 V |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

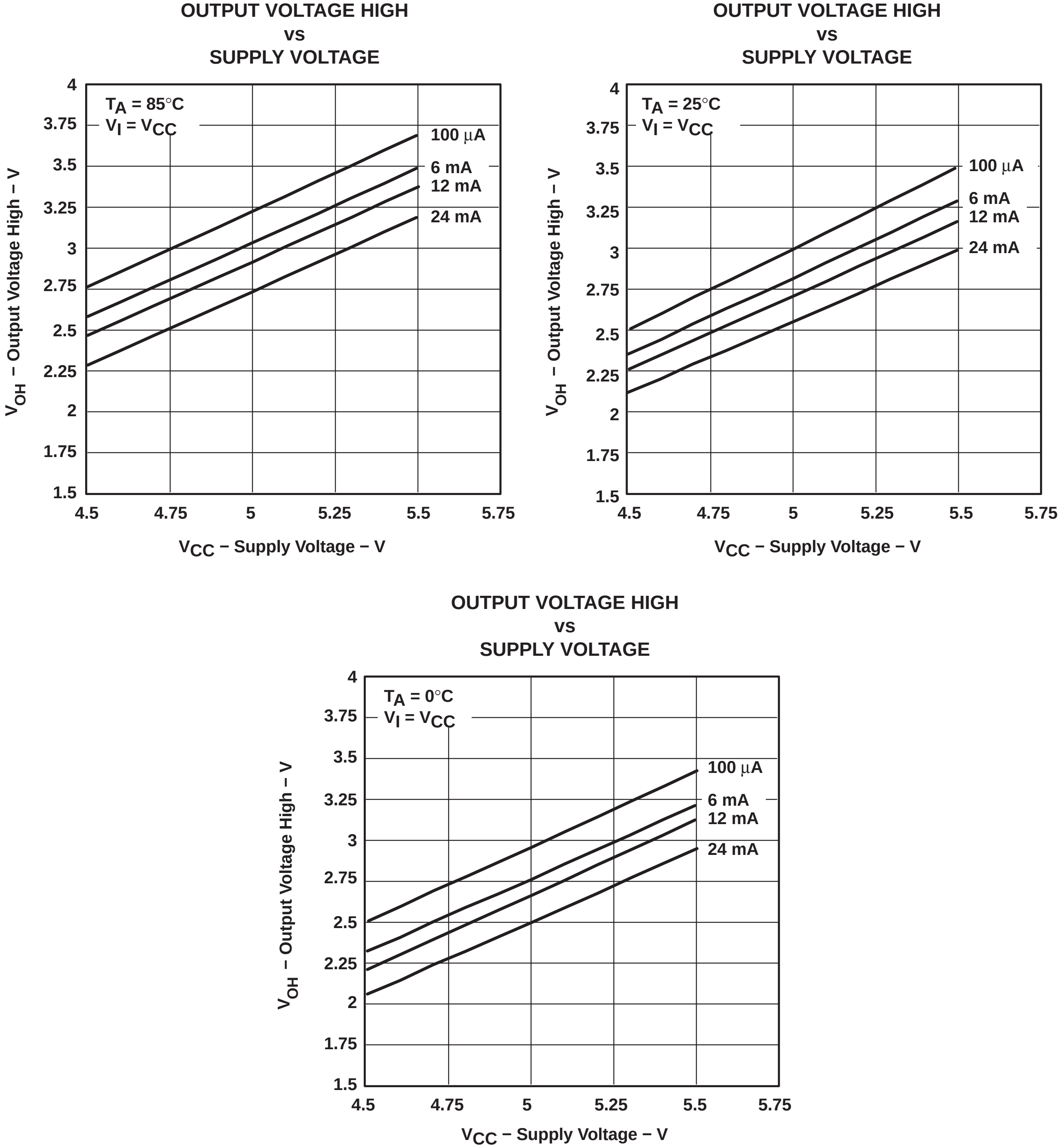



**Figure 4. $V_{OH}$ Values**

## TYPICAL CHARACTERISTICS (continued)

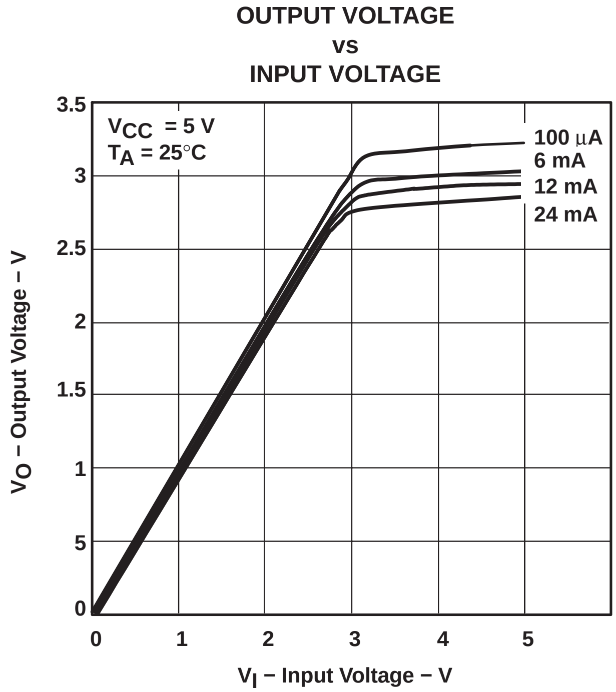



**Figure 5. Data Output Voltage vs Data Input Voltage**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CBTD3306CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CPWE4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CPWRE4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |
| SN74CBTD3306CPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CC306C | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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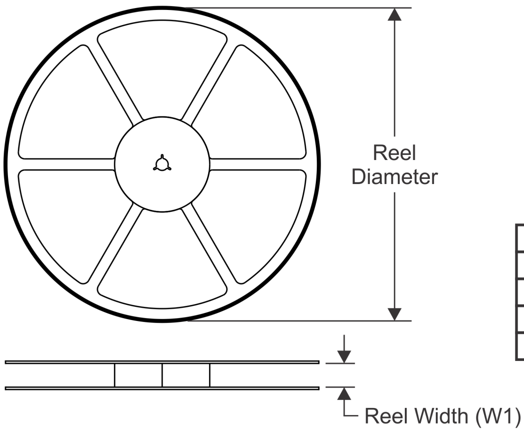
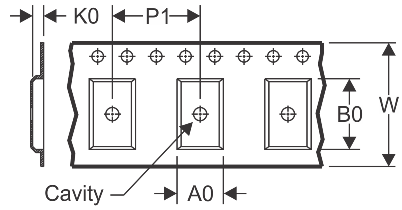
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

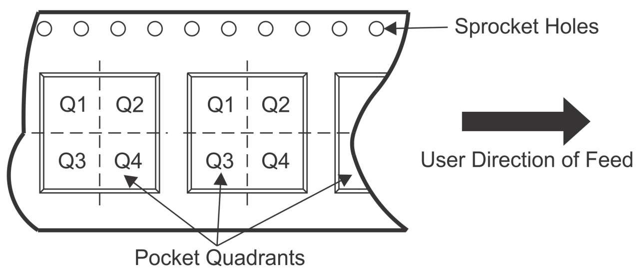



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

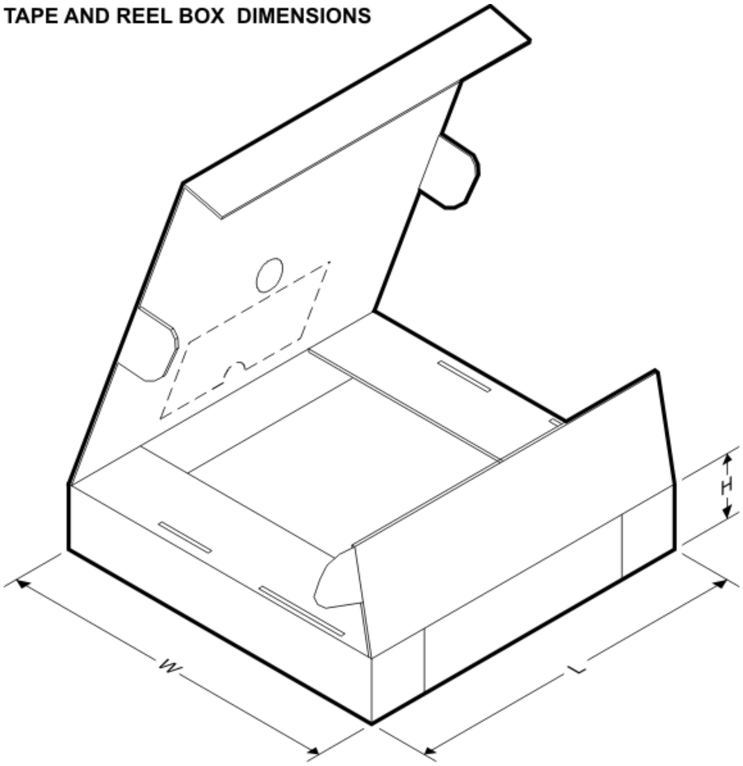
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CBTD3306CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN74CBTD3306CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CBTD3306CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

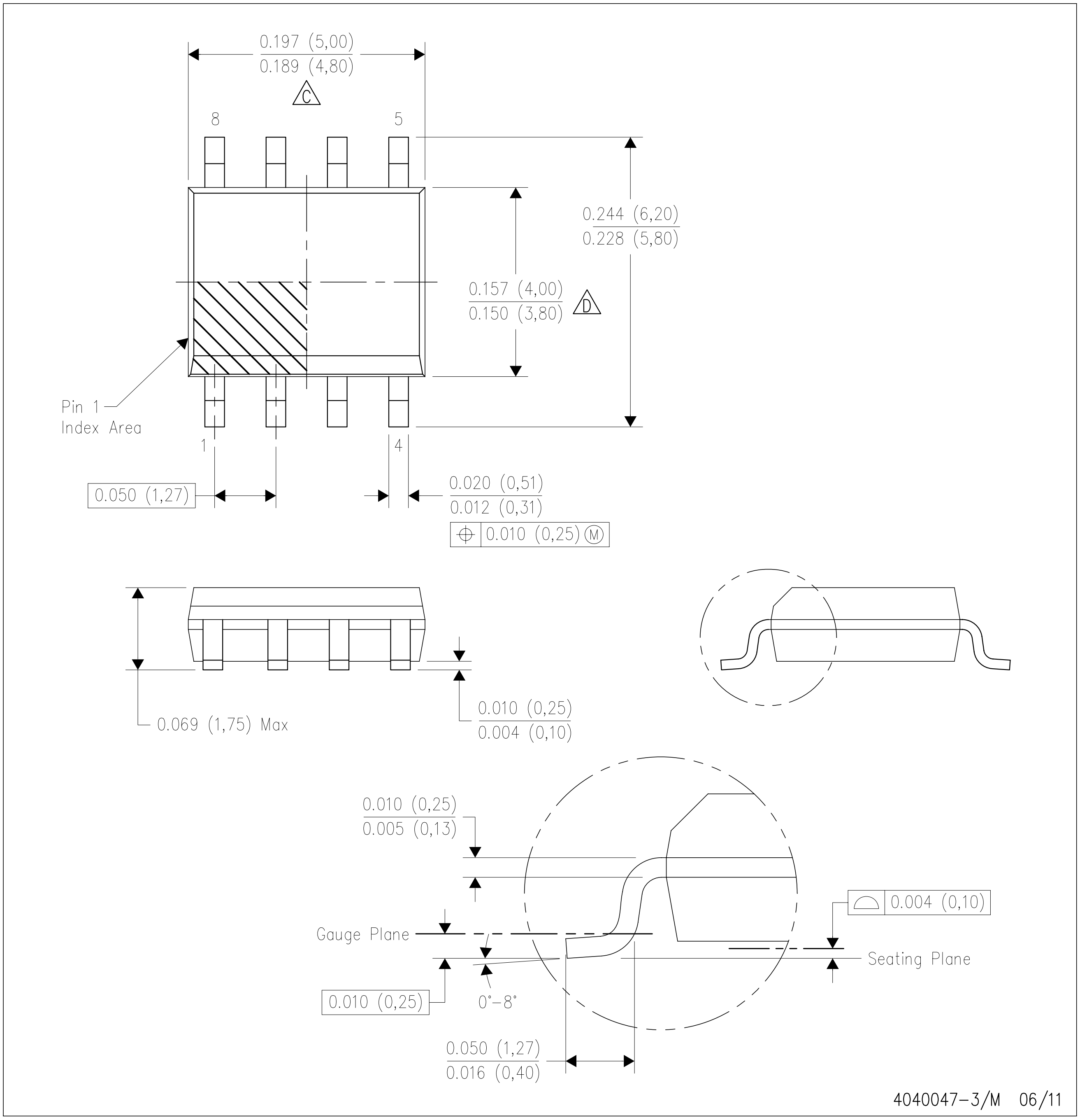
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

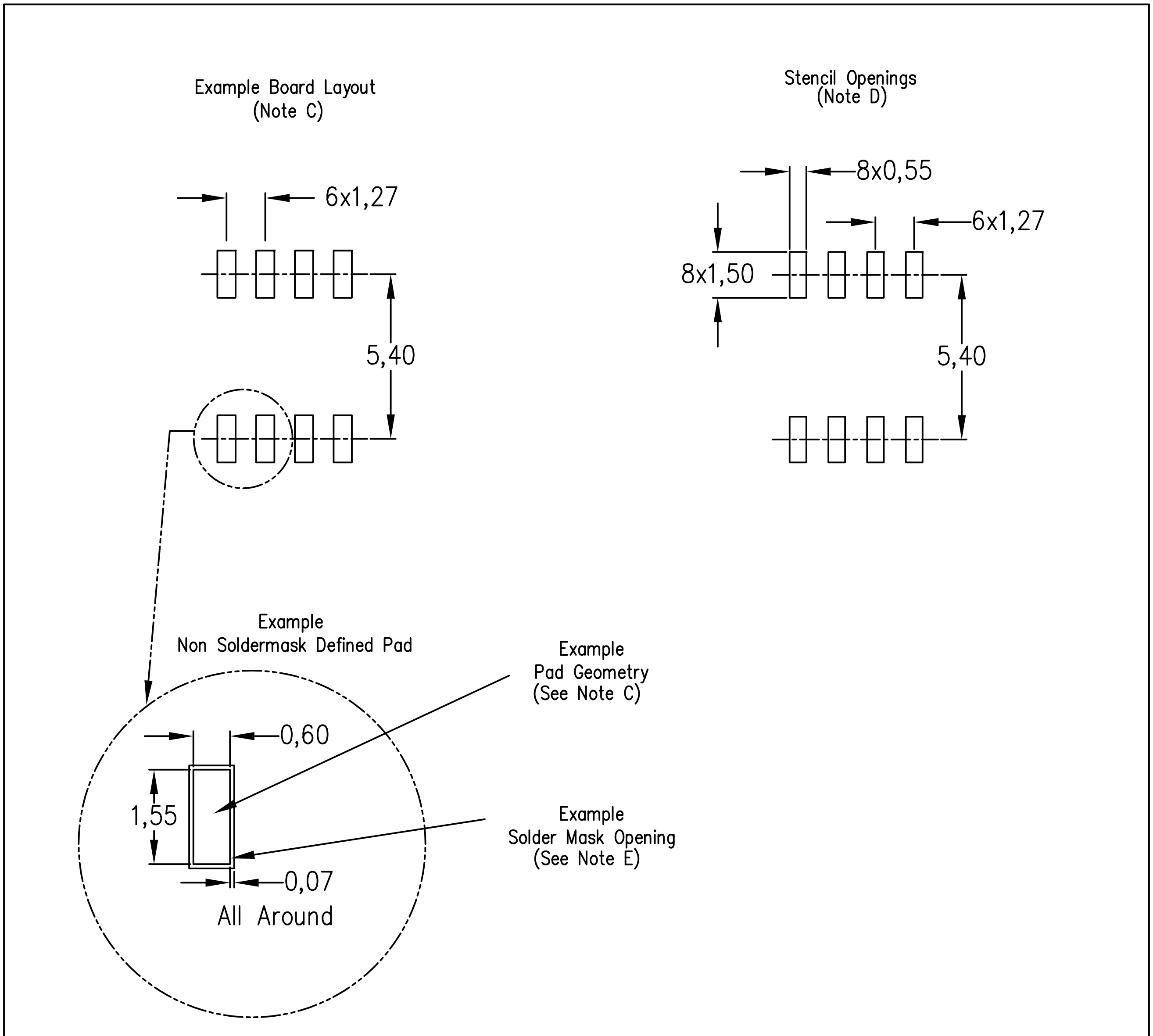
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74CBTD3306CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN74CBTD3306CPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74CBTD3306CPWR | TSSOP | PW | 8 | 2000 | 364.0 | 364.0 | 27.0 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

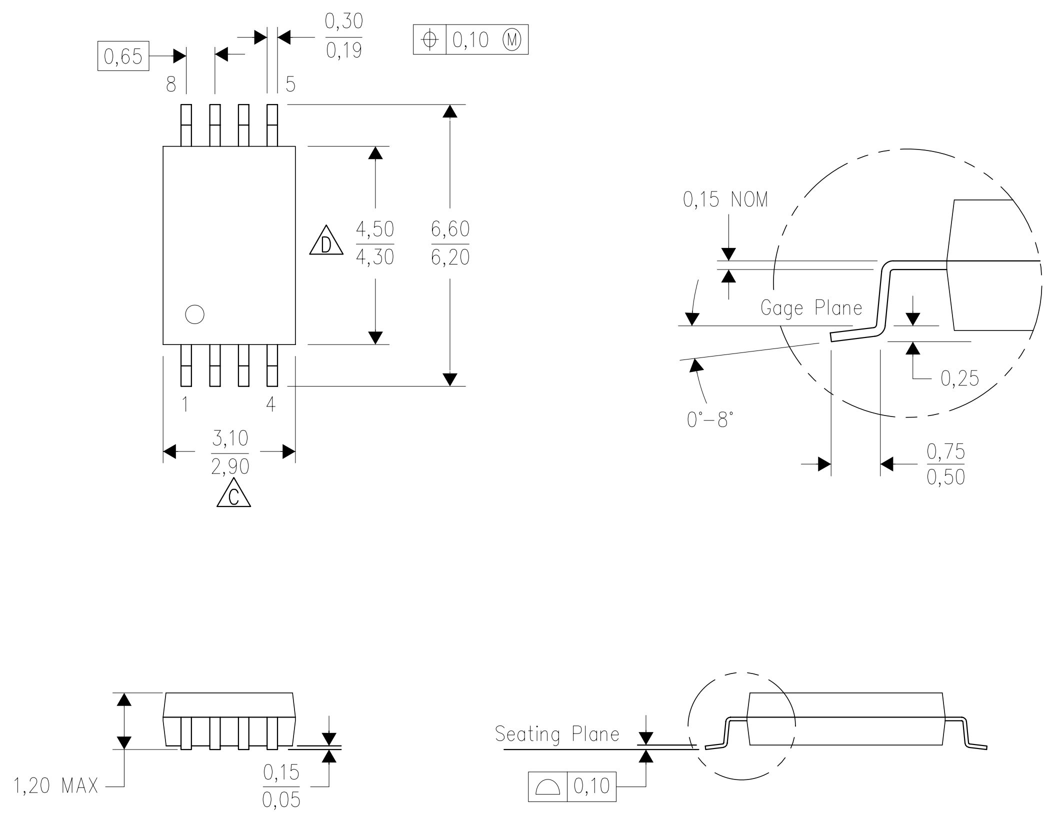
D (R-PDSO-G8) PLASTIC SMALL OUTLINE




4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8) PLASTIC SMALL OUTLINE




4040064-2/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

## IMPORTANT NOTICE



| **Products** | | **Applications** | |
|---|---|---|---|
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