HIGH-SPEED USB 2.0 (480-Mbps) 1-PORT SWITCH
WITH SINGLE ENABLE AND ESD PROTECTION

Check for Samples: TS3USB31E

FEATURES

- **V_{CC} Operation 2.25 V to 4.3 V**
- **1.8-V Compatible Control-Pin Inputs**
- **I_{OFF} Supports Partial Power-Down Mode Operation**
- **r_{on} = 10 Ω Maximum**
- **Δr_{on} <0.35 Ω Typical**
- **$C_{io(ON)}$ = 6 pF Typical**
- **Low Power Consumption (1 µA Maximum)**
- **ESD Performance Tested Per JESD 22**
  - **8000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
  - **250-V Machine Model (A115-A)**
- **ESD Performance COM Port to GND**
  - **15000-V Human-Body Model (A114-B, Class II)**
- **Wide –3-dB Bandwidth = 1100 MHz Typical**
- **Packaged in 8-Pin TQFN (1.5 mm × 1.5 mm)**

APPLICATIONS

- **Routes Signals for USB 1.0, 1.1, and 2.0**

DESCRIPTION/ORDERING INFORMATION

The TS3USB31E is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1100 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

**RSE PACKAGE
(TOP VIEW)**

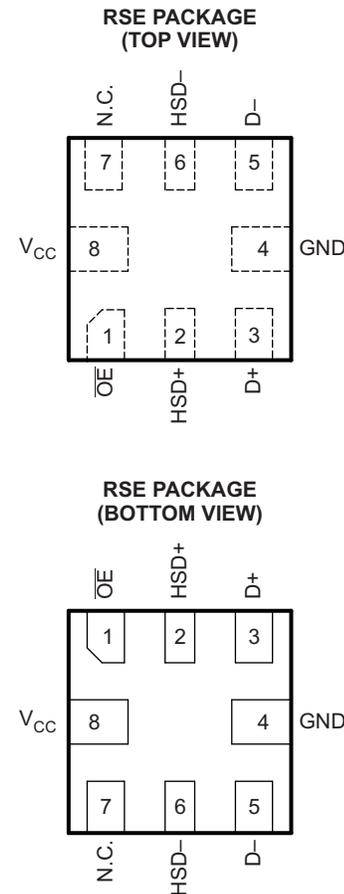**RSE PACKAGE
(BOTTOM VIEW)**

N.C. – No internal connection

Table 1. ORDERING INFORMATION

T_A	PACKAGE [1] [2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RSE	Tape and reel	TS3USB31ERSER	LJ

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

⚠️ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
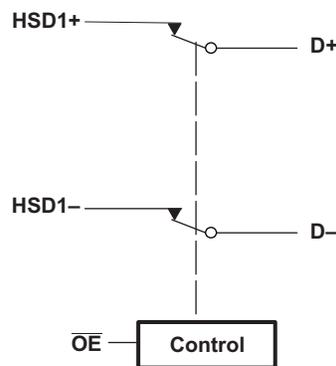
PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{OE}$	Bus-switch enable
D+, D–, HSD+, HSD–	Data ports
NC	No connect

TRUTH TABLE

$\overline{OE}$	FUNCTION
H	Disconnect
L	D+, D– = HSD+, HSD–

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_{IN}	Control input voltage range[2] [3]		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]	HSD+, HSD–	–0.5	V_{CC} + 0.3	V
		D+, D– when $V_{CC} > 0$	–0.5	V_{CC} + 0.3	
		D+, D– when $V_{CC} = 0$		5.25	
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current[5]			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

Product Folder Link(s): *TS3USB31E*

PACKAGE THERMAL IMPEDANCE

			TYP	UNIT
θ_{JA}	Package thermal impedance[1]	RSE package	253	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.25	4.3	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0.9		V
		V_{CC} = 3 V to 3.6 V	1.3		
		V_{CC} = 4.3 V	1.7		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.4	V
		V_{CC} = 3 V to 3.6 V		0.5	
		V_{CC} = 4.3 V		0.7	
$V_{I/O}$	Data input/output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS[1]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [2]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
I_{IN}	Control inputs	V_{CC} = 4.3 V, 0 V,	V_{IN} = 0 to 4.3 V			±1	µA
I_{OZ} [3]		V_{CC} = 4.3 V, V_I = 0,	V_O = 0 to 3.6 V, Switch OFF			±1	µA
I_{OFF}	D+ and D−	V_{CC} = 0 V, V_I = 0,	V_O = 0 to 4.3 V, V_{IN} = V_{CC} or GND			±2	µA
I_{CC}		V_{CC} = 4.3 V,	$I_{I/O}$ = 0, Switch ON or OFF			1	µA
ΔI_{CC} [4]	Control inputs	V_{CC} = 4.3 V,	V_{IN} = 2.6 V			10	µA
C_{in}	Control inputs	V_{CC} = 0 V,	V_{IN} = V_{CC} or GND		1		pF
$C_{io(OFF)}$		V_{CC} = 2.5 V,	$V_{I/O}$ = 2.5 V or 0, Switch OFF		2		pF
		V_{CC} = 3.3 V,	$V_{I/O}$ = 3.3 V or 0, Switch OFF		2		
$C_{io(ON)}$		V_{CC} = 2.5 V,	$V_{I/O}$ = 2.5 V or 0, Switch ON		6		pF
		V_{CC} = 3.3 V,	$V_{I/O}$ = 3.3 V or 0, Switch ON		6		
r_{on} [5]		V_{CC} = 2.5 V,	V_I = 0.4, I_O = −8 mA		7.5	9	Ω
		V_{CC} = 3 V,	V_I = 0.4, I_O = −8 mA		6.5	10	
Δr_{on}		V_{CC} = 2.5 V,	V_I = 0.4, I_O = −8 mA		0.4		Ω
		V_{CC} = 3 V,	V_I = 0.4, I_O = −8 mA		0.35		
$r_{on(flat)}$		V_{CC} = 2.5 V,	V_I = 0 V or 1 V, I_O = −8 mA		0.07		Ω
		V_{CC} = 3 V,	V_I = 0 V or 1 V, I_O = −8 mA		2		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

TS3USB31E

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP [1]	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 240 MHz, See Figure 9	-53	dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 240 MHz, See Figure 8	-30	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See Figure 10	1100	MHz

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP [1]	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 240 MHz, See Figure 9	−53	dB
O_{IRR}	OFF isolation	R_L = 50 Ω, f = 240 MHz, See Figure 8	−30	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See Figure 10	1100	MHz

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

SWITCHING CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
t_{pd}	Propagation delay[2] [3]	R_L = 50 Ω, C_L = 5 pF, See Figure 11		0.25		ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 7			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 7			25	ns
$t_{SK(O)}$	Output skew between center port to any other port[2]	R_L = 50 Ω, C_L = 5 pF, See Figure 12		50		ps
$t_{SK(P)}$	Skew between opposite transitions of the same output $(t_{PHL} - t_{PLH})$[2]	R_L = 50 Ω, C_L = 5 pF, See Figure 12		20		ps
t_J	Total jitter[2]	R_L = 50 Ω, C_L = 5 pF, $t_R = t_F$ = 500 ps at 480 Mbps		200		ps

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

Product Folder Link(s): TS3USB31E

SWITCHING CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
t_{pd}	Propagation delay [2] [3]	R_L = 50 Ω, C_L = 5 pF, See Figure 11		0.25		ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 7			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 7			25	ns
$t_{SK(O)}$	Output skew between center port to any other port [2]	R_L = 50 Ω, C_L = 5 pF, See Figure 12		50		ps
$t_{SK(P)}$	Skew between opposite transitions of the same output $(t_{PHL} - t_{PLH})$ [2]	R_L = 50 Ω, C_L = 5 pF, See Figure 12		20		ps
t_J	Total jitter [2]	R_L = 50 Ω, C_L = 5 pF, $t_R = t_F$ = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)		200		ps

(1)   For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2)   Specified by design
(3)   The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

TS3USB31E

APPLICATION INFORMATION
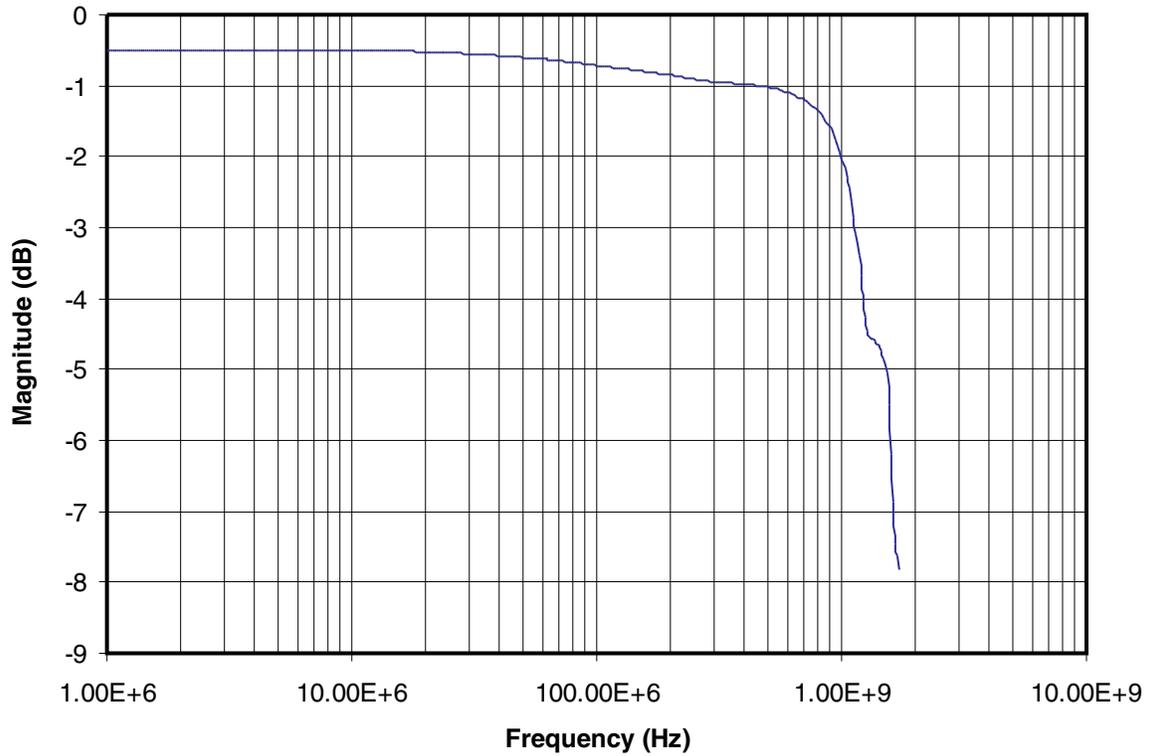
Figure 1. Insertion Loss

Figure 2. OFF Isolation

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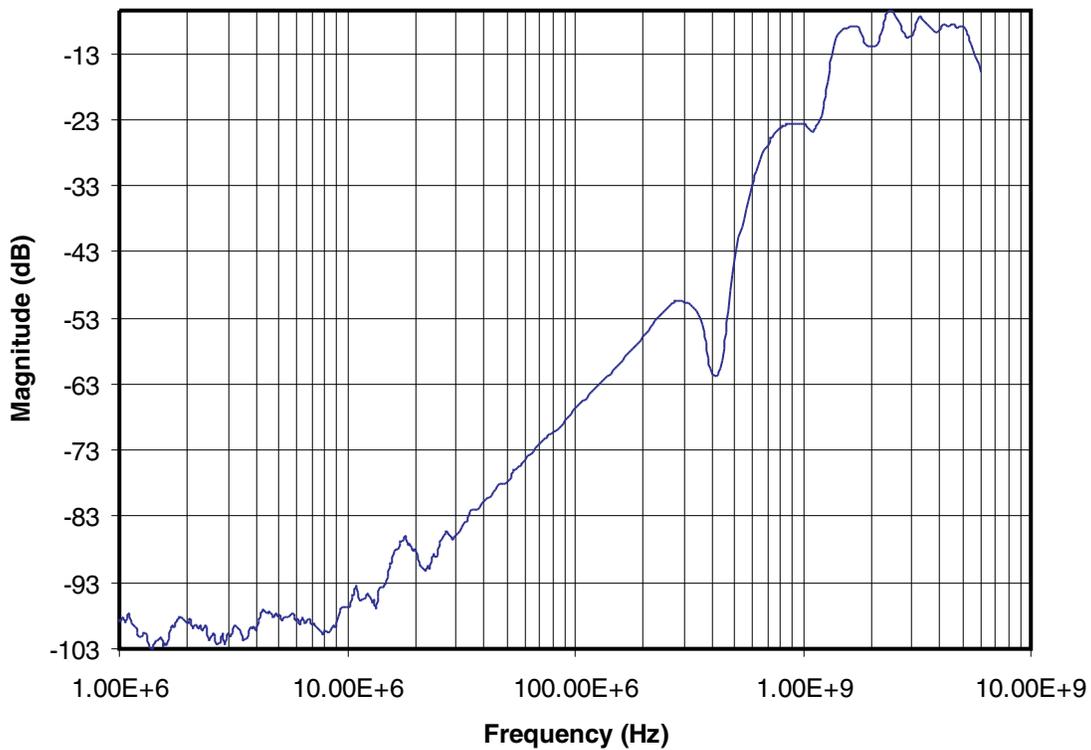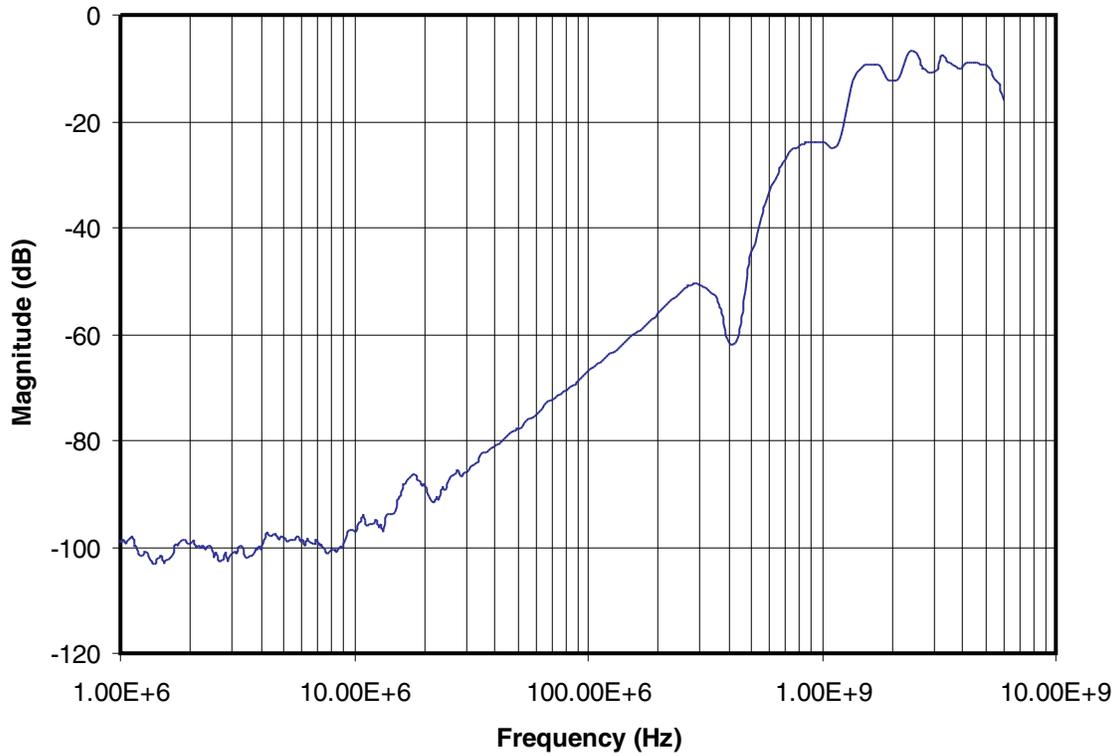
Figure 3. Crosstalk
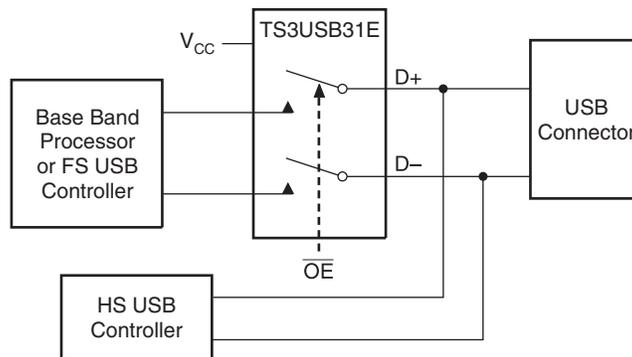
Figure 4. Application Diagram
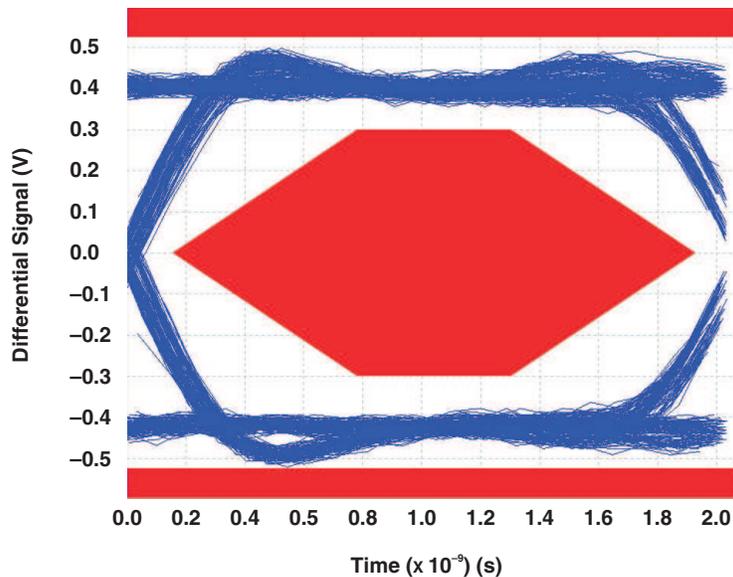
Figure 5. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

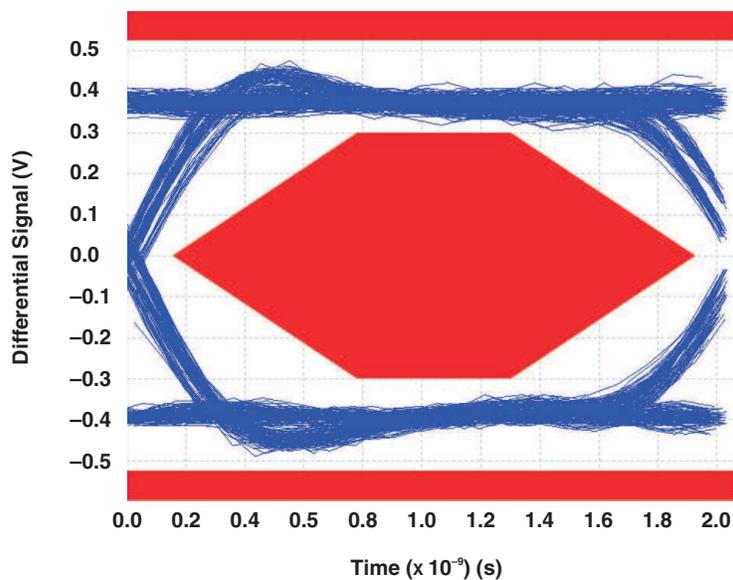**Figure 6. Eye Pattern: 480-Mbps USB Signal With Switch NO Path**

PARAMETER MEASUREMENT INFORMATION

TEST	R_L	C_L	V_{IN}
t_{ON}	50 Ω	5 pF	V_{CC}
t_{OFF}	50 Ω	5 pF	V_{CC}
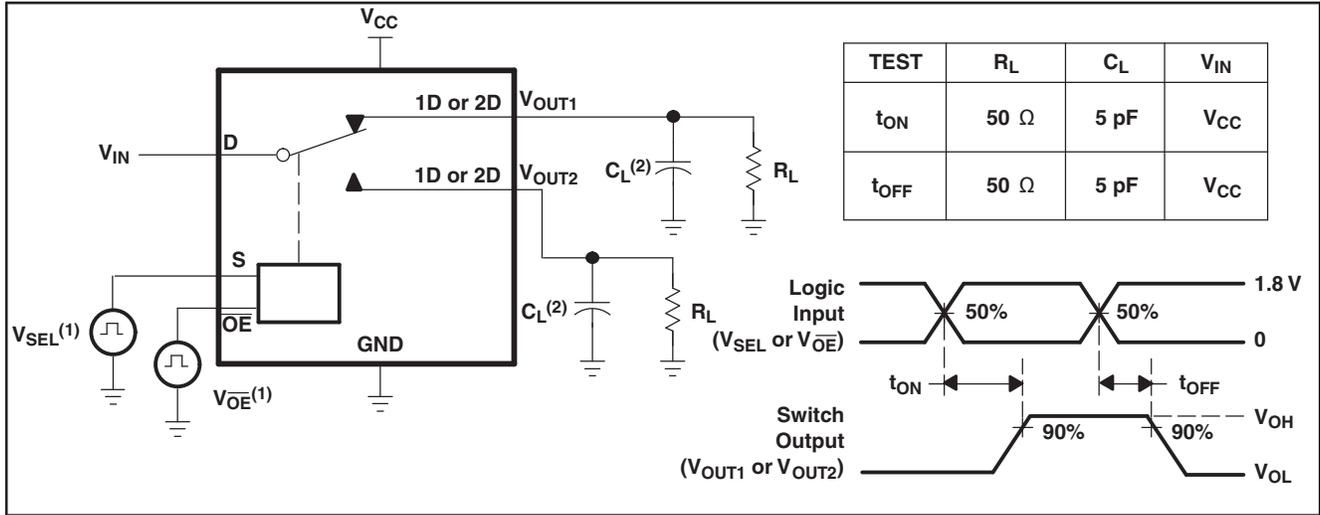
(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 7. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})
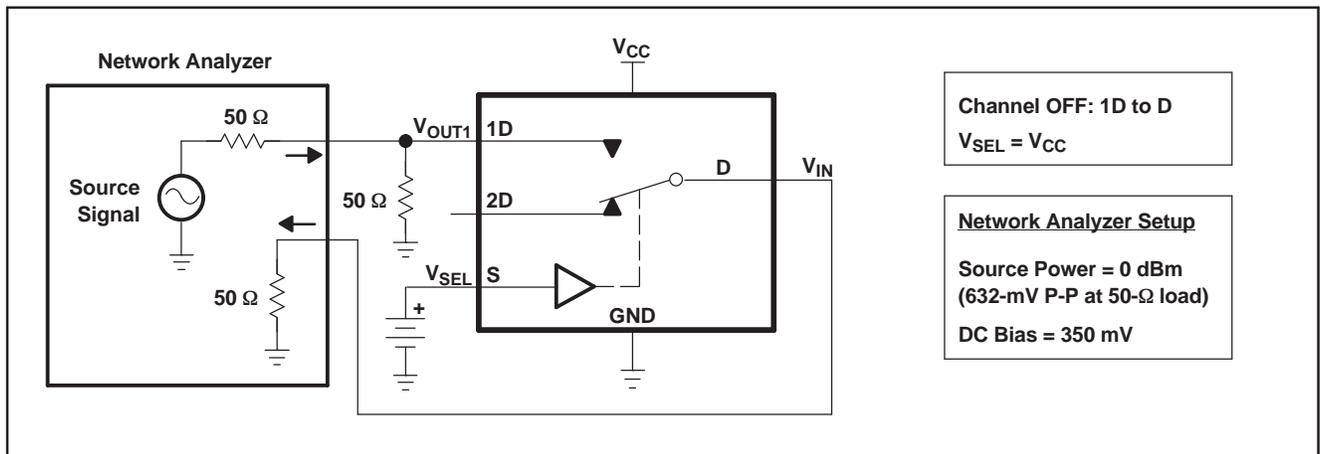
Figure 8. OFF Isolation (O_{IRR})

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TS3USB31E

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION (continued)
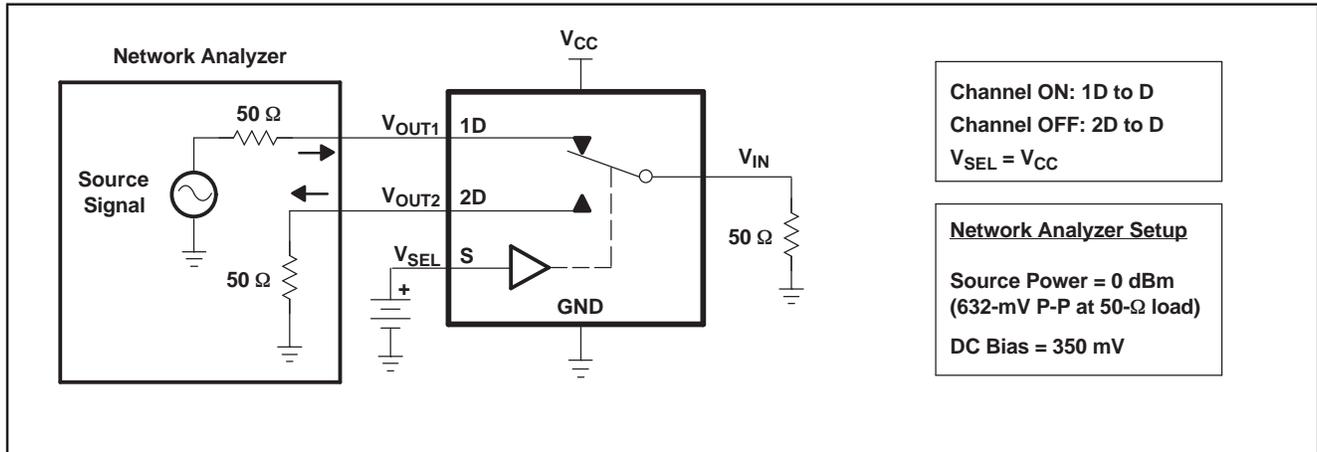
Figure 9. Crosstalk (X$_{TALK}$)
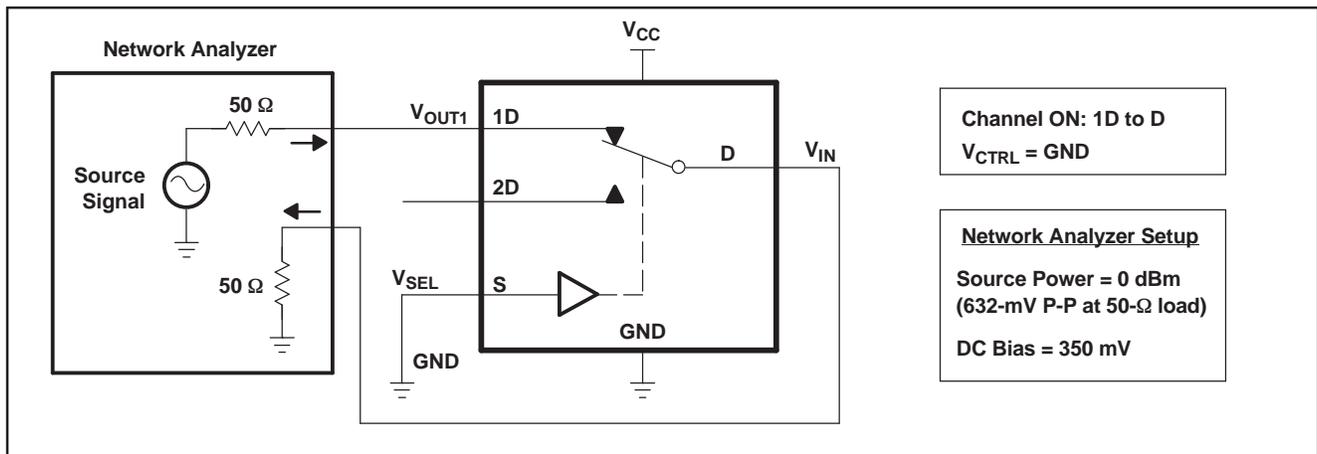
Figure 10. Bandwidth (BW)
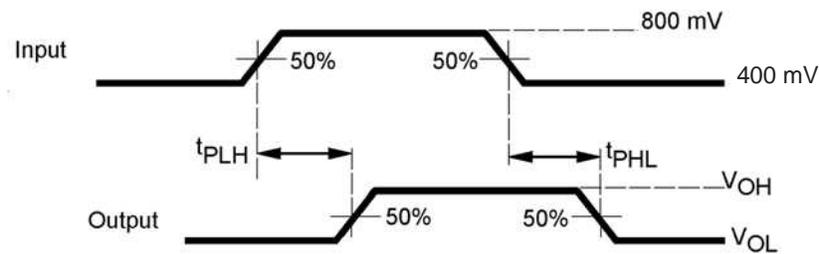
Figure 11. Propagation Delay

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PARAMETER MEASUREMENT INFORMATION (continued)

$$t_{SK(P)} = | t_{PHL} - t_{PLH} |$$

Pulse Skew $t_{SK(P)}$

$$t_{SK(O)} = |t_{PLH1} - t_{PLH2}| \text{ or } | t_{PHL1} - t_{PHL2} |$$
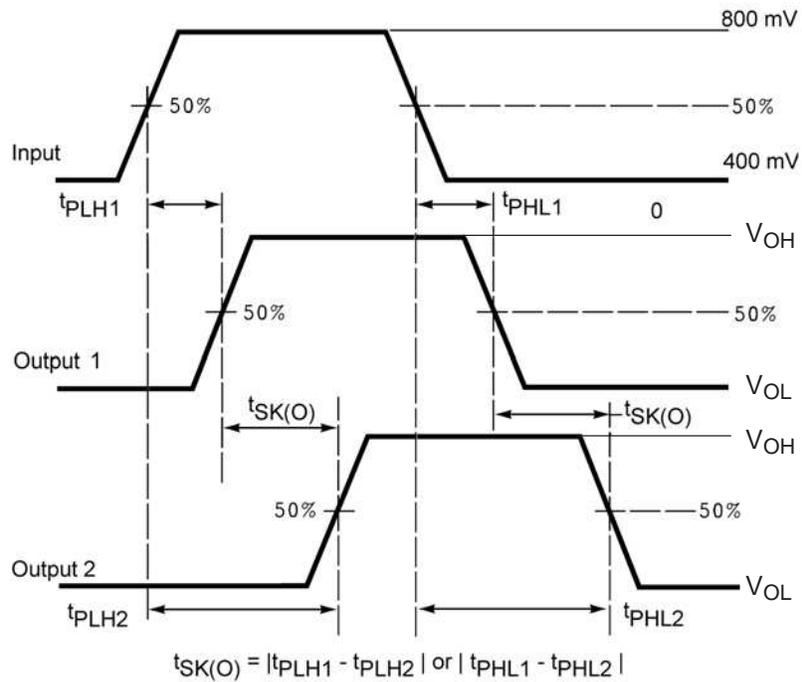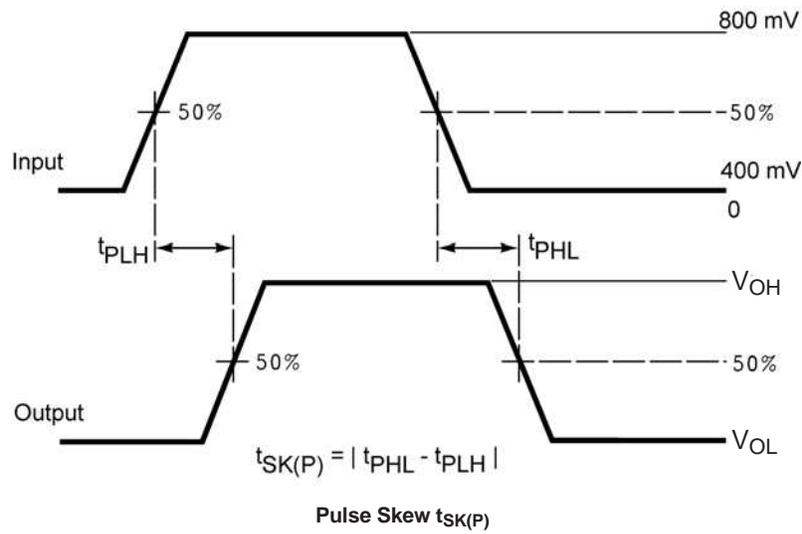
Output Skew $t_{SK(P)}$

Figure 12. Skew Test

Product Folder Link(s): TS3USB31E

PARAMETER MEASUREMENT INFORMATION (continued)

$$r_{on} = \frac{V_{IN} - V_{OUT2} \text{ or } V_{OUT1}}{I_{IN}} \, \Omega$$

Channel ON

$V_{SEL} = V_{IH}$ or V_{IL}
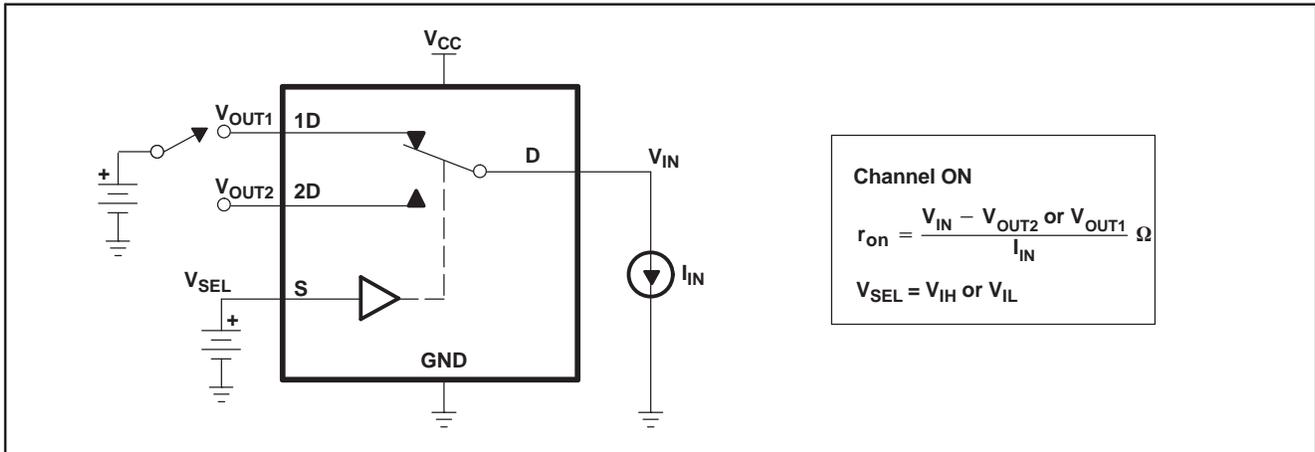
Figure 13. ON-State Resistance (r_{on})

OFF-State Leakage Current
Channel OFF
$V_{SEL} = V_{IH}$ or V_{IL}
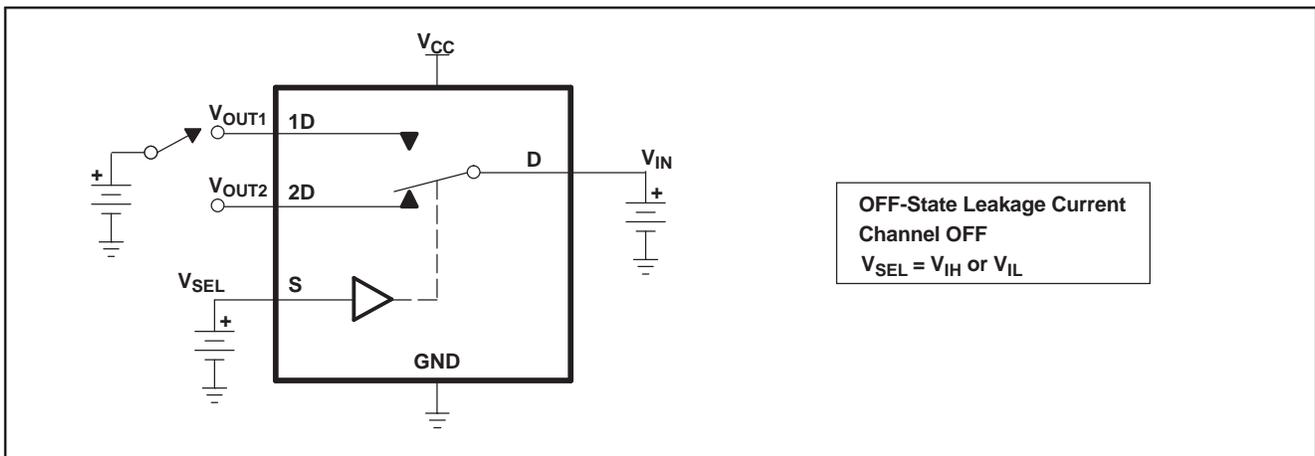
Figure 14. OFF-State Leakage Current

$V_{BIAS} = V_{CC}$ or GND

$V_{SEL} = V_{CC}$ or GND

Capacitance is measured at 1D, 2D, D, and S inputs during ON and OFF conditions.

Figure 15. Capacitance
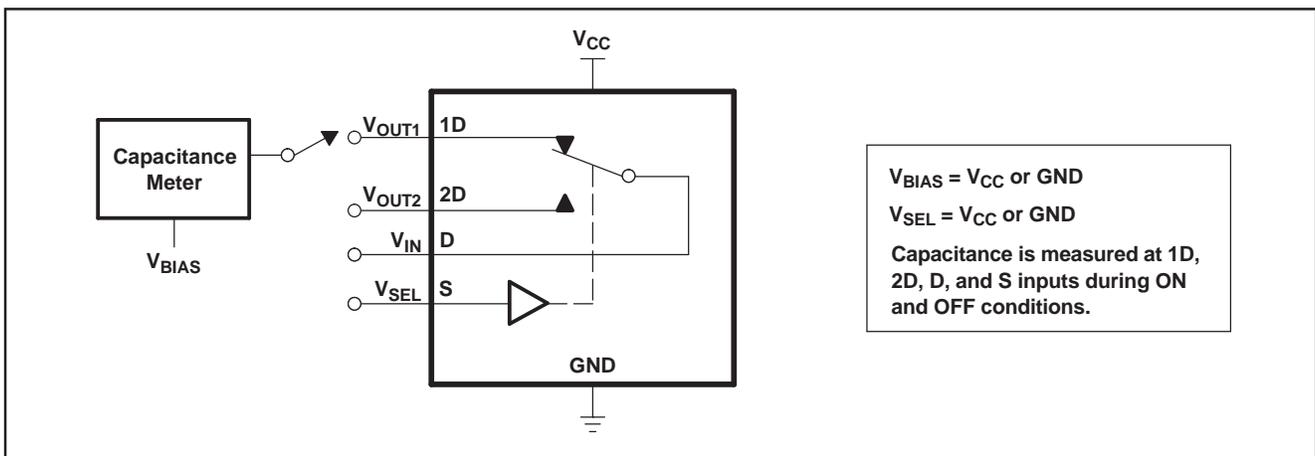
Product Folder Link(s): TS3USB31E

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB31ERSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
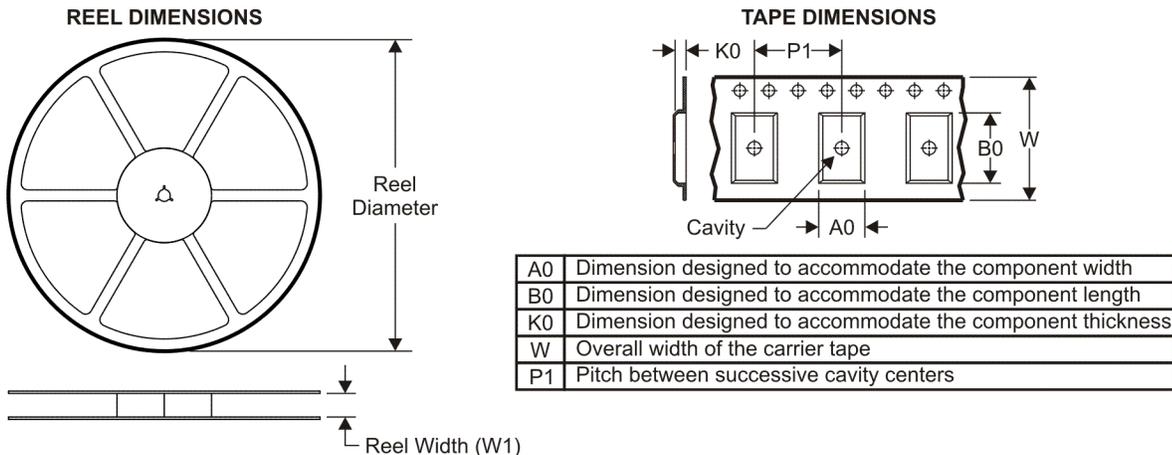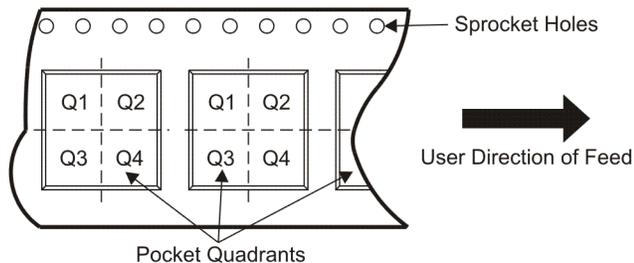
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB31ERSER	UQFN	RSE	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS
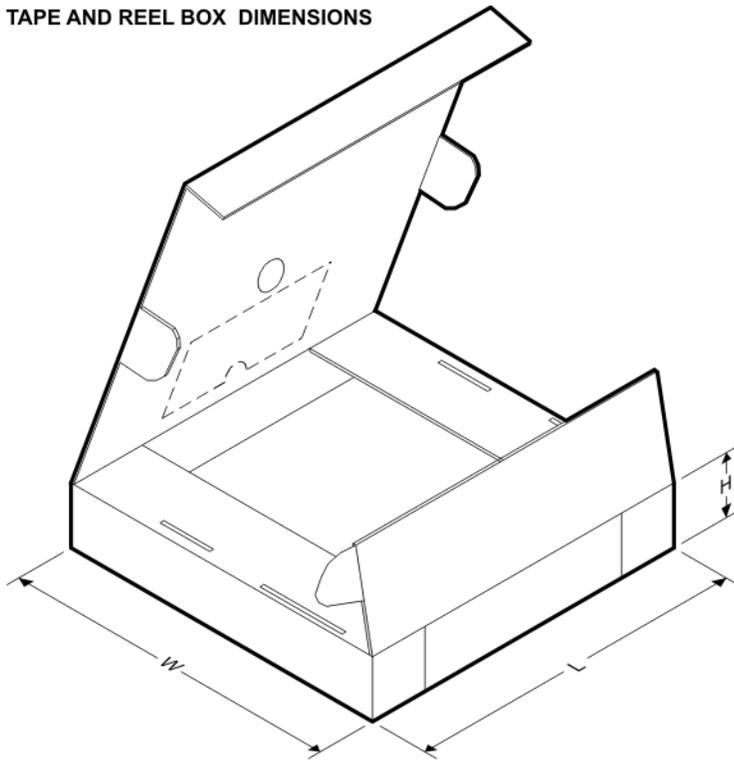
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB31ERSER	UQFN	RSE	8	3000	202.0	201.0	28.0

RSE (S−PUQFN−N8)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{1,55}{1,45}$ A

B

7   6   5

8   4

$\frac{1,55}{1,45}$

Pin 1 Index Area

1   2   3

$\frac{0,60}{0,50}$

Seating Plane

⌒ 0,05 C

$\frac{0,05}{0,00}$
Seating Height

C

1,00

0,50

6X $\frac{0,40}{0,30}$

1   2   3

Pin 1 Identifier
0,10 X 45°

8   4

2X $\frac{0,35}{0,25}$

7   6   5

2X $\frac{0,45}{0,35}$ 4X $\frac{0,30}{0,20}$

2X $\frac{0,25}{0,15}$

10X
⊕ | 0,10 Ⓜ | C A B |
  | 0,05 Ⓜ | C |

Bottom View

4207268−2/D   01/11

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   This package complies to JEDEC MO−288 variation UECD.

RSE (S−PUQFN−N8)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
(Note E)

Note D

0,05 Solder Mask Clearance for all pads

0,05

4208106−2/E 01/12

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Publication IPC−7351 is recommended for alternate designs.
       D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
       E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
       F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
           contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
       G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
           if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

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