

12-BITS 1:2 HIGH SPEED DDR2/DDR3 SWITCH

Check for Samples: [TS3DDR3642](#)

FEATURES

- High Bandwidth: 4.5GHz Typical
- Low ON Resistance
- Low Insertion Loss: $\leq 0.5\text{dB}$ (up to 933MHz)
- Low Crosstalk: -40dB at 800MHz
- Low Propagation Delay
- 12-bit Bus Width
- Bidirectional Operation
- Supports SSTL_15 and SSTL_18 Signaling
- Low Operating Current: 80 μA Typical
- V_{CC} Range: 3V –3.6V
- I_{OFF} Protection Prevents Current Leakage in Powered Down State ($V_{CC} = 0\text{ V}$)
- ESD Performance:
 - 2kV Human Body Model (A114B, Class II)
 - 1kV Charged Device Model (C101)
- 42-pin QFN Package (9 x 3.5 mm, 0.5 mm Pitch)

APPLICATIONS

- DDR2 Memory Bus Systems
- DDR3 Memory Bus Systems
- General Purpose High-Bandwidth Multiplexing

DESCRIPTION

The TS3DDR3642 is 1:2 or 2:1 high speed DDR2/DDR3 switch that offers 12-bit wide bus switching. The A port can be switched to the B or C port for all bits simultaneously. Designed for operation in DDR2 and DDR3 memory bus systems, the TS3DDR3642 uses a proprietary architecture that delivers high bandwidth (-3dB bandwidth at 4.5GHz), low insertion loss at low frequency, and very low propagation delay. The TS3DDR3642 is 1.8V logic compatible, and all switches are bi-directional for added design flexibility. The TS3DDR3642 also offers a power-down mode, in which all channels become high-Z and the device operates with minimal power.

TYPICAL APPLICATION DIAGRAM

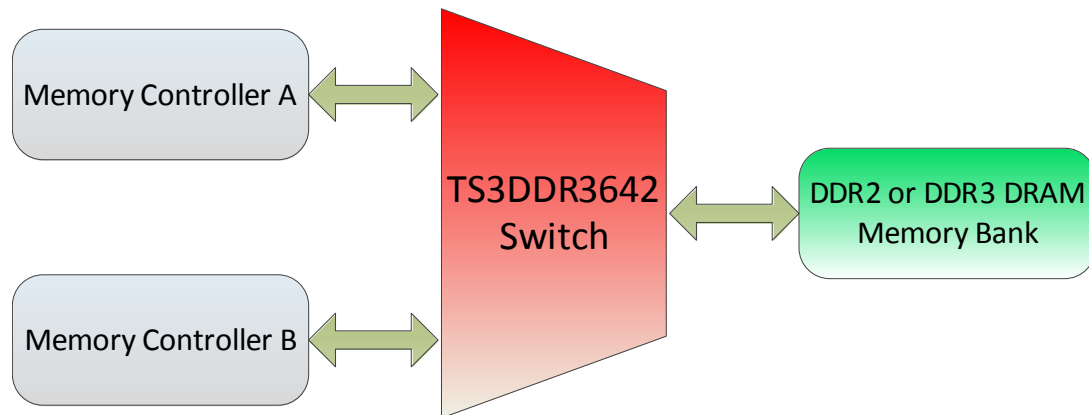


Figure 1. Typical Application Diagram showing Memory Bus Switching

PRODUCT PREVIEW


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DDR3642RUAR	PREVIEW	WQFN	RUA	42	3000	TBD	CU NIPDAU	Level-3-260C-168 HR		SL642	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

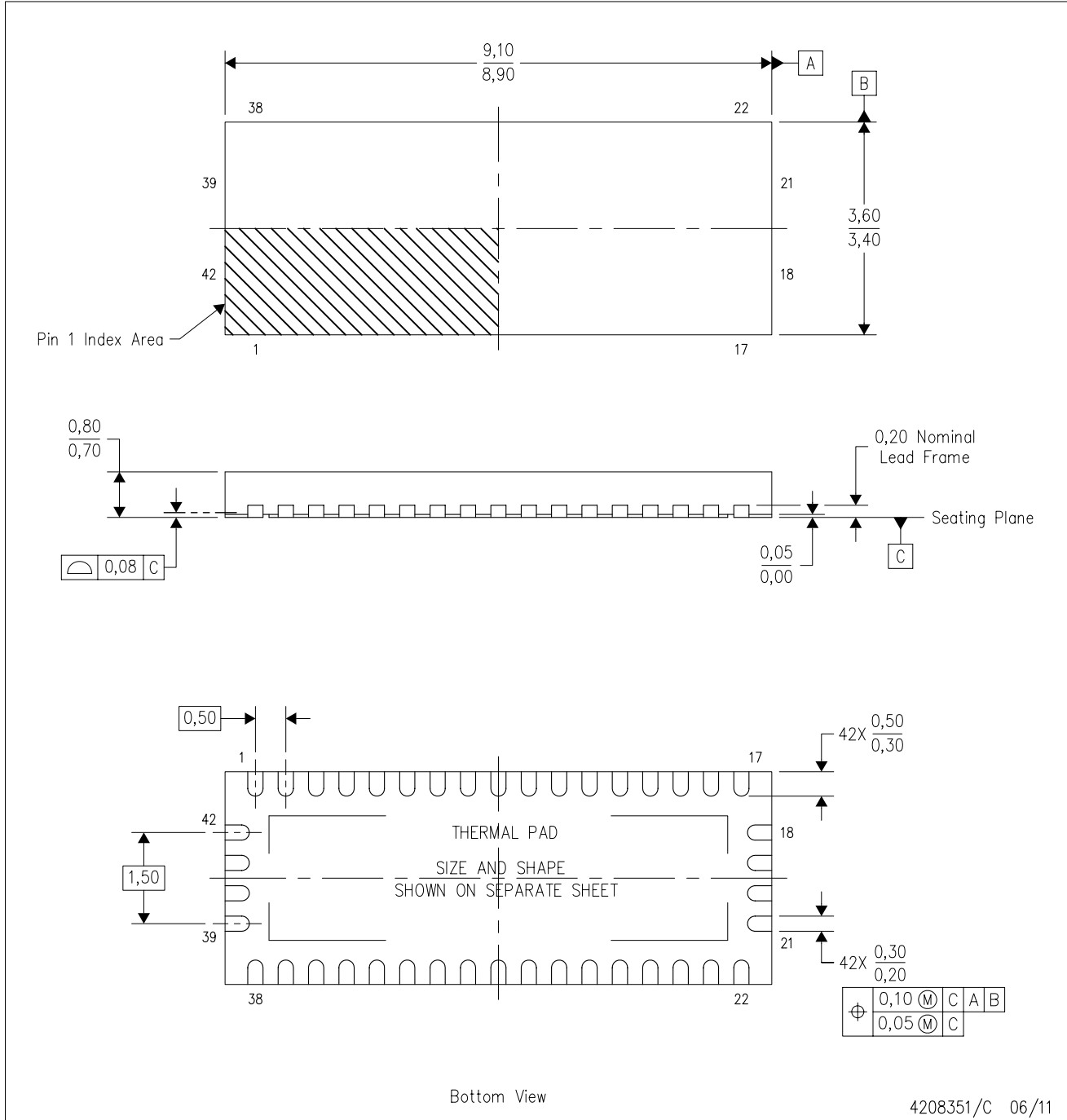
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MECHANICAL DATA

RUA (R-PWQFN-N42)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RUA (R-PWQFN-N42)

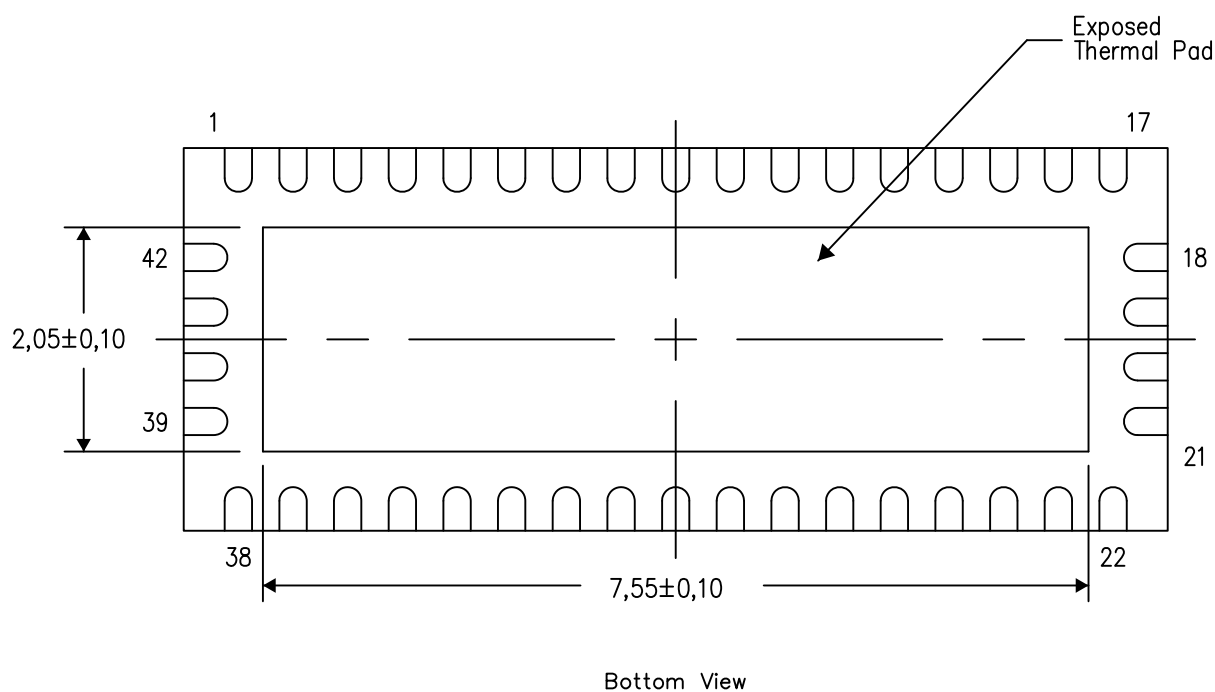
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



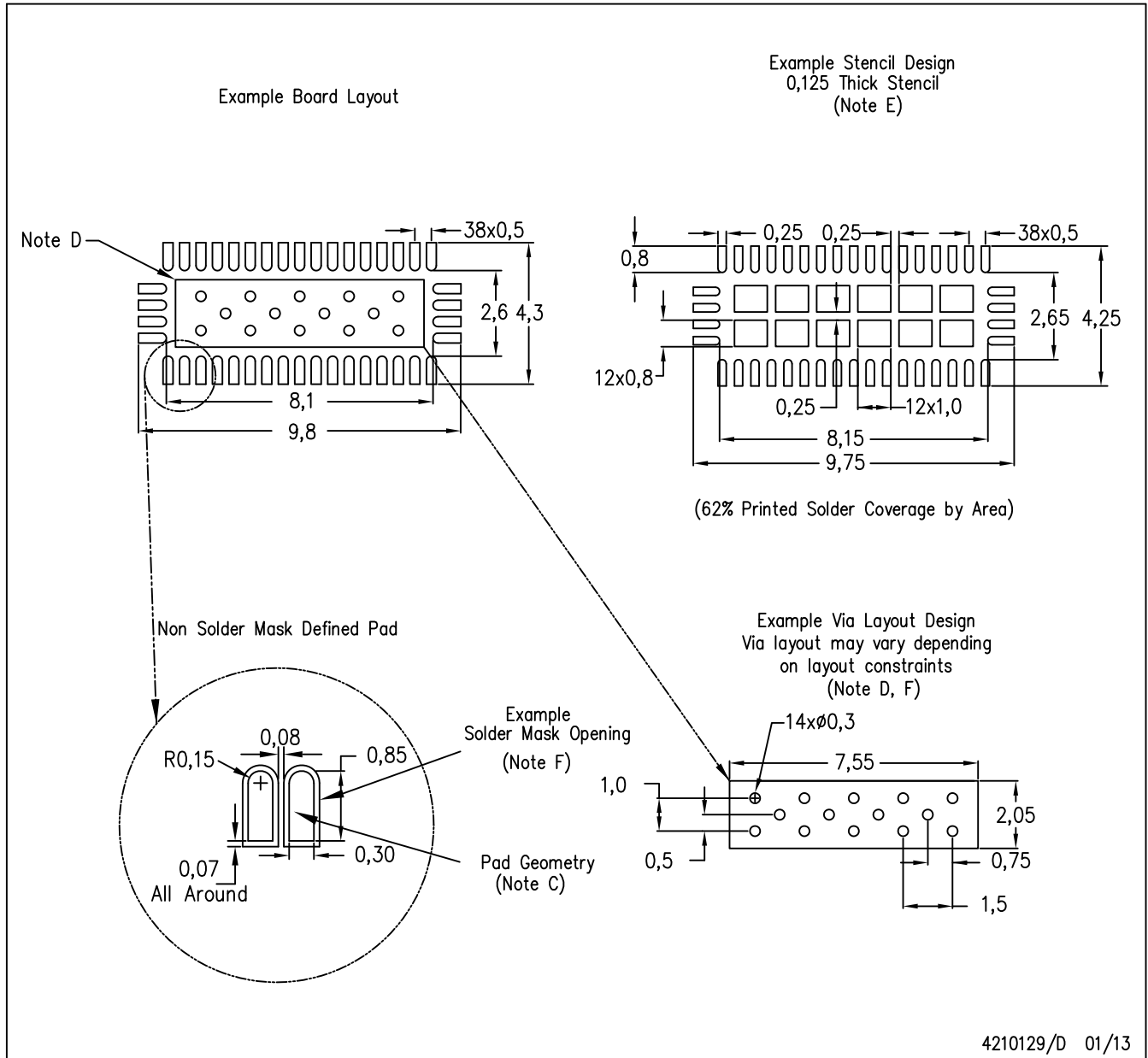
Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R-PWQFN-N42)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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