

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For tape-and-reel order entry, the DGG package is abbreviated to GR.

DESCRIPTION

This 20-bit flip-flop is designed for low-voltage 1.65-V to 3.6-V V_{CC} operation.

The 20 flip-flops of the SN74ALVCH162721 are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (\overline{CLKEN}) input is low. If \overline{CLKEN} is high, no data is stored.

A buffered output-enable (\overline{OE}) input places the 20 outputs in either a normal logic state (high or low level) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

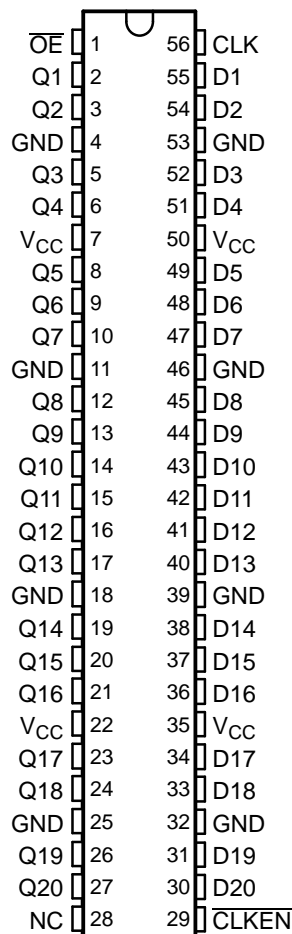
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

The SN74ALVCH162721 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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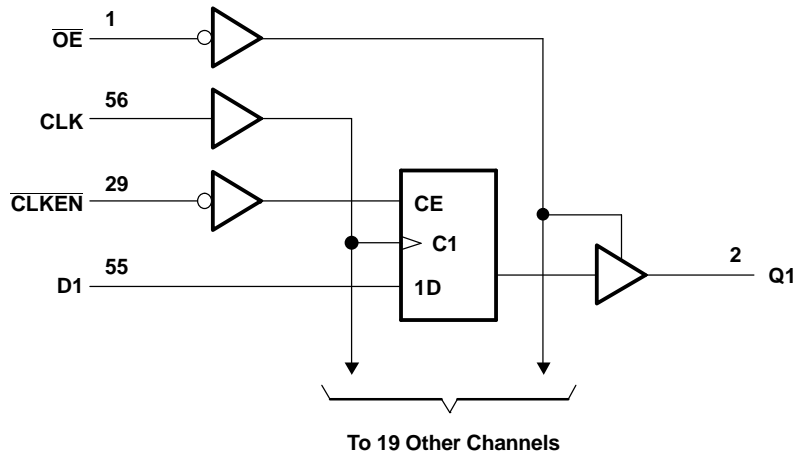
SN74ALVCH162721
3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS

SCES055G—DECEMBER 1995—REVISED SEPTEMBER 2004

FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | OUTPUT Q |
|-----------------|--------------------|--------|---|-------------|
| \overline{OE} | \overline{CLKEN} | CLK | D | |
| L | H | X | X | Q_0 |
| L | L | ↑ | H | H |
| L | L | ↑ | L | L |
| L | L | L or H | X | Q_0 |
| H | X | X | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 4.6 | V |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through each V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | 81 | °C/W |
| | | DL package | 74 | °C/W |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 0.8 | |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 1.65\text{ V}$ | -2 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | -6 | |
| | | $V_{CC} = 2.7\text{ V}$ | -8 | |
| | | $V_{CC} = 3\text{ V}$ | -12 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65\text{ V}$ | 2 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | 6 | |
| | | $V_{CC} = 2.7\text{ V}$ | 8 | |
| | | $V_{CC} = 3\text{ V}$ | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH162721
3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS

SCES055G–DECEMBER 1995–REVISED SEPTEMBER 2004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|--|-----------------|-----------------------|--------------------|-----|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | I _{OH} = -2 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -4 mA | 2.3 V | 1.9 | | | |
| | I _{OH} = -6 mA | 2.3 V | 1.7 | | | |
| | I _{OH} = -8 mA | 3 V | 2.4 | | | |
| | I _{OH} = -12 mA | 2.7 V | 2 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.2 | | | V |
| | I _{OL} = 2 mA | 1.65 V | 0.45 | | | |
| | I _{OL} = 4 mA | 2.3 V | 0.4 | | | |
| | I _{OL} = 6 mA | 2.3 V | 0.55 | | | |
| | I _{OL} = 8 mA | 3 V | 0.55 | | | |
| | I _{OL} = 8 mA | 2.7 V | 0.6 | | | |
| | I _{OL} = 12 mA | 3 V | 0.8 | | | |
| I _I | V _I = V _{CC} or GND | 3.6 V | ±5 | | | μA |
| I _{I(hold)} | V _I = 0.58 V | 1.65 V | 25 | | | μA |
| | V _I = 1.07 V | 1.65 V | -25 | | | |
| | V _I = 0.7 V | 2.3 V | 45 | | | |
| | V _I = 1.7 V | 2.3 V | -45 | | | |
| | V _I = 0.8 V | 3 V | 75 | | | |
| | V _I = 2 V | 3 V | -75 | | | |
| | V _I = 0 to 3.6 V ⁽²⁾ | 3.6 V | ±500 | | | |
| I _{OZ} | V _O = V _{CC} or GND | 3.6 V | ±10 | | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 40 | | | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | 750 | | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 3.5 | | | pF |
| C _o | V _O = V _{CC} or GND | 3.3 V | 7 | | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| | | V _{CC} = 1.8 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT | | |
|--------------------|---------------------------------|-------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|--|----|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| f _{clock} | Clock frequency | (1) | | 150 | | 150 | | 150 | | MHz | | |
| t _w | Pulse duration, CLK high or low | (1) | | 3.3 | | 3.3 | | 3.3 | | ns | | |
| t _{su} | Setup time | Data before CLK↑ | | (1) | | 4 | | 3.6 | | 3.1 | | ns |
| | | CLKEN before CLK↑ | | (1) | | 3.4 | | 3.1 | | 2.7 | | |
| t _h | Hold time | Data after CLK↑ | | (1) | | 0 | | 0 | | 0 | | ns |
| | | CLKEN after CLK↑ | | (1) | | 0 | | 0 | | 0 | | |

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|-------------------------|-----|---|-----|-------------------------|-----|---|-----|------|
| | | | MIN | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | (1) | | 150 | | 150 | | 150 | | MHz |
| t_{pd} | CLK | Q | | (1) | 1 | 6.7 | | 6.2 | 1 | 5.3 | ns |
| t_{en} | \overline{OE} | Q | | (1) | 1 | 7.2 | | 7 | 1 | 5.8 | ns |
| t_{dis} | \overline{OE} | Q | | (1) | 1 | 6.3 | | 5.4 | 1 | 5 | ns |

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

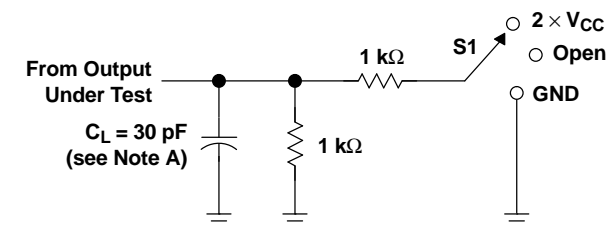
$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|--|------------------|---|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | Outputs enabled | $C_L = 50\text{ pF}, \quad f = 10\text{ MHz}$ | (1) | 55 | 59 | pF |
| | Outputs disabled | | (1) | 46 | 49 | |

(1) This information was not available at the time of publication.

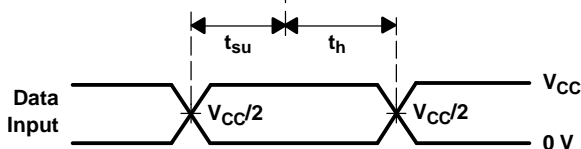
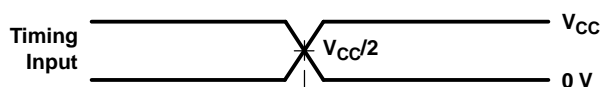
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$

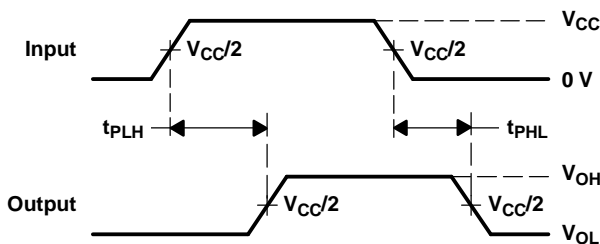


LOAD CIRCUIT

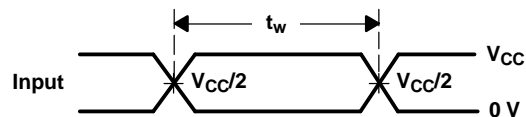
| TEST | S1 |
|-------------------|---------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 \times V_{CC} |
| t_{PHZ}/t_{PZH} | GND |



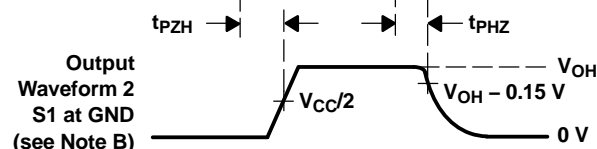
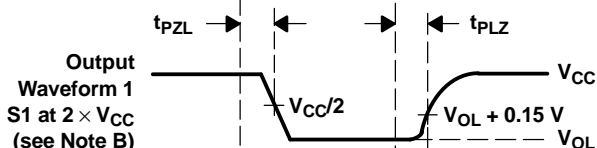
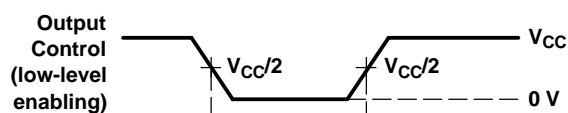
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



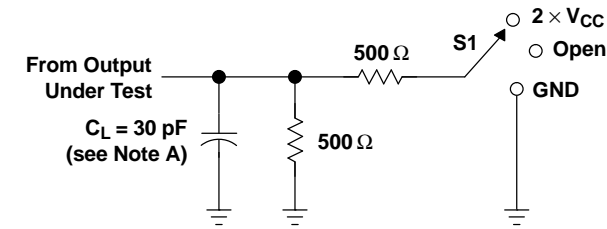
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

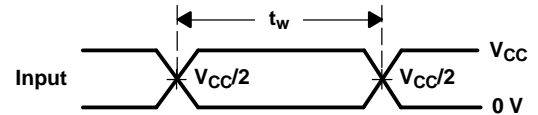
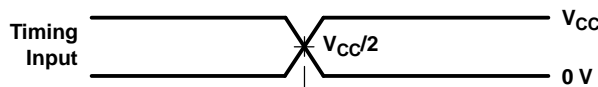
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

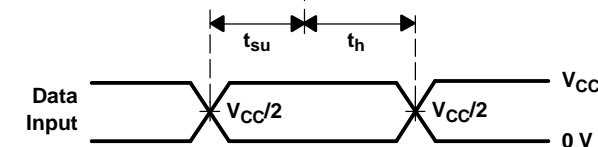


LOAD CIRCUIT

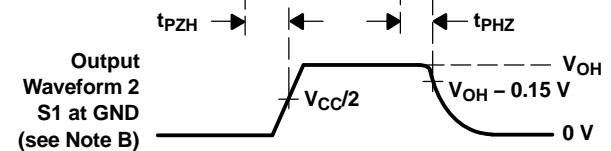
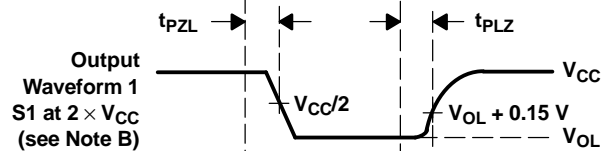
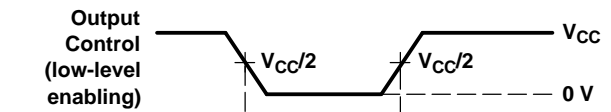
| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



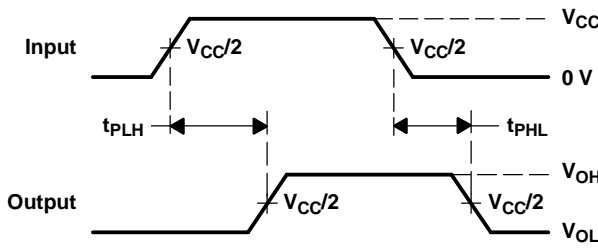
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



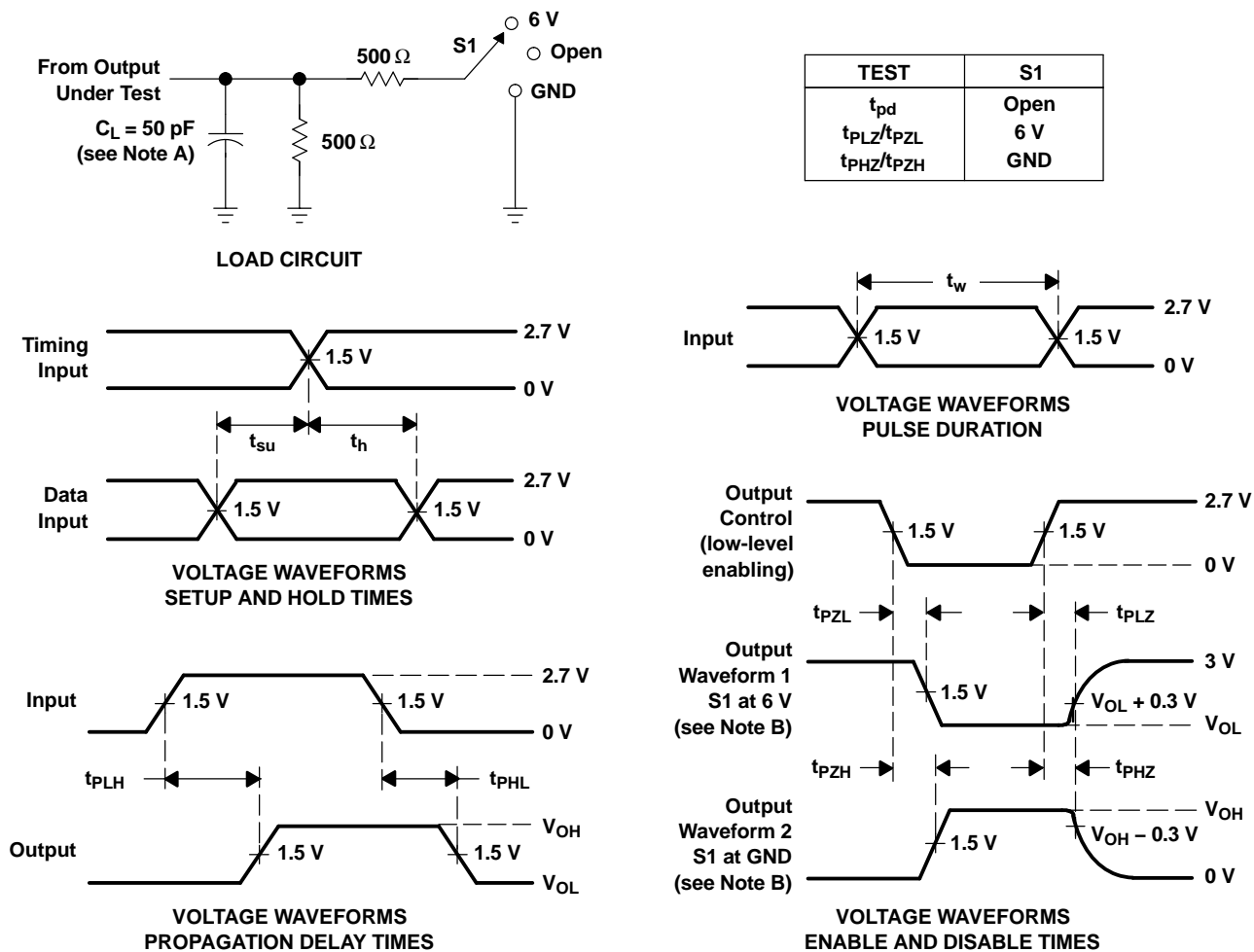
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|---------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74ALVCH162721DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162721DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162721GRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162721GRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162721DGGR | OBSOLETE | TSSOP | DGG | 56 | | TBD | Call TI | Call TI |
| SN74ALVCH162721DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162721DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162721GR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



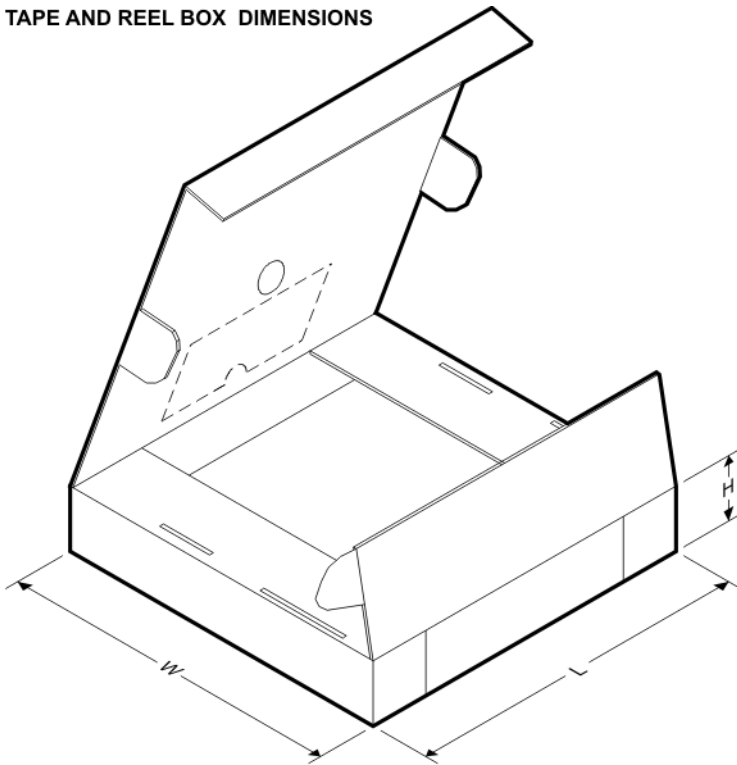
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVCH162721DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74ALVCH162721GR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVCH162721DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |
| SN74ALVCH162721GR | TSSOP | DGG | 56 | 2000 | 346.0 | 346.0 | 41.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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