SN74ALVCH32501
36-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES144G – OCTOBER 1998 – REVISED OCTOBER 2004

FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Operates From 1.65 V to 3.6 V**
- **Max t_{pd} of 3.9 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DESCRIPTION/ORDERING INFORMATION

This 36-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

This device can be used as two 18-bit transceivers or one 36-bit transceiver. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor, and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

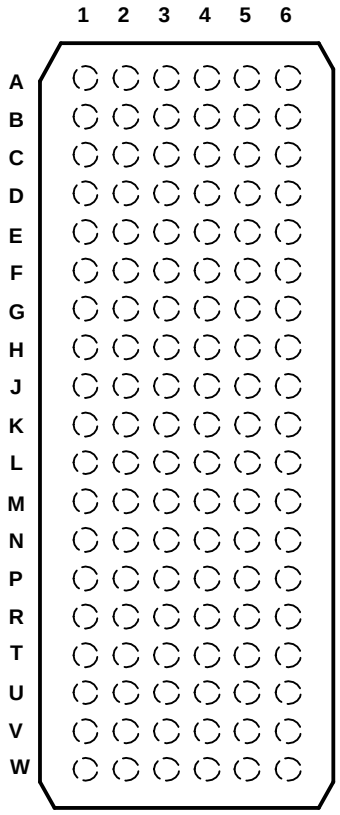
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA - GKF	Tape and reel	SN74ALVCH32501KR	ACH501
	LFBGA - ZKF (Pb-free)		74ALVCH32501ZKFR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GKF OR ZKF PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS(1)

	1	2	3	4	5	6
A	1A2	1A1	1LEAB	1CLKAB	1B1	1B2
B	1A4	1A3	1OEAB	GND	1B3	1B4
C	1A6	1A5	GND	GND	1B5	1B6
D	1A8	1A7	V_{CC}	V_{CC}	1B7	1B8
E	1A10	1A9	GND	GND	1B9	1B10
F	1A12	1A11	GND	GND	1B11	1B12
G	1A14	1A13	V_{CC}	V_{CC}	1B13	1B14
H	1A15	1A16	GND	GND	1B16	1B15
J	1A17	1A18	$1\overline{OEBA}$	1CLKBA	1B18	1B17
K	NC	2LEAB	1LEAB	GND	2CLKAB	NC
L	2A2	2A1	2OEAB	GND	2B1	2B2
M	2A4	2A3	GND	GND	2B3	2B4
N	2A6	2A5	V_{CC}	V_{CC}	2B5	2B6
P	2A8	2A7	GND	GND	2B7	2B8
R	2A10	2A9	GND	GND	2B9	2B10
T	2A12	2A11	V_{CC}	V_{CC}	2B11	2B12
U	2A14	2A13	GND	GND	2B13	2B14
V	2A15	2A16	$2\overline{OEBA}$	2CLKBA	2B16	2B15
W	2A17	2A18	2LEBA	GND	2B18	2B17

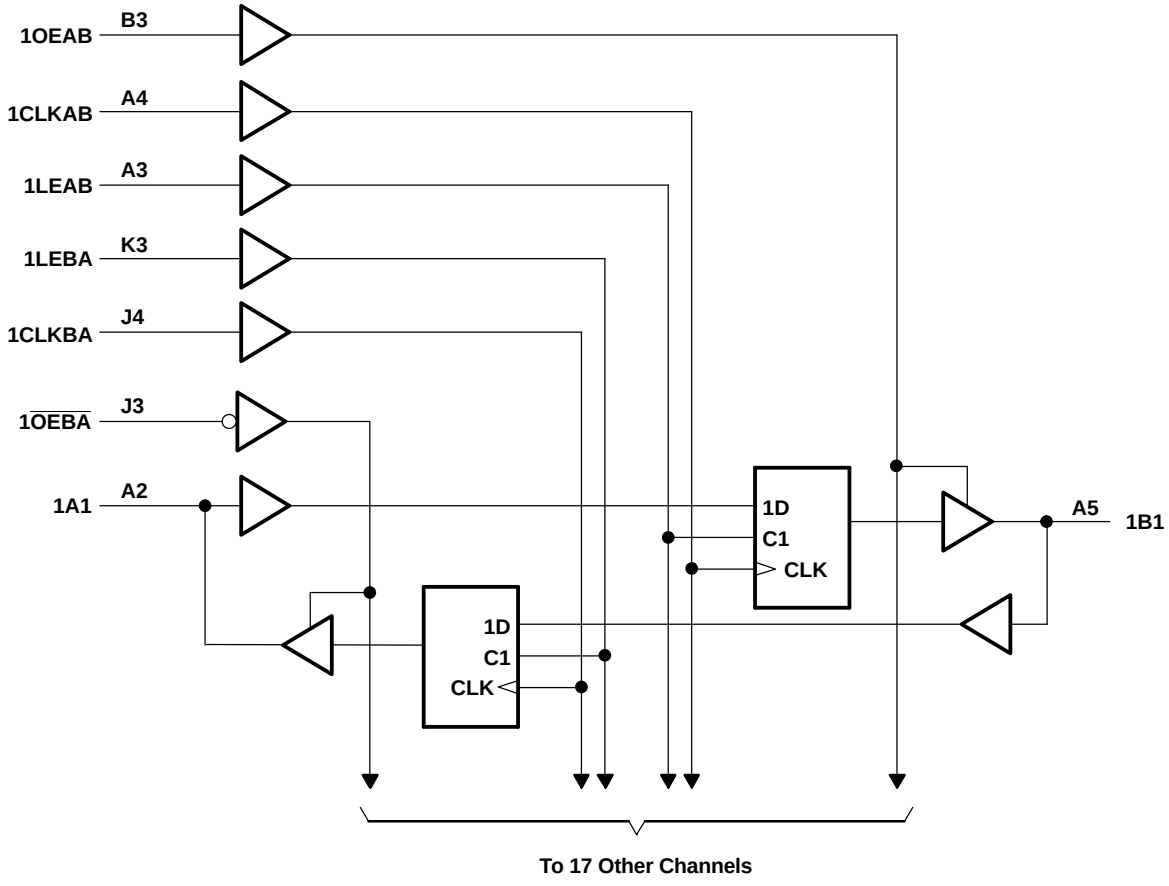
(1) NC - No internal connection

FUNCTION TABLE(1)

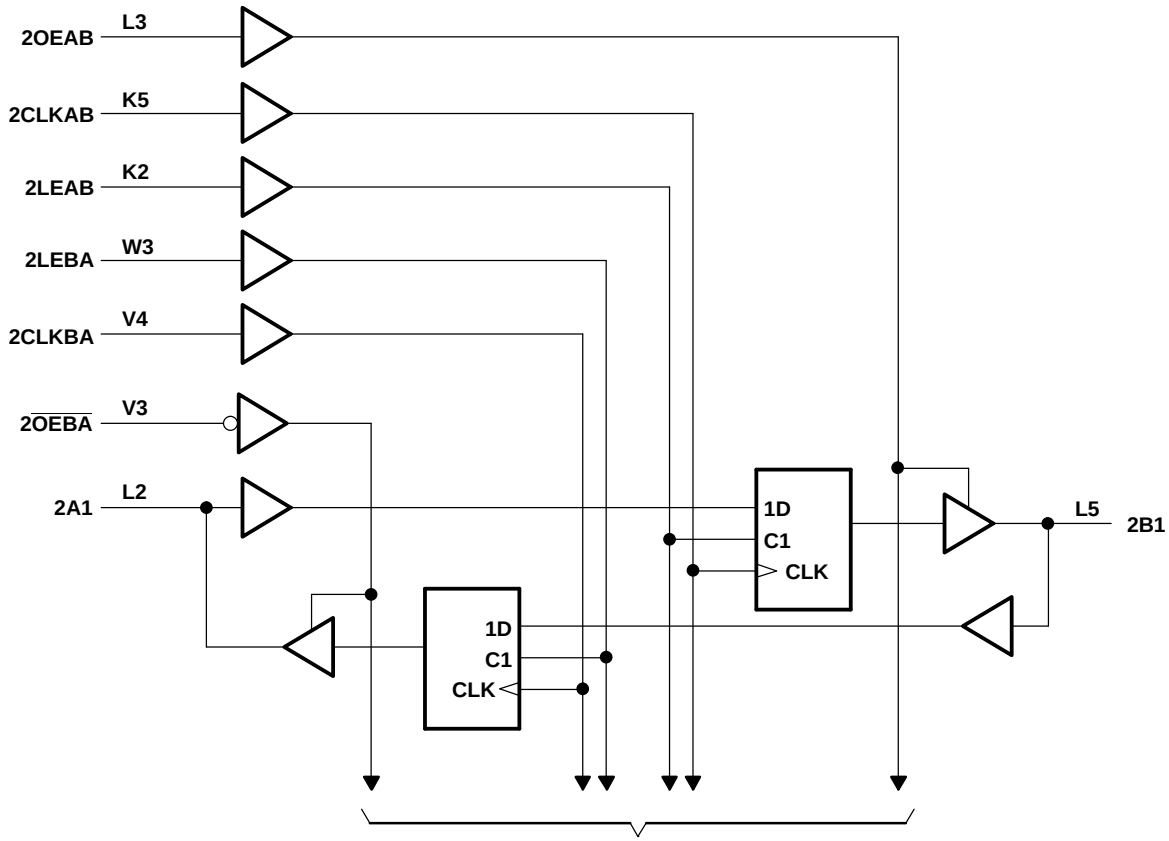
INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0(2)
H	L	L	X	B_0(3)

(1) A-to-B data flow is shown; B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
(3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range	Except I/O ports(2)	-0.5	4.6	V
		I/O ports(2)(3)	-0.5	V_{CC} + 0.5	
V_O	Output voltage range(2)(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	GKF/ZKF package		36	°C/W
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-4	mA
		V_{CC} = 2.3 V		-12	
		V_{CC} = 2.7 V		-12	
		V_{CC} = 3 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		12	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = -100 μA		1.65 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -4 mA		1.65 V	1.2			
		I_{OH} = -6 mA		2.3 V	2			
		I_{OH} = -12 mA		2.3 V	1.7			
				2.7 V	2.2			
				3 V	2.4			
		I_{OH} = -24 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 6 mA		2.3 V			0.4	
		I_{OL} = 12 mA		2.3 V			0.7	
				2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I		$V_I = V_{CC}$ or GND		3.6 V			±5	μA
$I_{I(hold)}$		V_I = 0.58 V		1.65 V	25			μA
		V_I = 1.07 V			-25			
		V_I = 0.7 V		2.3 V	45			
		V_I = 1.7 V			-45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			-75			
		V_I = 0 to 3.6 V(2)		3.6 V			±500	
I_{OZ}(3)		$V_O = V_{CC}$ or GND		3.6 V			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			80	μA
ΔI_{CC}		One input at V_{CC} - 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		4		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				(1)		150		150		150	MHz
t_w	Pulse duration	LE high		(1)		3.3		3.3		3.3		ns
		CLK high or low		(1)		3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑		(1)		2.2		2.1		1.7		ns
		Data before LE↓	CLK high	(1)		1.9		1.6		1.5		
			CLK low	(1)		1.3		1.1		1		
t_h	Hold time	Data after CLK↑		(1)		0.6		0.6		0.7		ns
		Data after LE↓	CLK high or low	(1)		1.4		1.7		1.4		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		150		150		150		MHz
t_{pd}	A or B	B or A		(1)	1	4.8		4.5	1	3.9	ns
	LE	A or B		(1)	1.1	5.7		5.3	1.3	4.6	
	CLK			(1)	1.2	6.1		5.6	1.4	4.9	
t_{en}	OEAB	B		(1)	1	5.8		5.3	1	4.6	ns
t_{dis}	OEAB	B		(1)	1.5	6.2		5.7	1.4	5	ns
t_{en}	$\overline{OEBA}$	A		(1)	1.3	6.3		6	1.1	5	ns
t_{dis}	$\overline{OEBA}$	A		(1)	1.3	5.3		4.6	1.3	4.2	ns

(1) This information was not available at the time of publication.

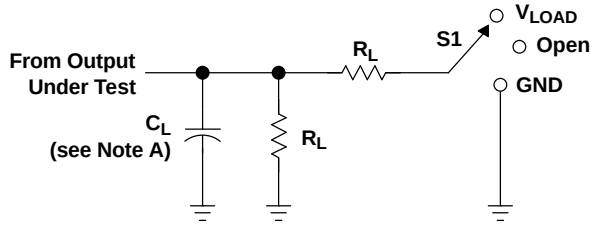
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	(1)	44	54	pF
		Outputs disabled		(1)	6	6	

(1) This information was not available at the time of publication.

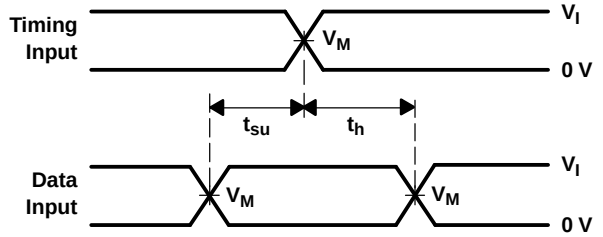
PARAMETER MEASUREMENT INFORMATION



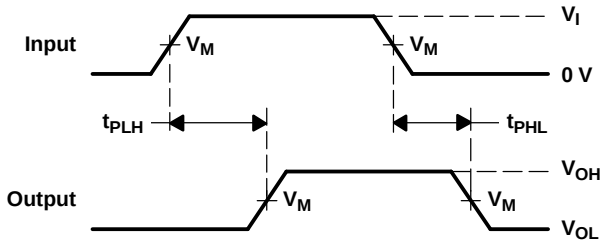
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

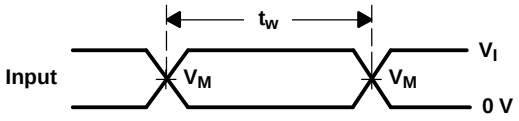
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



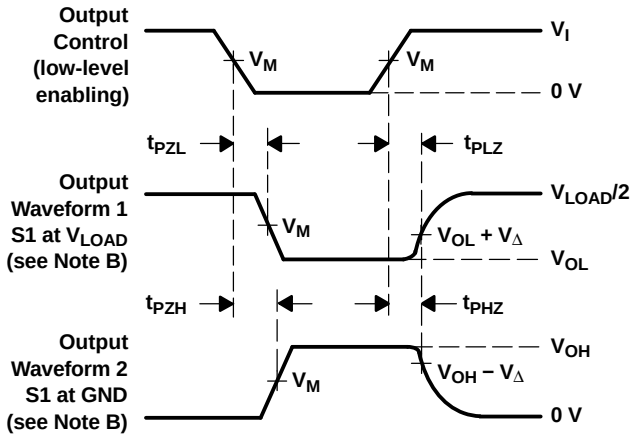
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ALVCH32501ZKFR	ACTIVE	LFBGA	ZKF	114	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	ACH501	Samples
SN74ALVCH32501KR	NRND	BGA MICROSTAR	GKF	114	1000	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	ACH501	

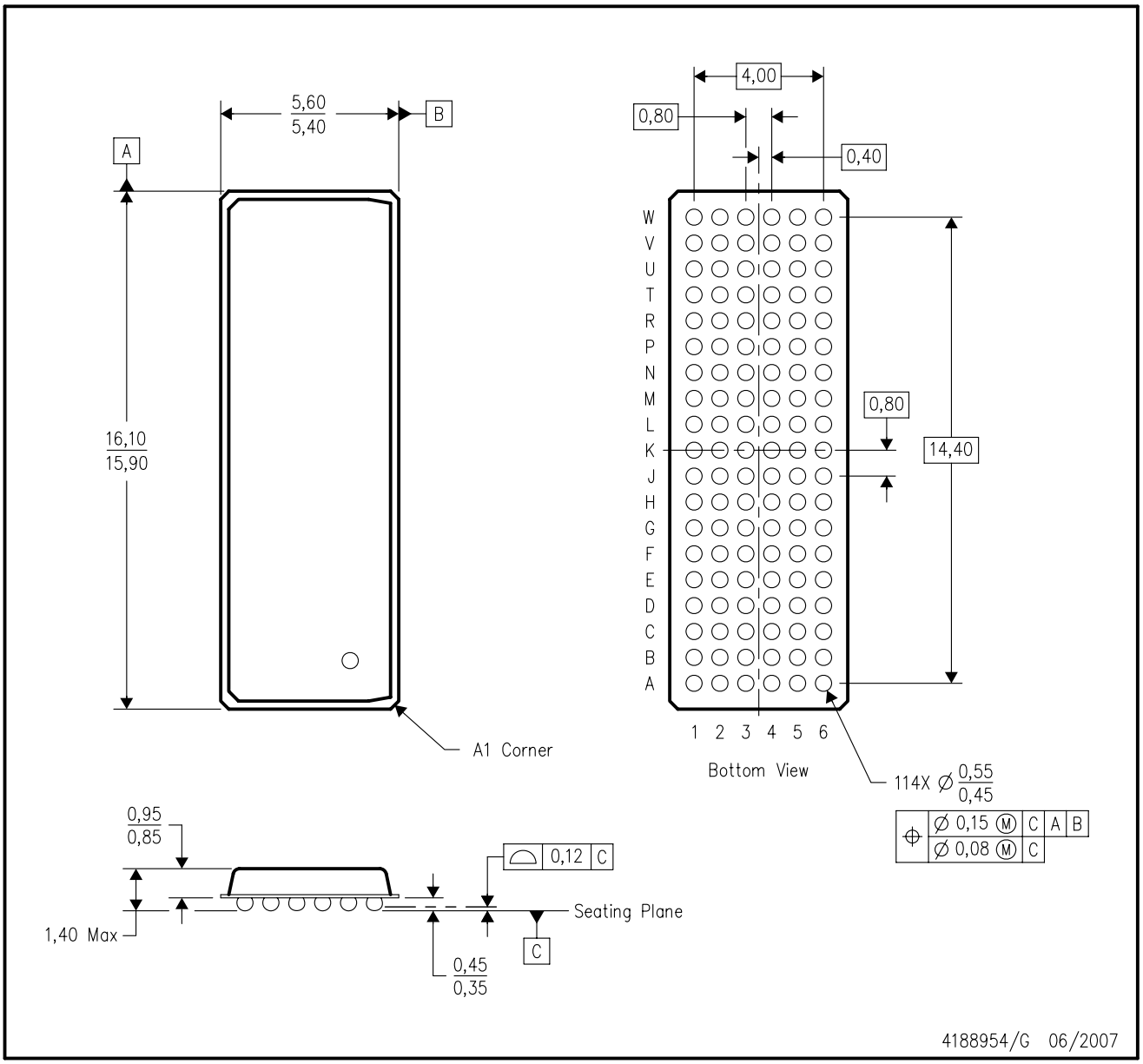
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

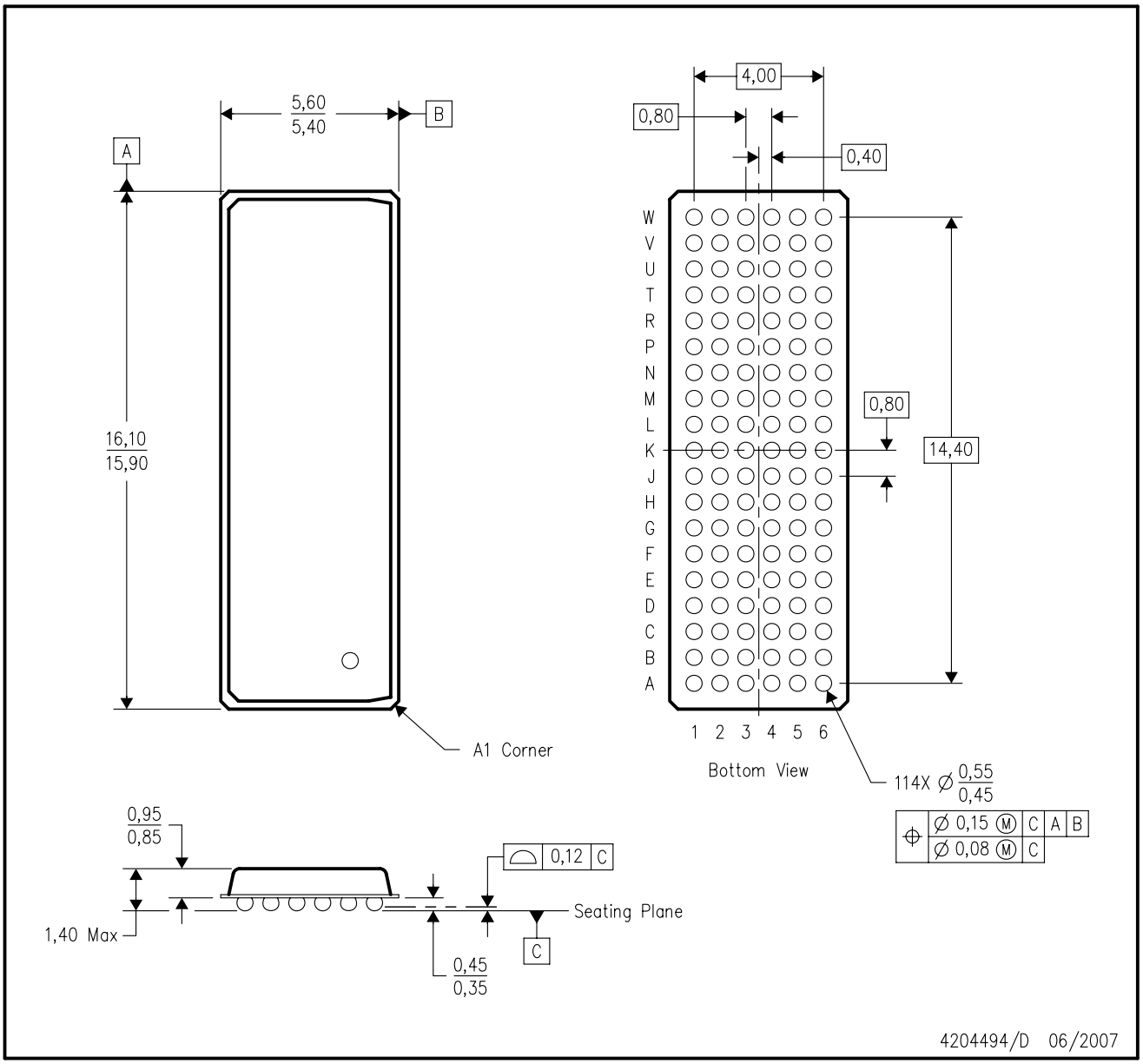
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

GKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation DC.
D. This package is tin–lead (SnPb). Refer to the 114 ZKF package (drawing 4204494) for lead–free.

ZKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation DC.
D. This package is lead–free. Refer to the 114 GKF package (drawing 4188954) for tin–lead (SnPb).

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