

SN54ALVTH32244, SN74ALVTH32244 2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- High Drive ($-24/24$ mA at 2.5-V V_{CC} and $-32/64$ mA at 3.3-V V_{CC})
- I_{off} and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds $V_{CC} + 0.5$ V
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- ESD Protection Exceeds JESD-22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

NOTE: For tape and reel order entry:
The GKER package is abbreviated to KR.

description

The 'ALVTH32244 devices are 32-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

When V_{CC} is between 0 and 1.2-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2-V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH32244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH32244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

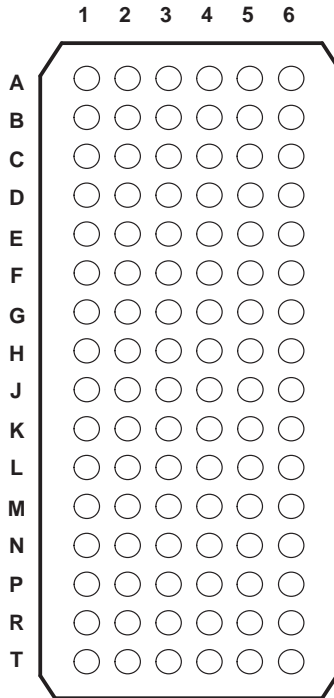


Copyright © 1999, Texas Instruments Incorporated

SN54ALVTH32244, SN74ALVTH32244
2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

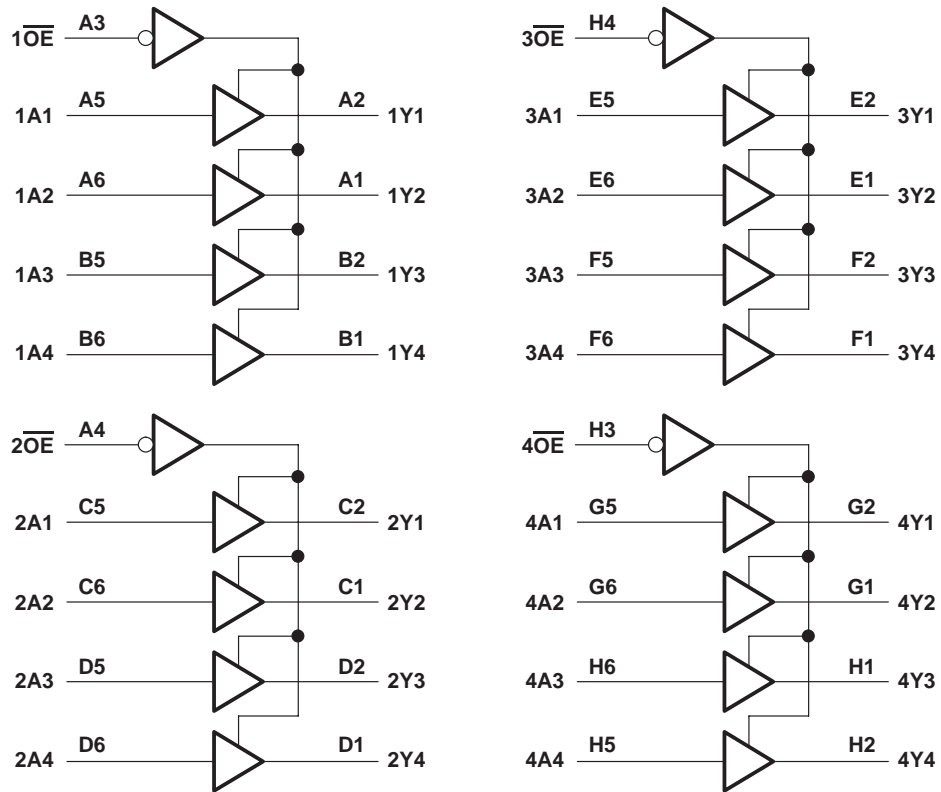
GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Y2	1Y1	$\overline{1OE}$	$\overline{2OE}$	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	$1V_{CC}$	$1V_{CC}$	2A1	2A2
D	2Y4	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	$1V_{CC}$	$1V_{CC}$	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	$\overline{4OE}$	$\overline{3OE}$	4A4	4A3
J	5Y2	5Y1	$\overline{5OE}$	$\overline{6OE}$	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	$2V_{CC}$	$2V_{CC}$	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	$2V_{CC}$	$2V_{CC}$	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	$\overline{8OE}$	$\overline{7OE}$	8A4	8A3

logic diagram (positive logic)



NOTE A: $1V_{CC}$ is associated with these channels.

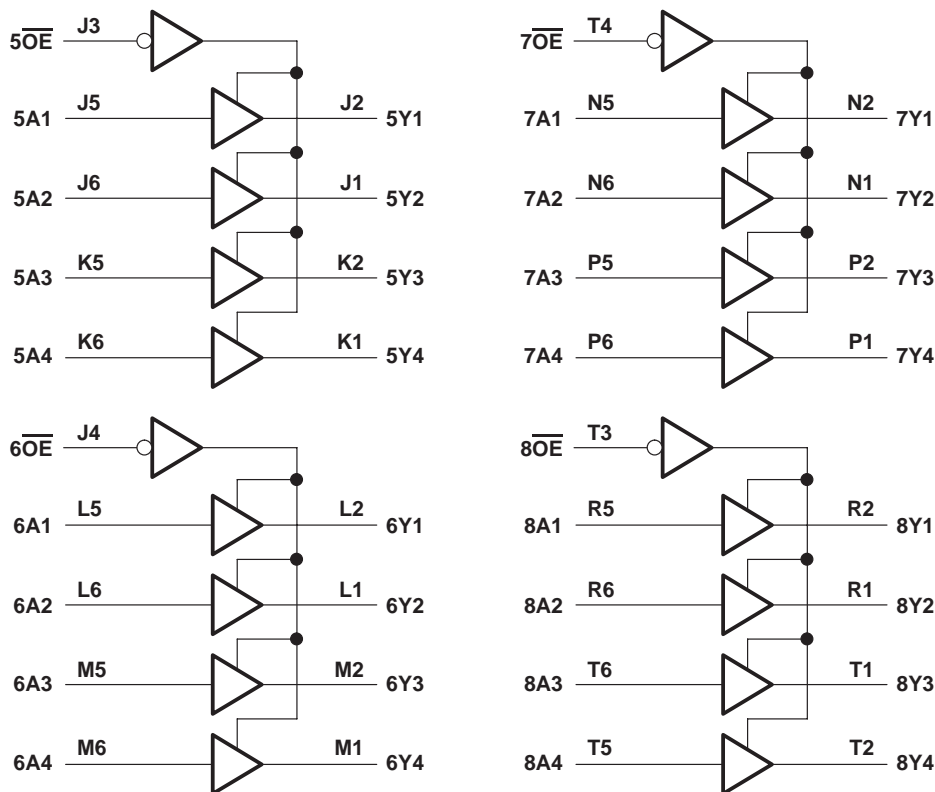
SN54ALVTH32244, SN74ALVTH32244

2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

logic diagram (positive logic)



NOTE A: $2V_{CC}$ is associated with these channels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, I_O : SN54ALVTH32244	96 mA
SN74ALVTH32244	128 mA
Current into any output in the high state, I_O (see Note 2): SN54ALVTH32244	48 mA
SN74ALVTH32244	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3)	40°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.



SN54ALVTH32244, SN74ALVTH32244 2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 4)

		SN54ALVTH32244		SN74ALVTH32244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.3	2.7	2.3	2.7	V
V_{IH}	High-level input voltage	1.7		1.7		V
V_{IL}	Low-level input voltage		0.7		0.7	V
V_I	Input voltage	0	5.5	0	5.5	V
I_{OH}	High-level output current		-6		-8	mA
I_{OL}	Low-level output current		6		8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$		18		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s/V}$
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 4)

		SN54ALVTH32244		SN74ALVTH32244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	3	3.6	3	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		24		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s/V}$
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTH32244, SN74ALVTH32244

2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH32244			SN74ALVTH32244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.3\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V
V_{OH}		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.3\text{ V}$		1.8			1.8			
V_{OL}		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2			V
		$V_{CC} = 2.3\text{ V}$		$I_{OL} = 6\text{ mA}$			0.4			
				$I_{OL} = 8\text{ mA}$			0.4			
				$I_{OL} = 18\text{ mA}$			0.5			
				$I_{OL} = 24\text{ mA}$			0.5			
I_I		Control inputs $V_{CC} = 2.7\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1			μA
				$V_{CC} = 0\text{ or } 2.7\text{ V}$, $V_I = 5.5\text{ V}$		10			10	
		Data inputs $V_{CC} = 2.7\text{ V}$		$V_I = V_{CC}$			1			
				$V_I = 0$			-5			
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$					± 100			μA
I_{BHL}^\ddagger		$V_{CC} = 2.3\text{ V}$, $V_I = 0.7\text{ V}$		115			115			μA
I_{BHH}^\S		$V_{CC} = 2.3\text{ V}$, $V_I = 1.7\text{ V}$		-10			-10			μA
I_{BHLO}^\P		$V_{CC} = 2.7\text{ V}$, $V_I = 0\text{ to } V_{CC}$		300			300			μA
$I_{BHHO}^\#$		$V_{CC} = 2.7\text{ V}$, $V_I = 0\text{ to } V_{CC}$		-300			-300			μA
I_{EX}^\parallel		$V_{CC} = 2.3\text{ V}$, $V_O = 5.5\text{ V}$		125			125			μA
$I_{OZ(PU/PD)}^\star$		$V_{CC} \leq 1.2\text{ V}$, $V_O = 0.5\text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$		± 100			± 100			μA
I_{OZH}		$V_{CC} = 2.7\text{ V}$, $V_O = 2.3\text{ V}$, $V_I = 0.7\text{ V or } 1.7\text{ V}$		5			5			μA
I_{OZL}		$V_{CC} = 2.7\text{ V}$, $V_O = 0.5\text{ V}$, $V_I = 0.7\text{ V or } 1.7\text{ V}$		-5			-5			μA
I_{CC}		$V_{CC} = 2.7\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$		Outputs high		0.04		0.1		mA
				Outputs low		2.3		4.5		
				Outputs disabled		0.04		0.1		
C_i		$V_{CC} = 2.5\text{ V}$, $V_I = 2.5\text{ V or } 0$		3			3			pF
C_o		$V_{CC} = 2.5\text{ V}$, $V_O = 2.5\text{ V or } 0$		6			6			pF

† All typical values are at $V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}\text{ max}$. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to $V_{IL}\text{ max}$.

§ The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}\text{ min}$. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH}\text{ min}$.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

* High-impedance state during power up or power down

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54ALVTH32244, SN74ALVTH32244
2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

**electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALVTH32244		SN74ALVTH32244		UNIT
				MIN	TYP†	MAX	MIN	
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V
V_{OH}		$V_{CC} = 3\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
		$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
V_{OL}		$V_{CC} = 3\text{ V to }3.6\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		V
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4		
				$I_{OL} = 24\text{ mA}$		0.5		
				$I_{OL} = 32\text{ mA}$				
				$I_{OL} = 48\text{ mA}$		0.55		
		$I_{OL} = 64\text{ mA}$				0.55		
I_I		Control inputs $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND $V_{CC} = 0$ or 3.6 V , $V_I = 5.5\text{ V}$		± 1		± 1		μA
				10		10		
		Data inputs $V_{CC} = 3.6\text{ V}$		20		20		
				1		1		
		$V_I = 0$		-5		-5		
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA
I_{BHL}^\ddagger		$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75		75		μA
I_{BHH}^\S		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$		-75		-75		μA
I_{BHLO}^\P		$V_{CC} = 3.6\text{ V}$, $V_I = 0$ to V_{CC}		500		500		μA
$I_{BHHO}^\#$		$V_{CC} = 3.6\text{ V}$, $V_I = 0$ to V_{CC}		-500		-500		μA
I_{EX}^\parallel		$V_{CC} = 3\text{ V}$, $V_O = 5.5\text{ V}$		125		125		μA
$I_{OZ}(\text{PU/PD})^\star$		$V_{CC} \leq 1.2\text{ V}$, $V_O = 0.5\text{ V to }V_{CC}$, $V_I = \text{GND or }V_{CC}$, $\text{OE} = \text{don't care}$		± 100		± 100		μA
I_{OZH}		$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$, $V_I = 0.8\text{ V or }2\text{ V}$		5		5		μA
I_{OZL}		$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$, $V_I = 0.8\text{ V or }2\text{ V}$		-5		-5		μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.07 0.1		mA
				Outputs low		3.2 5		
				Outputs disabled		0.07 0.1		
ΔI_{CC}^\square		$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND		0.4		0.4		mA
C_i		$V_{CC} = 3.3\text{ V}$		3		3		pF
C_o		$V_{CC} = 3.3\text{ V}$		6		6		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTH32244, SN74ALVTH32244
2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH32244		SN74ALVTH32244		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.1	1	3	ns
t_{PHL}			1	3.6	1	3.5	
t_{PZH}	\overline{OE}	Y	1.1	6	1.1	5.9	ns
t_{PZL}			1.1	4.8	1.1	4.7	
t_{PHZ}	\overline{OE}	Y	1.5	4.5	1.5	4.4	ns
t_{PLZ}			1	3.5	1	3.4	

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

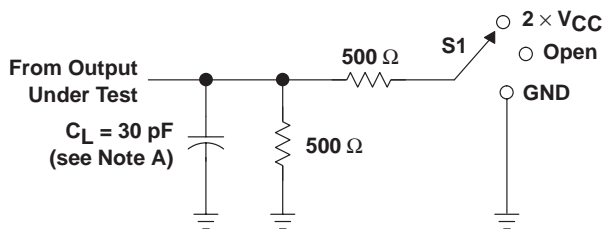
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH32244		SN74ALVTH32244		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	1	2.4	ns
t_{PHL}			1	2.6	1	2.5	
t_{PZH}	\overline{OE}	Y	1	3.9	1	3.8	ns
t_{PZL}			1	3	1	2.9	
t_{PHZ}	\overline{OE}	Y	1.5	4.3	1.5	4.2	ns
t_{PLZ}			1.5	3.7	1.5	3.6	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



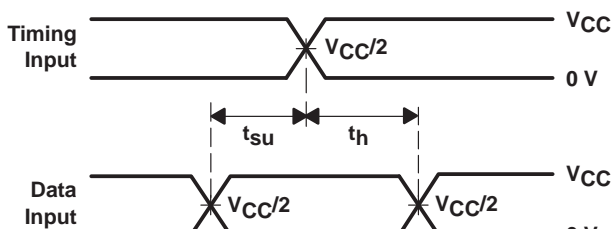
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

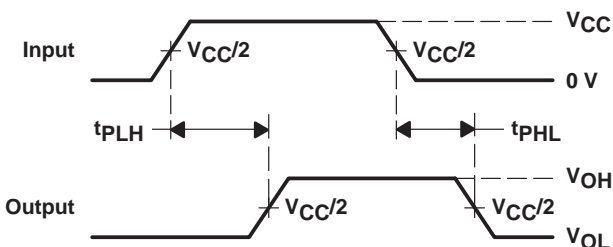


LOAD CIRCUIT

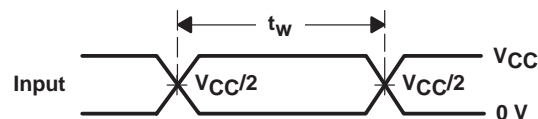
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



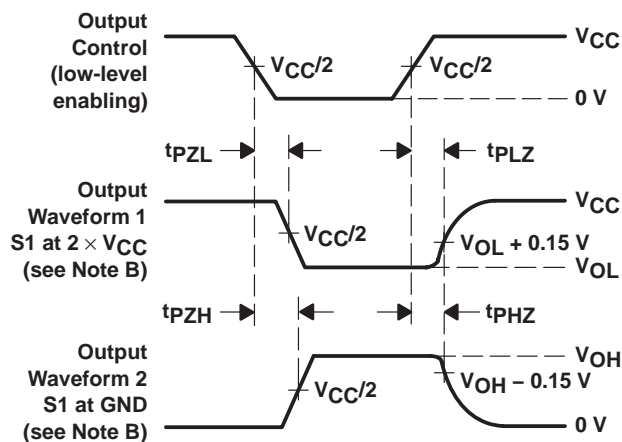
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

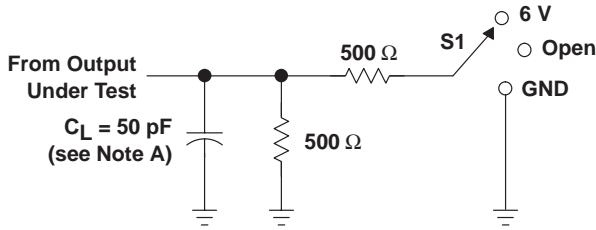
Figure 1. Load Circuit and Voltage Waveforms

SN54ALVTH32244, SN74ALVTH32244
2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

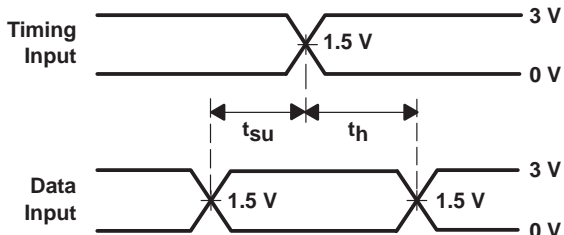
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

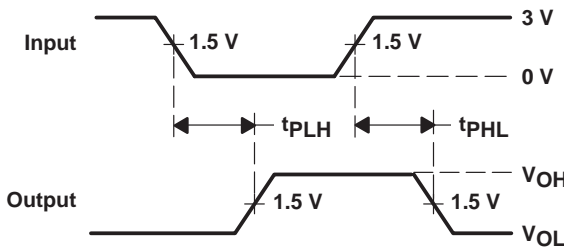


LOAD CIRCUIT

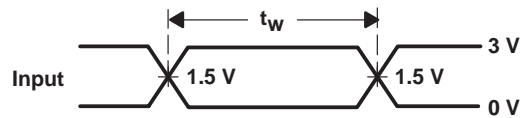
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



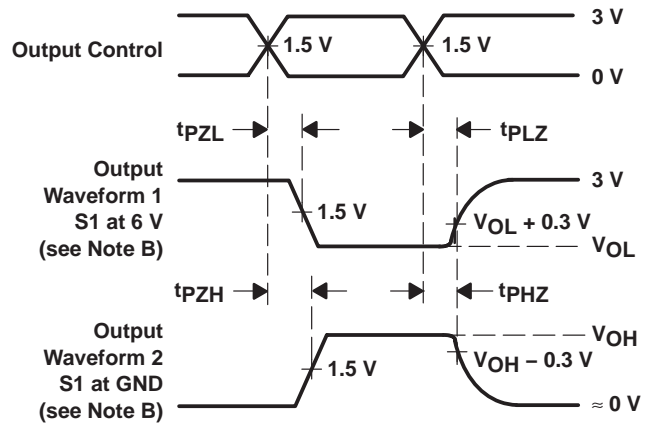
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ALVTH32244ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	VL244	Samples
SN74ALVTH32244KR	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	VL244	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

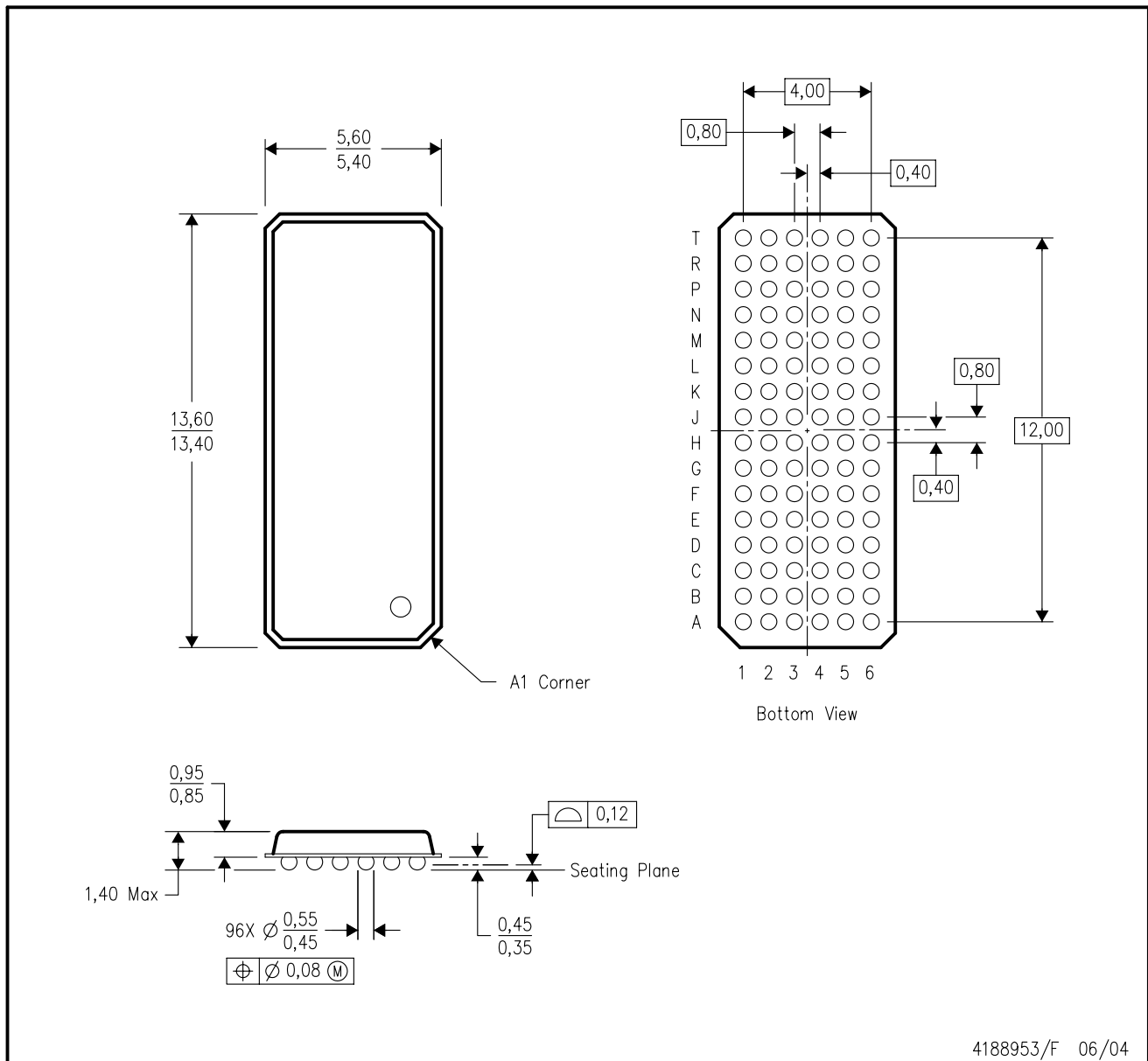
(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GKE (R-PBGA-N96)

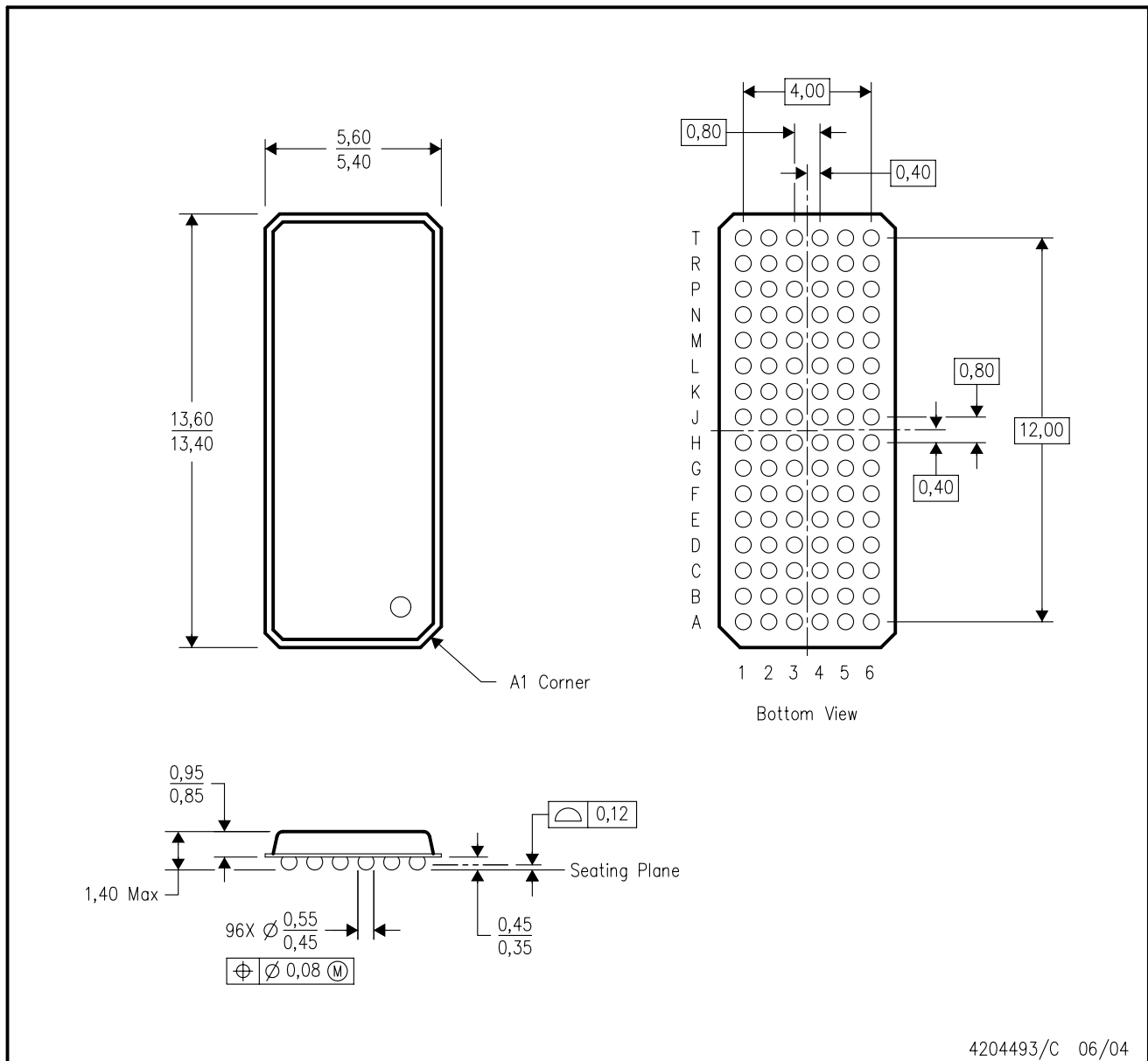
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com