# SN74ALVCH32374
# 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES283D – OCTOBER 1999 – REVISED AUGUST 2004

## FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Max $t_{pd}$ of 4.2 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

## DESCRIPTION/ORDERING INFORMATION

This 32-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74ALVCH32374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs. The output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**ORDERING INFORMATION**

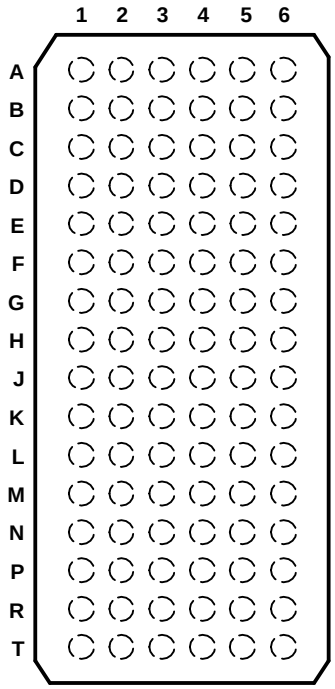
| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| -40°C to 85°C | LFBGA - GKE | Tape and reel | SN74ALVCH32374KR | ACH374 |
| | LFBGA - ZKE (Pb-free) | | 74ALVCH32374ZKER | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE (each flip-flop)**

| INPUTS | | | OUTPUT Q |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

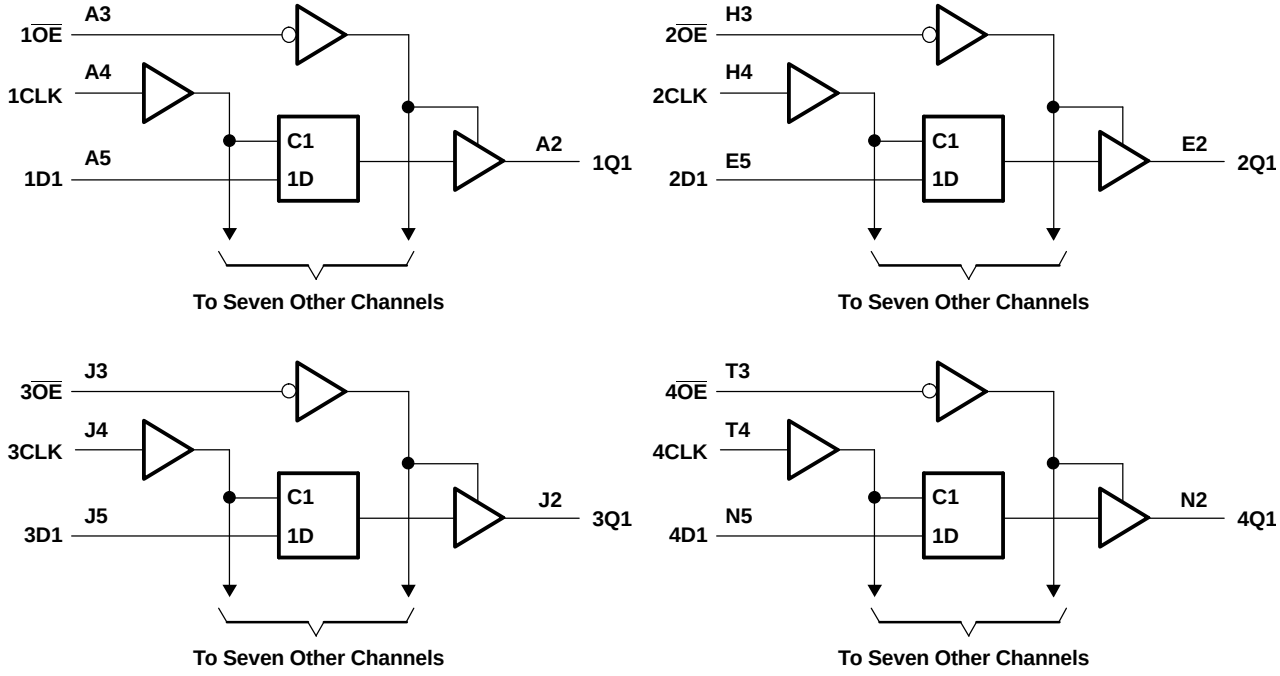
**GKE OR ZKE PACKAGE**
**(TOP VIEW)**




## TERMINAL ASSIGNMENTS

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | 1Q2 | 1Q1 | $1\overline{OE}$ | 1CLK | 1D1 | 1D2 |
| B | 1Q4 | 1Q3 | GND | GND | 1D3 | 1D4 |
| C | 1Q6 | 1Q5 | $V_{CC}$ | $V_{CC}$ | 1D5 | 1D6 |
| D | 1Q8 | 1Q7 | GND | GND | 1D7 | 1D8 |
| E | 2Q2 | 2Q1 | GND | GND | 2D1 | 2D2 |
| F | 2Q4 | 2Q3 | $V_{CC}$ | $V_{CC}$ | 2D3 | 2D4 |
| G | 2Q6 | 2Q5 | GND | GND | 2D5 | 2D6 |
| H | 2Q7 | 2Q8 | $2\overline{OE}$ | 2CLK | 2D8 | 2D7 |
| J | 3Q2 | 3Q1 | $3\overline{OE}$ | 3CLK | 3D1 | 3D2 |
| K | 3Q4 | 3Q3 | GND | GND | 3D3 | 3D4 |
| L | 3Q6 | 3Q5 | $V_{CC}$ | $V_{CC}$ | 3D5 | 3D6 |
| M | 3Q8 | 3Q7 | GND | GND | 3D7 | 3D8 |
| N | 4Q2 | 4Q1 | GND | GND | 4D1 | 4D2 |
| P | 4Q4 | 4Q3 | $V_{CC}$ | $V_{CC}$ | 4D3 | 4D4 |
| R | 4Q6 | 4Q5 | GND | GND | 4D5 | 4D6 |
| T | 4Q7 | 4Q8 | $4\overline{OE}$ | 4CLK | 4D8 | 4D7 |

## LOGIC DIAGRAM (POSITIVE LOGIC)



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 4.6 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | 4.6 | V |
| $V_O$ | Output voltage range(2)(3) | | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | GKE/ZKE package | | 40 | °C/W |
| $T_{stg}$ | Storage temperature range | | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | -4 | mA |
| | | $V_{CC}$ = 2.3 V | | -8 | |
| | | $V_{CC}$ = 2.7 V | | -12 | |
| | | $V_{CC}$ = 3 V | | -24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = -100 μA | | 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | | | V |
| | | $I_{OH}$ = -4 mA | | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = -8 mA | | 2.3 V | 1.7 | | | |
| | | $I_{OH}$ = -12 mA | | 2.7 V | 2.2 | | | |
| | | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = -24 mA | | 3 V | 2.2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.7 | |
| | | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | | $V_I$ = 0.58 V | | 1.65 V | 25 | | | μA |
| | | $V_I$ = 1.07 V | | 1.65 V | -25 | | | |
| | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | |
| | | $V_I$ = 1.7 V | | 2.3 V | -45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | 3 V | -75 | | | |
| | | $V_I$ = 0 to 3.6 V(2) | | 3.6 V | | | ±500 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 80 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ - 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3 | | pF |
| | Data inputs | | | | | 6 | | |
| $C_o$ | Outputs | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 7 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | (1) | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | (1) | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before CLK↑ | (1) | | 2.1 | | 2.2 | | 1.9 | | ns |
| $t_h$ | Hold time, data after CLK↑ | (1) | | 0.6 | | 0.5 | | 0.5 | | ns |

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | (1) | | 150 | | 150 | | 150 | | MHz |
| $t_{pd}$ | CLK | Q | (1) | (1) | 1 | 5.3 | | 4.9 | 1 | 4.2 | ns |
| $t_{en}$ | $\overline{OE}$ | Q | (1) | (1) | 1 | 6.2 | | 5.9 | 1 | 4.8 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | (1) | (1) | 1 | 5.3 | | 4.7 | 1.2 | 4.3 | ns |

(1) This information was not available at the time of publication.

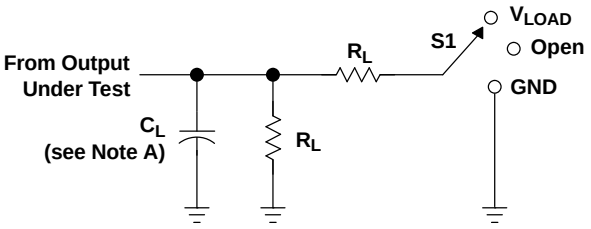
## OPERATING CHARACTERISTICS

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 10 MHz | (1) | 31 | 30 | pF |
| | | Outputs disabled | | (1) | 16 | 18 | |

(1) This information was not available at the time of publication.

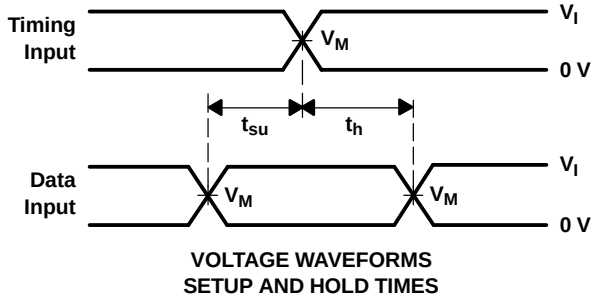
## PARAMETER MEASUREMENT INFORMATION



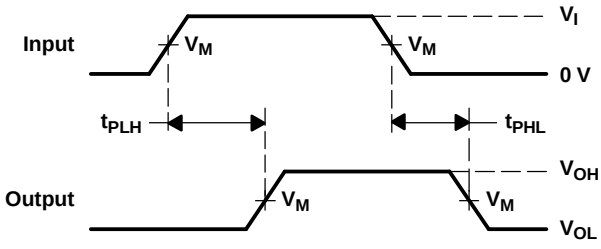

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

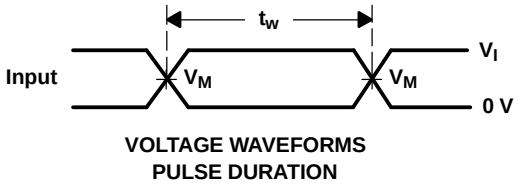
| $V_{CC}$ | INPUT | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



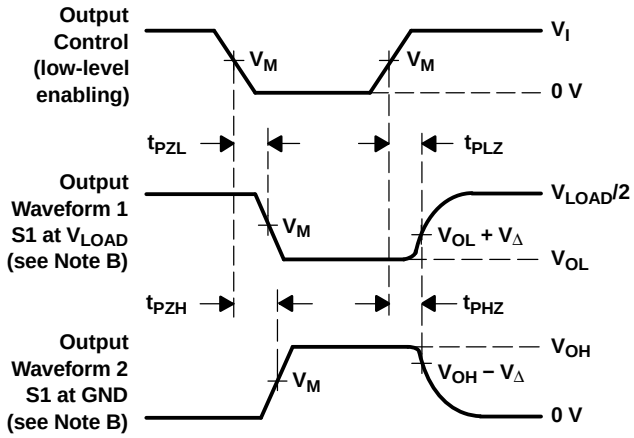

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74ALVCH32374ZKER | ACTIVE | LFBGA | ZKE | 96 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | ACH374 | Samples |
| SN74ALVCH32374GKE | OBSOLETE | LFBGA | GKE | 96 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74ALVCH32374KR | NRND | LFBGA | GKE | 96 | 1000 | TBD | SNPB | Level-2-235C-1 YEAR | -40 to 85 | ACH374 | |

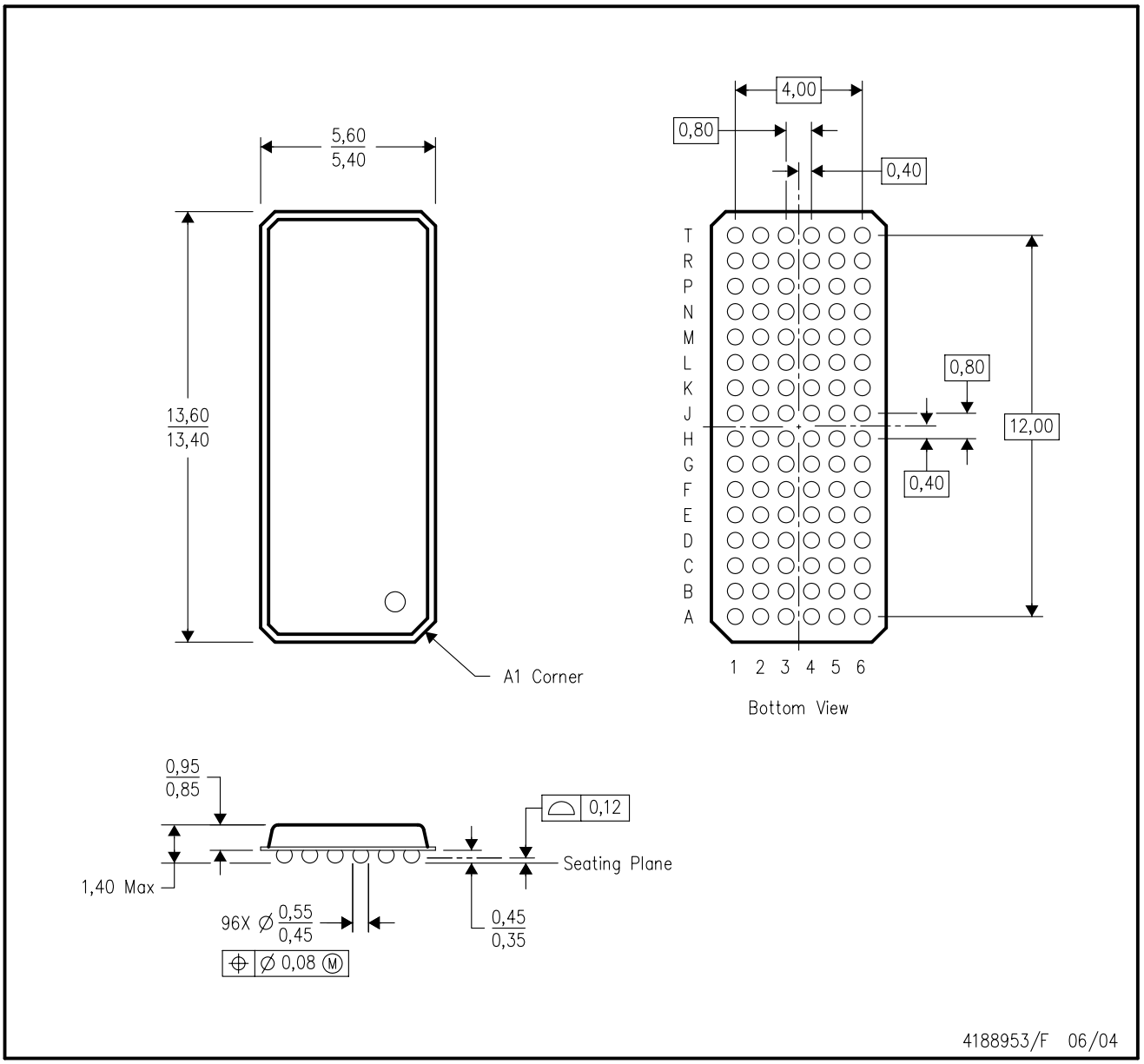
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

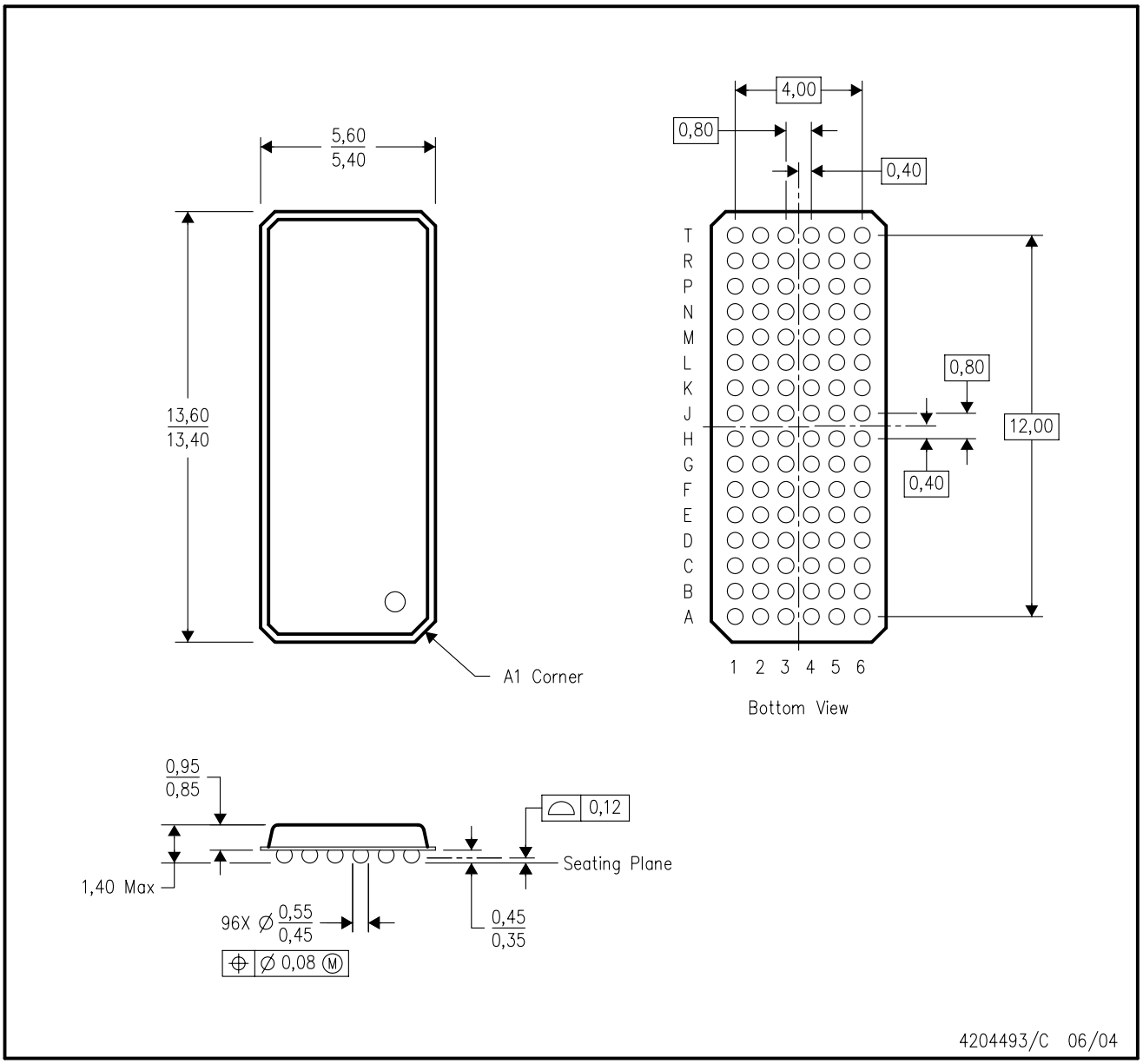
(4) Only one of markings shown within the brackets will appear on the physical device.

GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).

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|---|---|---|---|
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| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
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