

# SN54ALVTH32373, SN74ALVTH32373 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus+*™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- High Drive ( $-24/24$  mA at 2.5-V and  $-32/64$  mA at 3.3-V  $V_{CC}$ )
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds  $V_{CC} + 0.5$  V
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

NOTE: For tape and reel order entry:  
The GKER package is abbreviated to KR.

## description

The 'ALVTH32373 devices are 32-bit transparent D-type latches with 3-state outputs designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as four 8-bit latches, two 16-bit latches, or one 32-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

When  $V_{CC}$  is between 0 and 1.2 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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# SN54ALVTH32373, SN74ALVTH32373

## 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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#### description (continued)

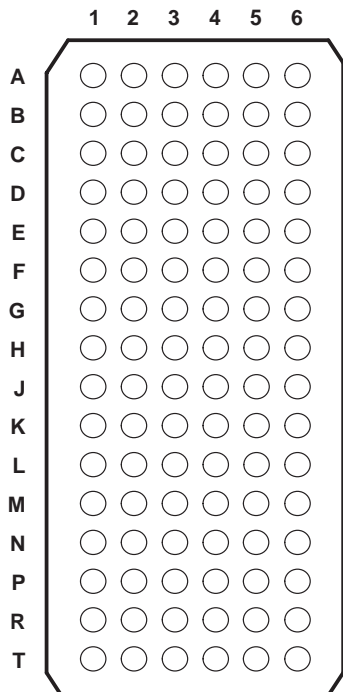
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH32373 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALVTH32373 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each 8-bit latch)

| INPUTS                 |    |   | OUTPUT |
|------------------------|----|---|--------|
| $\overline{\text{OE}}$ | LE | D | Q      |
| L                      | H  | H | H      |
| L                      | H  | L | L      |
| L                      | L  | X | $Q_0$  |
| H                      | X  | X | Z      |

GKE PACKAGE  
(TOP VIEW)



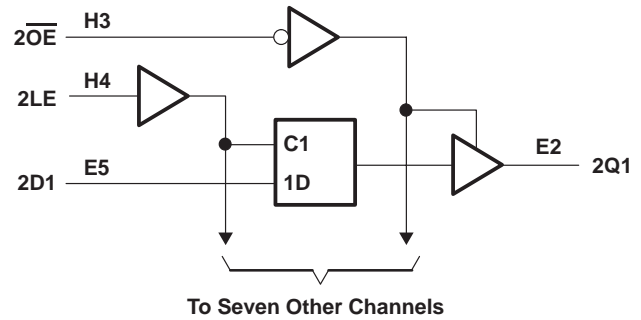
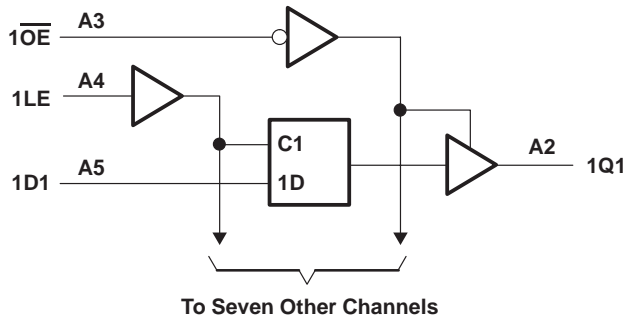
terminal assignments

|   | 1   | 2   | 3                       | 4         | 5   | 6   |
|---|-----|-----|-------------------------|-----------|-----|-----|
| A | 1Q2 | 1Q1 | $1\overline{\text{OE}}$ | 1LE       | 1D1 | 1D2 |
| B | 1Q4 | 1Q3 | GND                     | GND       | 1D3 | 1D4 |
| C | 1Q6 | 1Q5 | $1V_{CC}$               | $1V_{CC}$ | 1D5 | 1D6 |
| D | 1Q8 | 1Q7 | GND                     | GND       | 1D7 | 1D8 |
| E | 2Q2 | 2Q1 | GND                     | GND       | 2D1 | 2D2 |
| F | 2Q4 | 2Q3 | $1V_{CC}$               | $1V_{CC}$ | 2D3 | 2D4 |
| G | 2Q6 | 2Q5 | GND                     | GND       | 2D5 | 2D6 |
| H | 2Q7 | 2Q8 | $2\overline{\text{OE}}$ | 2LE       | 2D8 | 2D7 |
| J | 3Q2 | 3Q1 | $3\overline{\text{OE}}$ | 3LE       | 3D1 | 3D2 |
| K | 3Q4 | 3Q3 | GND                     | GND       | 3D3 | 3D4 |
| L | 3Q6 | 3Q5 | $2V_{CC}$               | $2V_{CC}$ | 3D5 | 3D6 |
| M | 3Q8 | 3Q7 | GND                     | GND       | 3D7 | 3D8 |
| N | 4Q2 | 4Q1 | GND                     | GND       | 4D1 | 4D2 |
| P | 4Q4 | 4Q3 | $2V_{CC}$               | $2V_{CC}$ | 4D3 | 4D4 |
| R | 4Q6 | 4Q5 | GND                     | GND       | 4D5 | 4D6 |
| T | 4Q7 | 4Q8 | $4\overline{\text{OE}}$ | 4LE       | 4D8 | 4D7 |

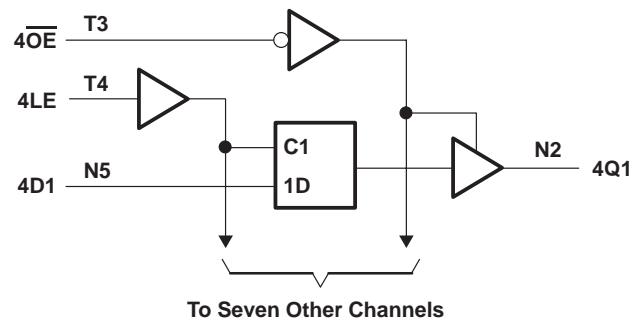
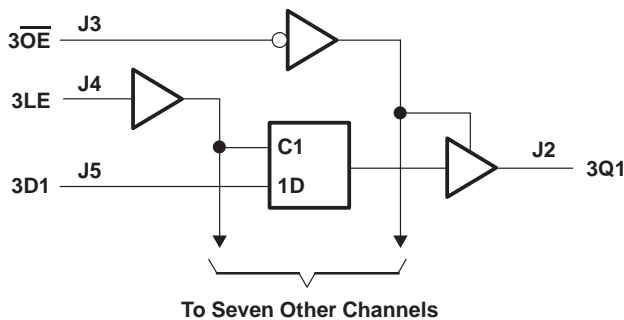
# SN54ALVTH32373, SN74ALVTH32373 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



NOTE A: 1V<sub>CC</sub> is associated with these channels.



NOTE B: 2V<sub>CC</sub> is associated with these channels.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                 |
|--|-----------------|
| Supply voltage range, V <sub>CC</sub> .....  | -0.5 V to 4.6 V |
| Input voltage range, V <sub>I</sub> (see Note 1) .....   | -0.5 V to 7 V   |
| Voltage range applied to any output in the high-impedance<br>or power-off state, V <sub>O</sub> (see Note 1) ..... | -0.5 V to 7 V   |
| Voltage range applied to any output in the high state, V <sub>O</sub> (see Note 1) .....                           | -0.5 V to 7 V   |
| Output current in the low state, I <sub>O</sub> : SN54ALVTH32373 .....   | 96 mA           |
| SN74ALVTH32373 .....   | 128 mA          |
| Output current in the high state, I <sub>O</sub> : SN54ALVTH32373 .....  | -48 mA          |
| SN74ALVTH32373 .....   | -64 mA          |
| Continuous current through V <sub>CC</sub> or GND .....  | ±100 mA         |
| Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0) .....  | -50 mA          |
| Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0) .....   | -50 mA          |
| Package thermal impedance, θ <sub>JA</sub> (see Note 2) .....  | 40°C/W          |
| Storage temperature range, T <sub>stg</sub> .....  | -65°C to 150°C  |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

# SN54ALVTH32373, SN74ALVTH32373

## 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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### recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

|                          |  | SN54ALVTH32373  |          |     | SN74ALVTH32373 |          |     | UNIT               |
|--------------------------|--|-----------------|----------|-----|----------------|----------|-----|--------------------|
|                          |  | MIN             | TYP      | MAX | MIN            | TYP      | MAX |                    |
| $V_{CC}$                 | Supply voltage   | 2.3             |          | 2.7 | 2.3            |          | 2.7 | V                  |
| $V_{IH}$                 | High-level input voltage   | 1.7             |          |     | 1.7            |          |     | V                  |
| $V_{IL}$                 | Low-level input voltage  |                 |          | 0.7 |                |          | 0.7 | V                  |
| $V_I$                    | Input voltage  | 0               | $V_{CC}$ | 5.5 | 0              | $V_{CC}$ | 5.5 | V                  |
| $I_{OH}$                 | High-level output current  |                 |          | -6  |                |          | -8  | mA                 |
| $I_{OL}$                 | Low-level output current   |                 |          | 6   |                |          | 8   | mA                 |
|                          | Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$ |                 |          | 18  |                |          | 24  |                    |
| $\Delta t/\Delta v$      | Input transition rise or fall rate   | Outputs enabled |          | 10  |                |          | 10  | ns/V               |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate   | 200             |          |     | 200            |          |     | $\mu\text{s/V}$    |
| $T_A$                    | Operating free-air temperature   | -55             |          | 125 | -40            |          | 85  | $^{\circ}\text{C}$ |

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

|                          |  | SN54ALVTH32373  |          |     | SN74ALVTH32373 |          |     | UNIT               |
|--------------------------|--|-----------------|----------|-----|----------------|----------|-----|--------------------|
|                          |  | MIN             | TYP      | MAX | MIN            | TYP      | MAX |                    |
| $V_{CC}$                 | Supply voltage   | 3               |          | 3.6 | 3              |          | 3.6 | V                  |
| $V_{IH}$                 | High-level input voltage   | 2               |          |     | 2              |          |     | V                  |
| $V_{IL}$                 | Low-level input voltage  |                 |          | 0.8 |                |          | 0.8 | V                  |
| $V_I$                    | Input voltage  | 0               | $V_{CC}$ | 5.5 | 0              | $V_{CC}$ | 5.5 | V                  |
| $I_{OH}$                 | High-level output current  |                 |          | -24 |                |          | -32 | mA                 |
| $I_{OL}$                 | Low-level output current   |                 |          | 24  |                |          | 32  | mA                 |
|                          | Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$ |                 |          | 48  |                |          | 64  |                    |
| $\Delta t/\Delta v$      | Input transition rise or fall rate   | Outputs enabled |          | 10  |                |          | 10  | ns/V               |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate   | 200             |          |     | 200            |          |     | $\mu\text{s/V}$    |
| $T_A$                    | Operating free-air temperature   | -55             |          | 125 | -40            |          | 85  | $^{\circ}\text{C}$ |

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54ALVTH32373, SN74ALVTH32373**  
**2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)**

| PARAMETER          |                | TEST CONDITIONS   | SN54ALVTH32373          |      |      | SN74ALVTH32373 |      |     | UNIT          |
|--------------------|----------------|---|-------------------------|------|------|----------------|------|-----|---------------|
|                    |                |   | MIN                     | TYP† | MAX  | MIN            | TYP† | MAX |               |
| $V_{IK}$           |                | $V_{CC} = 2.3\text{ V}$ ,<br>$I_I = -18\text{ mA}$  | -1.2                    |      |      | -1.2           |      |     | V             |
| $V_{OH}$           |                | $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ ,<br>$I_{OH} = -100\text{ }\mu\text{A}$  | $V_{CC}-0.2$            |      |      | $V_{CC}-0.2$   |      |     | V             |
|                    |                | $V_{CC} = 2.3\text{ V}$   | 1.8                     |      |      | 1.8            |      |     |               |
| $V_{OL}$           |                | $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ ,<br>$I_{OL} = 100\text{ }\mu\text{A}$   | 0.2                     |      |      | 0.2            |      |     | V             |
|                    |                | $V_{CC} = 2.3\text{ V}$   | $I_{OL} = 6\text{ mA}$  |      |      | 0.4            |      |     |               |
|                    |                |   | $I_{OL} = 8\text{ mA}$  |      |      | 0.4            |      |     |               |
|                    |                |   | $I_{OL} = 18\text{ mA}$ |      |      | 0.5            |      |     |               |
|                    |                |   | $I_{OL} = 24\text{ mA}$ |      |      | 0.5            |      |     |               |
| $I_I$              | Control inputs | $V_{CC} = 2.7\text{ V}$ ,<br>$V_I = V_{CC}$ or GND  | $\pm 1$                 |      |      | $\pm 1$        |      |     | $\mu\text{A}$ |
|                    |                | $V_{CC} = 0$ or $2.7\text{ V}$ ,<br>$V_I = 5.5\text{ V}$  | 10                      |      |      | 10             |      |     |               |
|                    | Data inputs    | $V_{CC} = 2.7\text{ V}$   | $V_I = 5.5\text{ V}$    |      |      | 10             |      |     |               |
|                    |                |   | $V_I = V_{CC}$          |      |      | 1              |      |     |               |
|                    |                |   | $V_I = 0$               |      |      | -5             |      |     |               |
| $I_{off}$          |                | $V_{CC} = 0$ ,<br>$V_I$ or $V_O = 0$ to $4.5\text{ V}$  |                         |      |      | $\pm 100$      |      |     | $\mu\text{A}$ |
| $I_{BHL}^\ddagger$ |                | $V_{CC} = 2.3\text{ V}$ ,<br>$V_I = 0.7\text{ V}$   | 115*                    |      |      | 115            |      |     | $\mu\text{A}$ |
| $I_{BHH}^\S$       |                | $V_{CC} = 2.3\text{ V}$ ,<br>$V_I = 1.7\text{ V}$   | -10*                    |      |      | -10            |      |     | $\mu\text{A}$ |
| $I_{BHLO}^\P$      |                | $V_{CC} = 2.7\text{ V}$ ,<br>$V_I = 0$ to $V_{CC}$  | 300*                    |      |      | 300            |      |     | $\mu\text{A}$ |
| $I_{BHHO}^\#$      |                | $V_{CC} = 2.7\text{ V}$ ,<br>$V_I = 0$ to $V_{CC}$  | -300*                   |      |      | -300           |      |     | $\mu\text{A}$ |
| $I_{EX}^\parallel$ |                | $V_{CC} = 2.3\text{ V}$ ,<br>$V_O = 5.5\text{ V}$   | 125                     |      |      | 125            |      |     | $\mu\text{A}$ |
| $I_{OZ(PU/PD)}^*$  |                | $V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V to } V_{CC}$ ,<br>$V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$ | $\pm 100$               |      |      | $\pm 100$      |      |     | $\mu\text{A}$ |
| $I_{OZH}$          |                | $V_{CC} = 2.7\text{ V}$<br>$V_O = 2.3\text{ V}$ ,<br>$V_I = 0.7\text{ V or } 1.7\text{ V}$  | 5                       |      |      | 5              |      |     | $\mu\text{A}$ |
| $I_{OZL}$          |                | $V_{CC} = 2.7\text{ V}$<br>$V_O = 0.5\text{ V}$ ,<br>$V_I = 0.7\text{ V or } 1.7\text{ V}$  | -5                      |      |      | -5             |      |     | $\mu\text{A}$ |
| $I_{CC}$           |                | $V_{CC} = 2.7\text{ V}$ ,<br>$I_O = 0$ ,<br>$V_I = V_{CC}$ or GND   | Outputs high            |      | 0.04 | 0.1            | 0.04 | 0.1 | mA            |
|                    |                |   | Outputs low             |      | 2.3  | 4.5            | 2.3  | 4.5 |               |
|                    |                |   | Outputs disabled        |      | 0.04 | 0.1            | 0.04 | 0.1 |               |
| $C_i$              |                | $V_{CC} = 2.5\text{ V}$ ,<br>$V_I = 2.5\text{ V or } 0$   | 3.5                     |      |      | 3.5            |      |     | pF            |
| $C_o$              |                | $V_{CC} = 2.5\text{ V}$ ,<br>$V_O = 2.5\text{ V or } 0$   | 6                       |      |      | 6              |      |     | pF            |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

\* High-impedance state during power up or power down

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electrical characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS  |  | SN54ALVTH32373           |      |      | SN74ALVTH32373       |      |     | UNIT |
|--------------------------|--|--|--------------------------|------|------|----------------------|------|-----|------|
|                          |  |  | MIN                      | TYP† | MAX  | MIN                  | TYP† | MAX |      |
| V <sub>IK</sub>          | V <sub>CC</sub> = 3 V, I <sub>I</sub> = -18 mA   |  | -1.2                     |      |      | -1.2                 |      |     | V    |
| V <sub>OH</sub>          | V <sub>CC</sub> = 3 V to 3.6 V, I <sub>OH</sub> = -100 μA  |  | V <sub>CC</sub> -0.2     |      |      | V <sub>CC</sub> -0.2 |      |     | V    |
|                          | V <sub>CC</sub> = 3 V  | I <sub>OH</sub> = -24 mA   | 2                        |      |      |                      |      |     |      |
|                          |  |  | I <sub>OH</sub> = -32 mA |      |      |                      | 2    |     |      |
| V <sub>OL</sub>          | V <sub>CC</sub> = 3 V to 3.6 V, I <sub>OL</sub> = 100 μA   |  | 0.2                      |      |      | 0.2                  |      |     | V    |
|                          | V <sub>CC</sub> = 3 V  | I <sub>OL</sub> = 16 mA  |                          |      |      | 0.4                  |      |     |      |
|                          |  | I <sub>OL</sub> = 24 mA  | 0.5                      |      |      |                      |      |     |      |
|                          |  | I <sub>OL</sub> = 32 mA  |                          |      |      | 0.5                  |      |     |      |
|                          |  | I <sub>OL</sub> = 48 mA  | 0.55                     |      |      |                      |      |     |      |
|                          |  | I <sub>OL</sub> = 64 mA  |                          |      |      | 0.55                 |      |     |      |
| I <sub>I</sub>           | Control inputs   | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND | ±1                       |      |      | ±1                   |      |     | μA   |
|                          |  | V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V             | 10                       |      |      | 10                   |      |     |      |
|                          | Data inputs  | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 5.5 V                  | 10                       |      |      | 10                   |      |     |      |
|                          |  | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub>        | 1                        |      |      | 1                    |      |     |      |
|                          |  | V <sub>I</sub> = 0   | -5                       |      |      | -5                   |      |     |      |
| I <sub>off</sub>         | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V   |  |                          |      |      | ±100                 |      |     | μA   |
| I <sub>BHL</sub> ‡       | V <sub>CC</sub> = 3 V, V <sub>I</sub> = 0.8 V  |  | 75*                      |      |      | 75                   |      |     | μA   |
| I <sub>BHH</sub> §       | V <sub>CC</sub> = 3 V, V <sub>I</sub> = 2 V  |  | -75*                     |      |      | -75                  |      |     | μA   |
| I <sub>BHLO</sub> ¶      | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 to V <sub>CC</sub>   |  | 500*                     |      |      | 500                  |      |     | μA   |
| I <sub>BHHO</sub> #      | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 to V <sub>CC</sub>   |  | -500*                    |      |      | -500                 |      |     | μA   |
| I <sub>EX</sub>          | V <sub>CC</sub> = 3 V, V <sub>O</sub> = 5.5 V  |  | 125                      |      |      | 125                  |      |     | μA   |
| I <sub>OZ</sub> (PU/PD)* | V <sub>CC</sub> ≤ 1.2 V, V <sub>O</sub> = 0.5 V to V <sub>CC</sub> , V <sub>I</sub> = GND or V <sub>CC</sub> , OE = don't care |  | ±100                     |      |      | ±100                 |      |     | μA   |
| I <sub>OZH</sub>         | V <sub>CC</sub> = 3.6 V  | V <sub>O</sub> = 3 V, V <sub>I</sub> = 0.8 V or 2 V              | 5                        |      |      | 5                    |      |     | μA   |
| I <sub>OZL</sub>         | V <sub>CC</sub> = 3.6 V  | V <sub>O</sub> = 0.5 V, V <sub>I</sub> = 0.8 V or 2 V            | -5                       |      |      | -5                   |      |     | μA   |
| I <sub>CC</sub>          | V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND   |  | Outputs high             |      | 0.07 | 0.1                  | 0.07 | 0.1 | mA   |
|                          |  |  | Outputs low              |      | 3.2  | 5                    | 3.2  | 5   |      |
|                          |  |  | Outputs disabled         |      | 0.07 | 0.1                  | 0.07 | 0.1 |      |
| ΔI <sub>CC</sub> □       | V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND                   |  | 0.4                      |      |      | 0.4                  |      |     | mA   |
| C <sub>i</sub>           | V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 3.3 V or 0   |  | 3.5                      |      |      | 3.5                  |      |     | pF   |
| C <sub>o</sub>           | V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = 3.3 V or 0   |  | 6                        |      |      | 6                    |      |     | pF   |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

¶ An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

# An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

|| Current into an output in the high state when V<sub>O</sub> > V<sub>CC</sub>

\* High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



**SN54ALVTH32373, SN74ALVTH32373**  
**2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

|          |                             | SN54ALVTH32373 |     | SN74ALVTH32373 |     | UNIT |
|----------|-----------------------------|----------------|-----|----------------|-----|------|
|          |                             | MIN            | MAX | MIN            | MAX |      |
| $t_w$    | Pulse duration, LE high     | 1.5            |     | 1.5            |     | ns   |
| $t_{su}$ | Setup time, data before LE↓ | Data high      | 1.1 | 1              |     | ns   |
|          |                             | Data low       | 1.6 | 1.5            |     |      |
| $t_h$    | Hold time, data after LE↓   | Data high      | 1   | 0.9            |     | ns   |
|          |                             | Data low       | 1.6 | 1.5            |     |      |

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 2)**

|          |                             | SN54ALVTH32373 |     | SN74ALVTH32373 |     | UNIT |
|----------|-----------------------------|----------------|-----|----------------|-----|------|
|          |                             | MIN            | MAX | MIN            | MAX |      |
| $t_w$    | Pulse duration, LE high     | 1.5            |     | 1.5            |     | ns   |
| $t_{su}$ | Setup time, data before LE↓ | Data high      | 1.5 | 1.4            |     | ns   |
|          |                             | Data low       | 1.6 | 0.9            |     |      |
| $t_h$    | Hold time, data after LE↓   | Data high      | 1   | 0.9            |     | ns   |
|          |                             | Data low       | 1.5 | 1.4            |     |      |

**switching characteristics over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$ ,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | SN54ALVTH32373 |     | SN74ALVTH32373 |     | UNIT |
|-----------|-----------------|-------------|----------------|-----|----------------|-----|------|
|           |                 |             | MIN            | MAX | MIN            | MAX |      |
| $t_{PLH}$ | D               | Q           | 1              | 3.4 | 1              | 3.3 | ns   |
| $t_{PHL}$ |                 |             | 1              | 4.3 | 1              | 4.2 |      |
| $t_{PLH}$ | LE              | Q           | 1.4            | 3.9 | 1.5            | 3.8 | ns   |
| $t_{PHL}$ |                 |             | 1.4            | 4.6 | 1.5            | 4.5 |      |
| $t_{PZH}$ | $\overline{OE}$ | Q           | 1.7            | 4.4 | 1.8            | 4.3 | ns   |
| $t_{PZL}$ |                 |             | 1.4            | 4.1 | 1.5            | 4   |      |
| $t_{PHZ}$ | $\overline{OE}$ | Q           | 1.4            | 4.7 | 1.5            | 4.6 | ns   |
| $t_{PLZ}$ |                 |             | 1              | 3.7 | 1              | 3.6 |      |

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 2)**

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | SN54ALVTH32373 |     | SN74ALVTH32373 |     | UNIT |
|-----------|-----------------|-------------|----------------|-----|----------------|-----|------|
|           |                 |             | MIN            | MAX | MIN            | MAX |      |
| $t_{PLH}$ | D               | Q           | 1              | 3.2 | 1              | 3.1 | ns   |
| $t_{PHL}$ |                 |             | 1              | 3.4 | 1              | 3.3 |      |
| $t_{PLH}$ | LE              | Q           | 1              | 3.4 | 1              | 3.3 | ns   |
| $t_{PHL}$ |                 |             | 1              | 3.6 | 1              | 3.5 |      |
| $t_{PZH}$ | $\overline{OE}$ | Q           | 1.3            | 4.1 | 1.4            | 4   | ns   |
| $t_{PZL}$ |                 |             | 1              | 3.5 | 1              | 3.4 |      |
| $t_{PHZ}$ | $\overline{OE}$ | Q           | 1.4            | 5   | 1.5            | 4.9 | ns   |
| $t_{PLZ}$ |                 |             | 1.4            | 4.6 | 1.5            | 4.5 |      |

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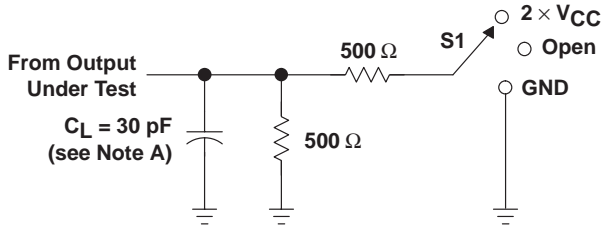


**SN54ALVTH32373, SN74ALVTH32373**  
**2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

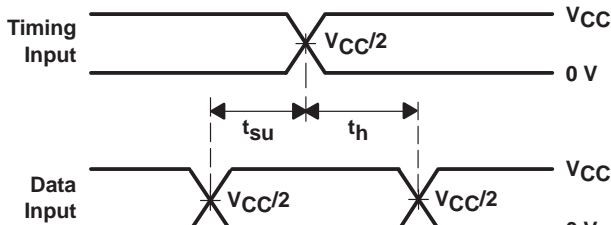
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

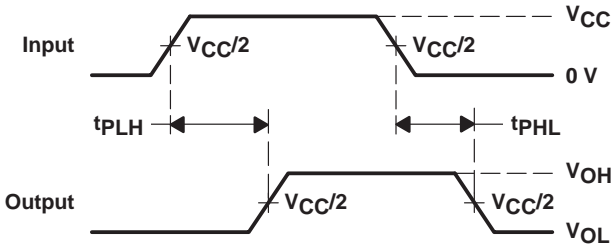


**LOAD CIRCUIT**

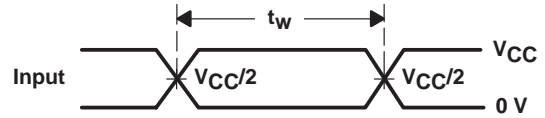
| TEST              | S1                  |
|-------------------|---------------------|
| $t_{PLH}/t_{PHL}$ | Open                |
| $t_{PLZ}/t_{PZL}$ | 2 $\times$ $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND                 |



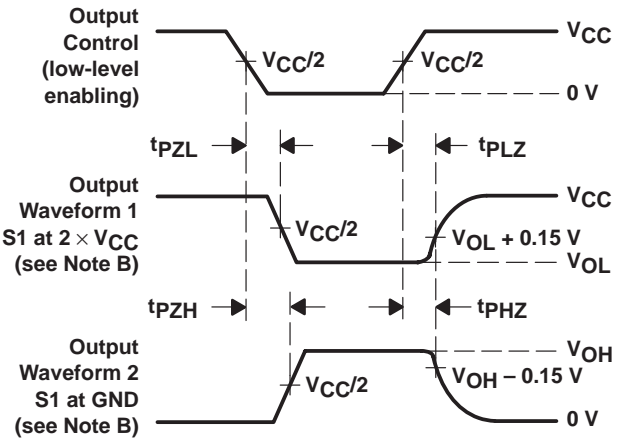
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

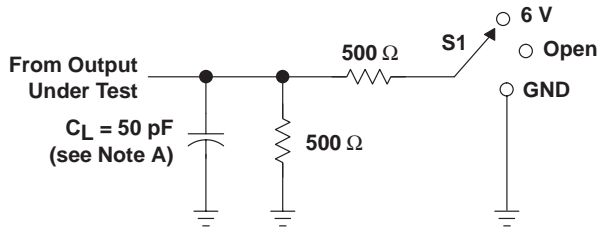


SN54ALVTH32373, SN74ALVTH32373  
2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES  
WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

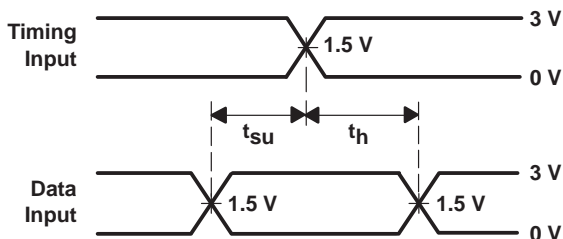
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

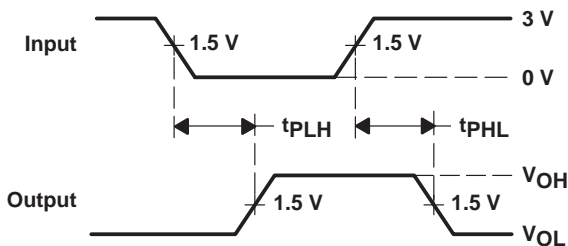


LOAD CIRCUIT

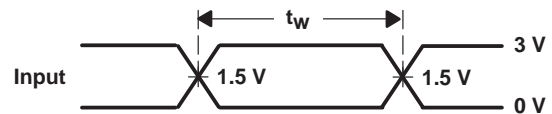
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



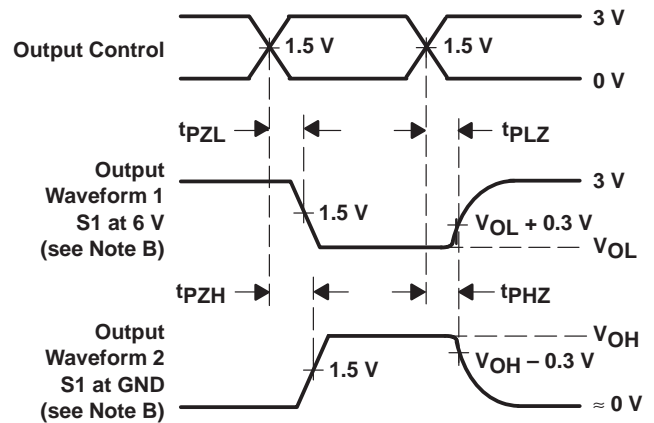
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---------|
| 74ALVTH32373ZKER | ACTIVE        | LFBGA        | ZKE             | 96   | 1000        | Green (RoHS & no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  | -40 to 85    | VL373                    | Samples |
| SN74ALVTH32373KR | NRND          | LFBGA        | GKE             | 96   | 1000        | TBD                     | SNPB             | Level-2-235C-1 YEAR  | -40 to 85    | VL373                    |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



4188953/F 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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