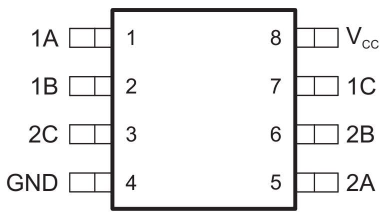
SN74LVC2G66 DUAL BILATERAL ANALOG SWITCH

FEATURES

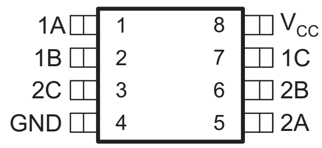
- **Available in the Texas Instruments NanoFree™ Package**
- **1.65-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 0.8 ns at 3.3 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)**
- **Rail-to-Rail Input/Output**
- **Low On-State Resistance, Typically ≈6 Ω (V_{CC} = 4.5 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DCT PACKAGE
(TOP VIEW)

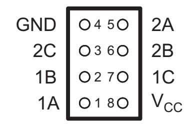


See mechanical drawings for dimensions.

DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



DESCRIPTION/ORDERING INFORMATION

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

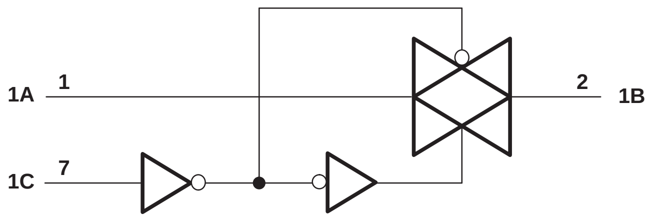
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC2G66YZPR	_ _ _C6_
	SSOP – DCT	Reel of 3000	SN74LVC2G66DCTR	C66_ _ _
	VSSOP – DCU	Reel of 3000	SN74LVC2G66DCUR	C66_
		Reel of 250	SN74LVC2G66DCUT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE (EACH SECTION)

CONTROL INPUT (C)	SWITCH
L	Off
H	On

LOGIC DIAGRAM, EACH SWITCH (POSITIVE LOGIC)



One of Two Switches

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		–0.5	6.5	V
V_I	Input voltage range[2][3]		–0.5	6.5	V
V_O	Switch I/O voltage range[2][3][4]		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	$V_I < 0$		–50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		–50	mA
I_T	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[5]	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.65		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		V_{CC} × 0.35	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
Δt/Δv	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	On-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.65 V		12.5	30	Ω
			I_S = 8 mA	2.3 V		9	20	
			I_S = 24 mA	3 V		7.5	15	
			I_S = 32 mA	4.5 V		6	10	
$r_{on(p)}$	Peak on-state resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.65 V		85	120(1)	Ω
			I_S = 8 mA	2.3 V		22	30(1)	
			I_S = 24 mA	3 V		12	20	
			I_S = 32 mA	4.5 V		7.5	15	
Δr_{on}	Difference of on-state resistance between switches	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.65 V			7	Ω
			I_S = 8 mA	2.3 V			5	
			I_S = 24 mA	3 V			3	
			I_S = 32 mA	4.5 V			2	
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 3)		5.5 V			±1	μA
							±0.1(1)	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see Figure 4)		5.5 V			±1	μA
							±0.1(1)	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5 V			±1	μA
							±0.1(1)	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5 V			10	μA
							1(1)	
ΔI_{CC}	Supply-current change	$V_C = V_{CC} – 0.6$ V		5.5 V			500	μA
C_{ic}	Control input capacitance			5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance			5 V		6		pF
$C_{io(on)}$	Switch input/output capacitance			5 V		14		pF

(1) T_A = 25°C

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}(1)	A or B	B or A		2		1.2		0.8		0.6	ns
t_{en}(2)	C	A or B	2.3	10	1.6	5.6	1.5	4.4	1.3	3.9	ns
t_{dis}(3)	C	A or B	2.5	10.5	1.2	6.9	2	7.2	1.1	6.3	ns

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{PZL} and t_{PZH} are the same as t_{en}.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk(1) (between switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	–58	dB
				2.3 V	–58	
				3 V	–58	
				4.5 V	–58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	–42	
				2.3 V	–42	
				3 V	–42	
				4.5 V	–42	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feedthrough attenuation (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	–58	dB
				2.3 V	–58	
				3 V	–58	
				4.5 V	–58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	–42	
				2.3 V	–42	
				3 V	–42	
				4.5 V	–42	
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15	
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

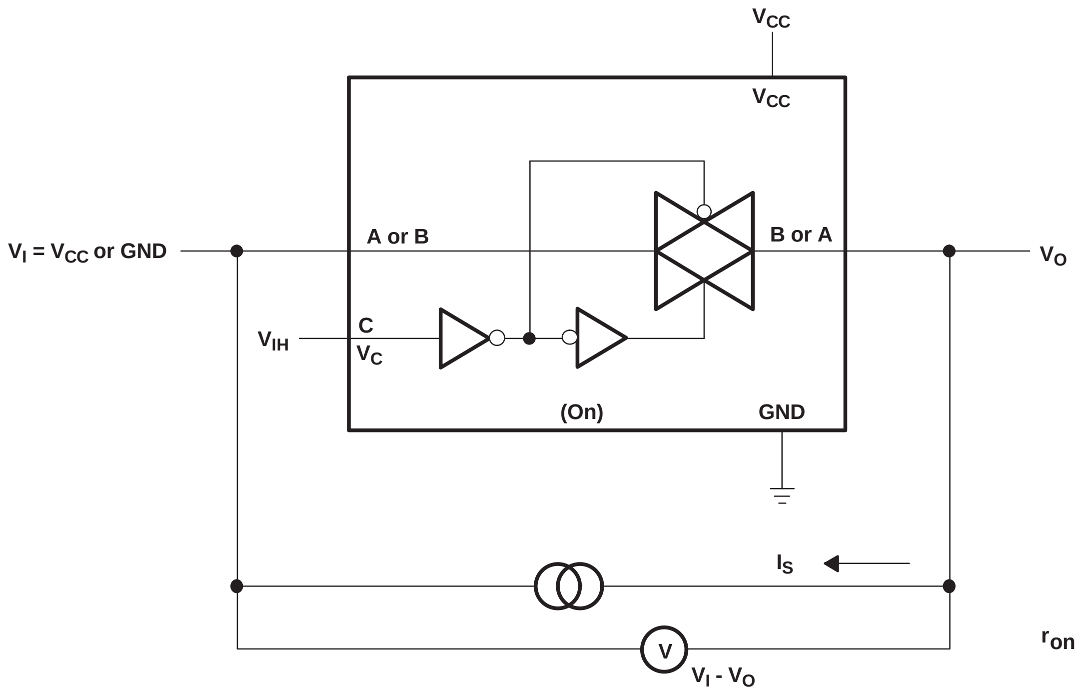
(1) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	8	9	9.5	11	pF

PARAMETER MEASUREMENT INFORMATION



$$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$$

Figure 1. On-State Resistance Test Circuit

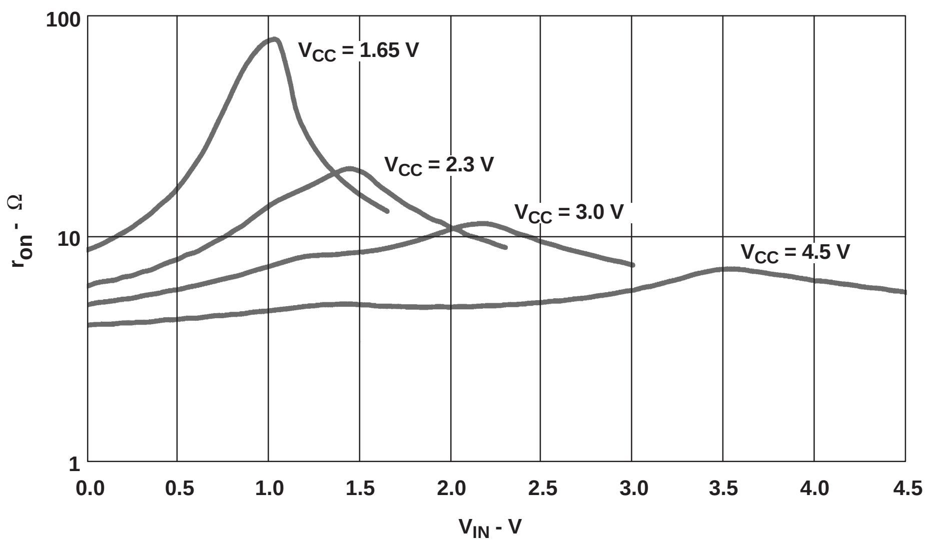


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION

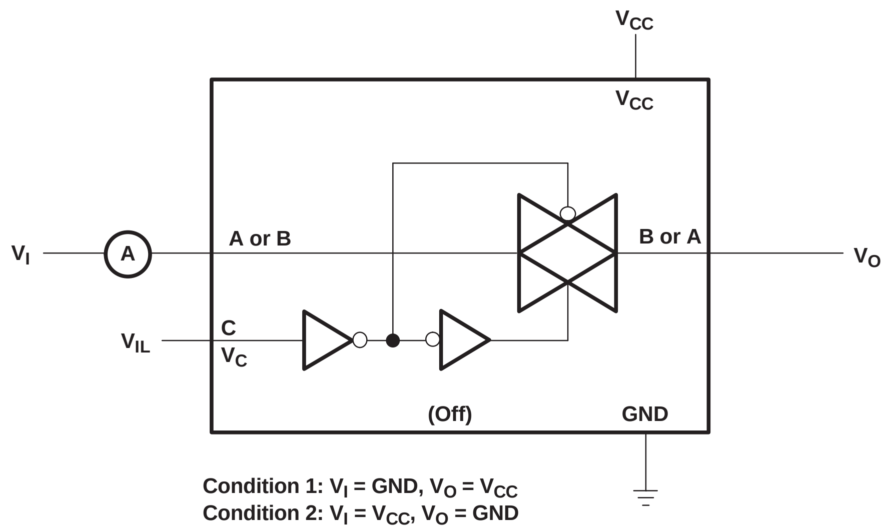


Figure 3. Off-State Switch Leakage-Current Test Circuit

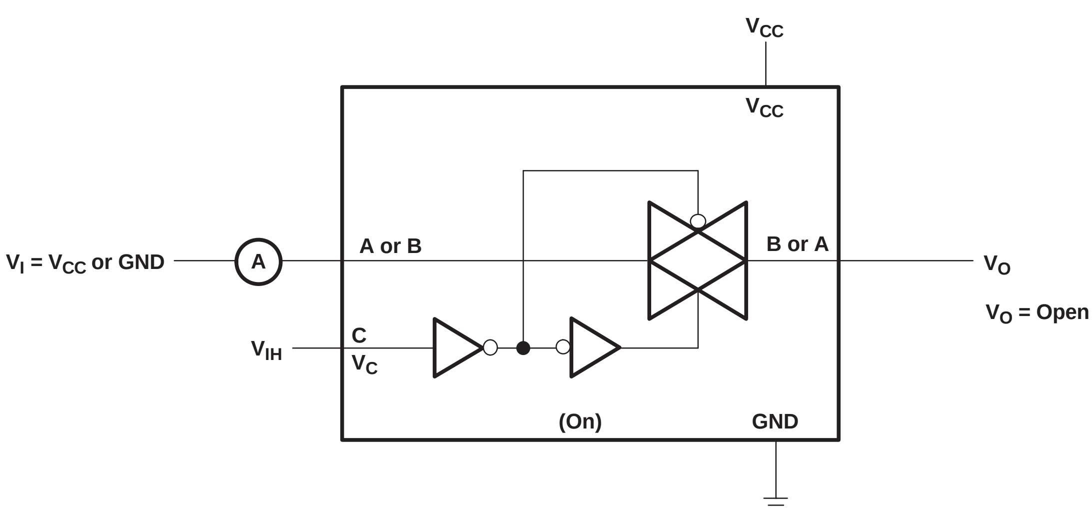
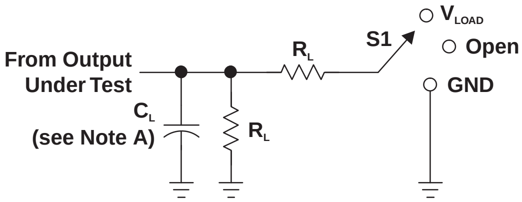


Figure 4. On-State Leakage-Current Test Circuit

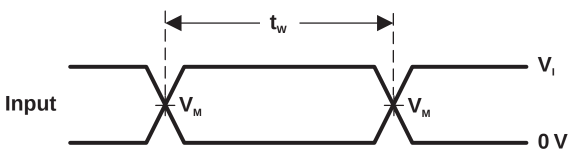
PARAMETER MEASUREMENT INFORMATION



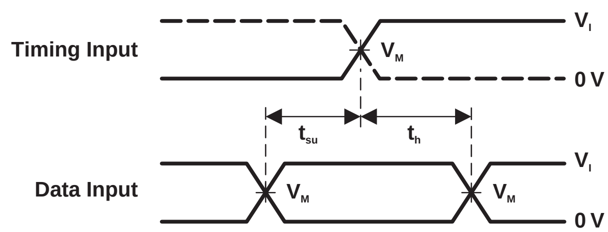
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

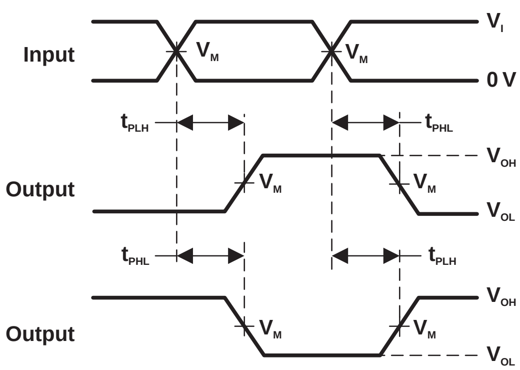
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



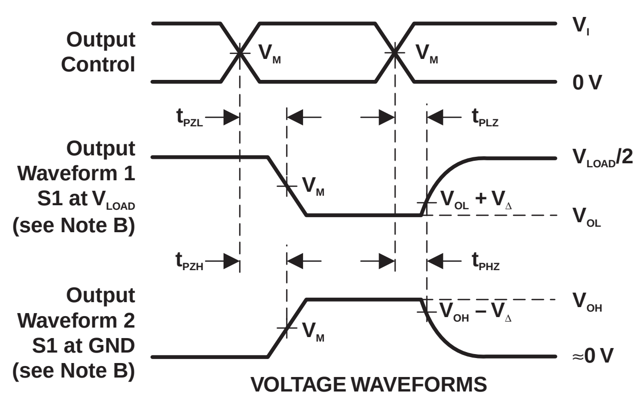
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

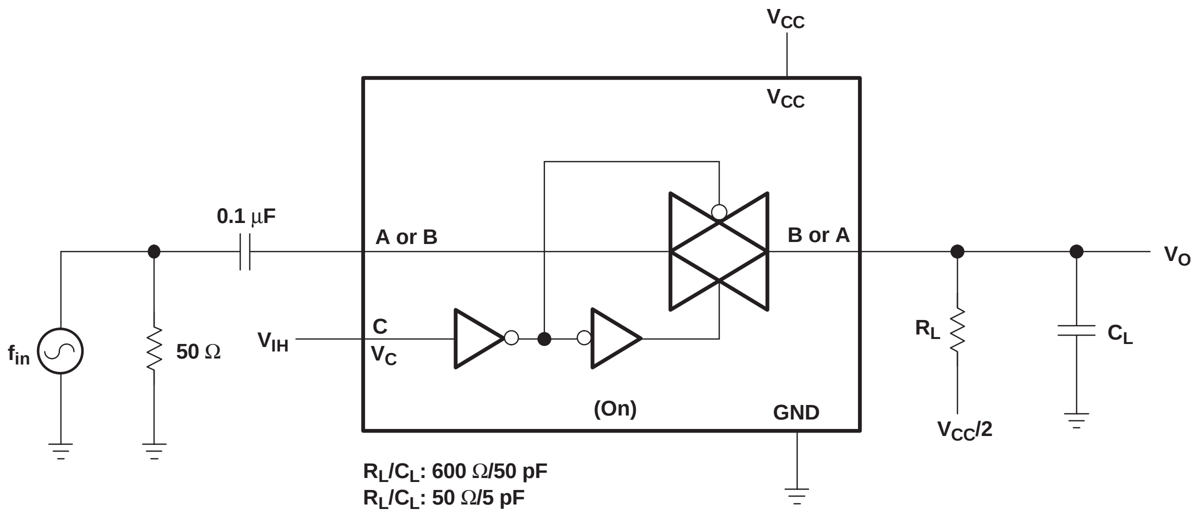


Figure 6. Frequency Response (Switch On)

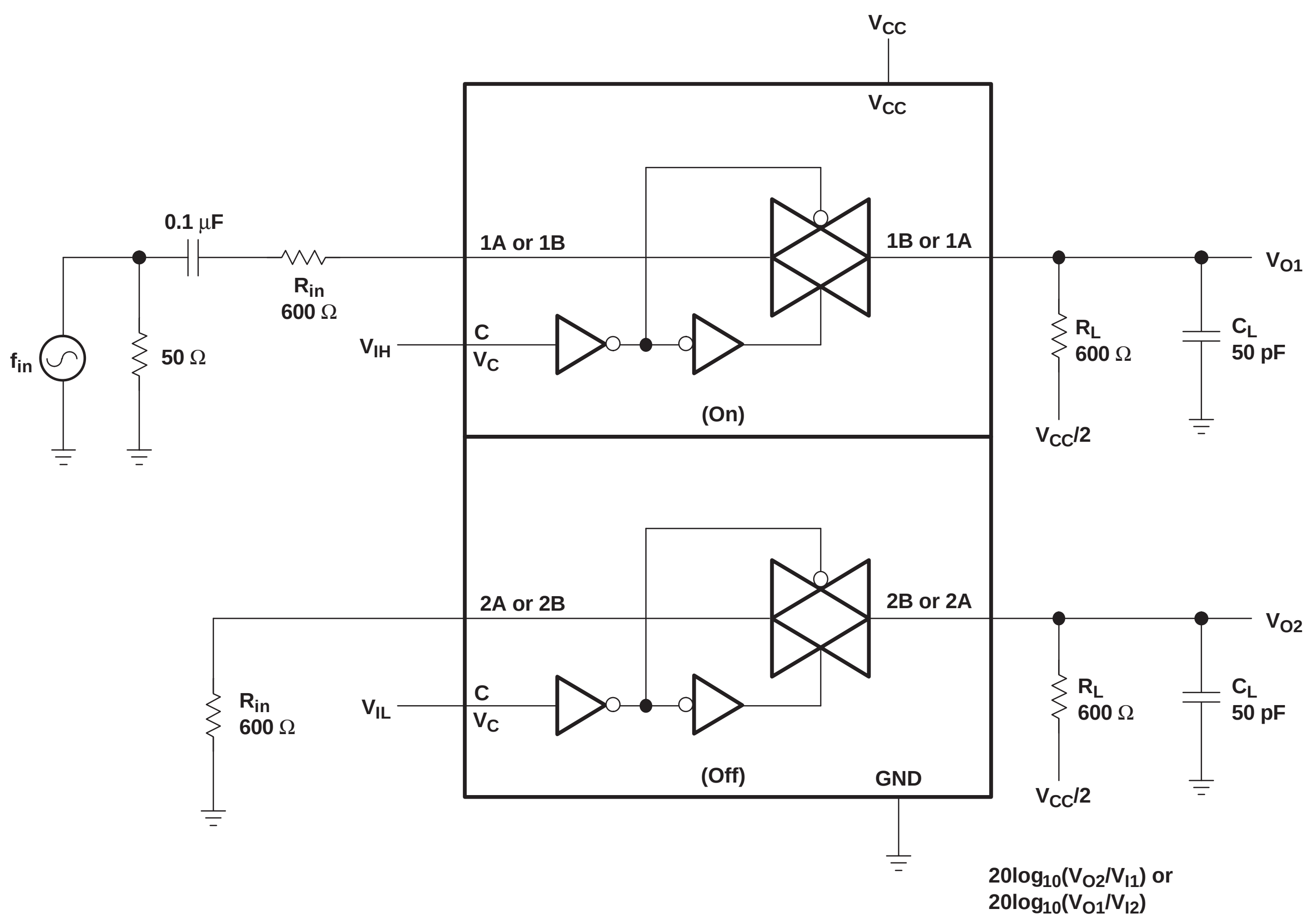


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

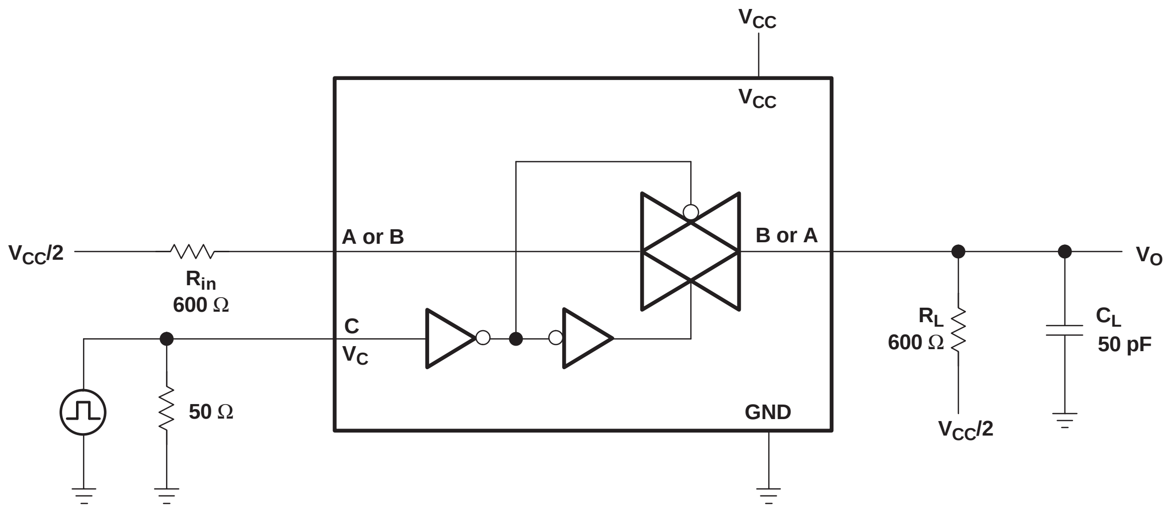


Figure 8. Crosstalk (Control Input, Switch Output)

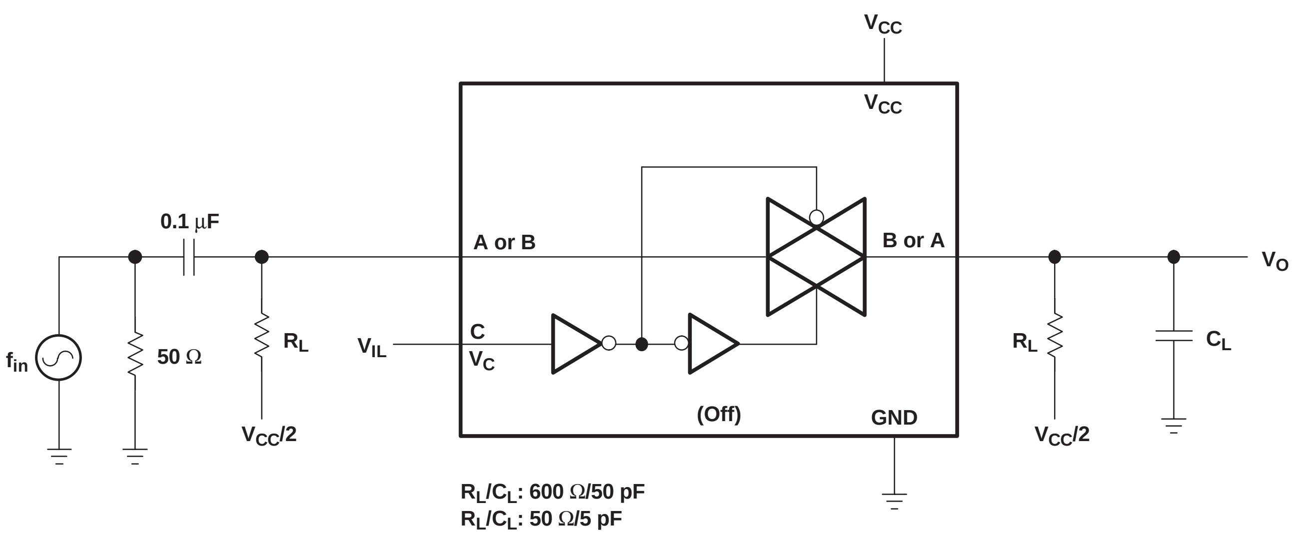
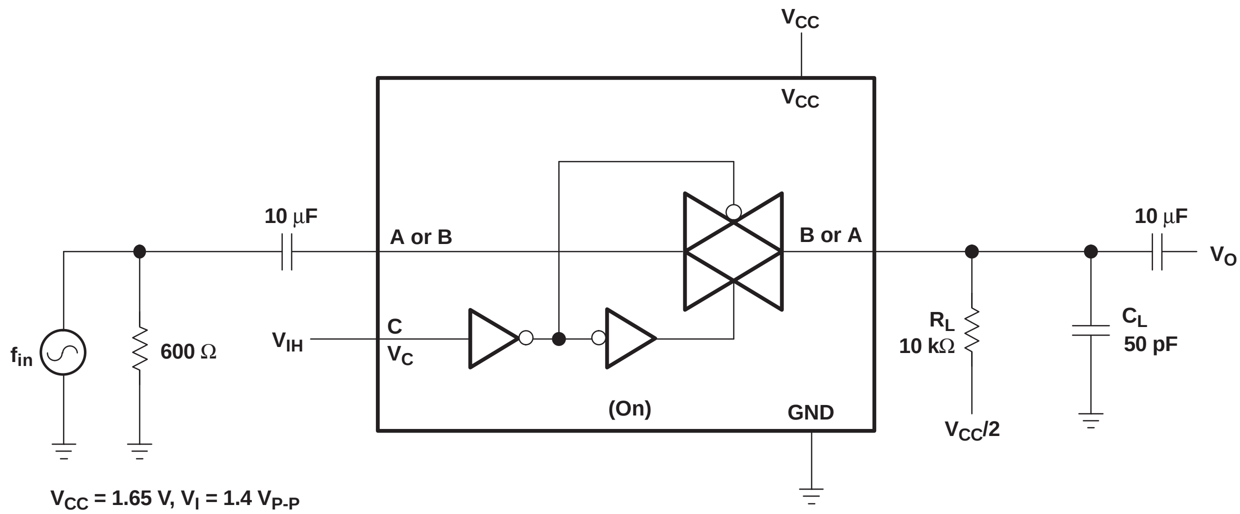


Figure 9. Feedthrough (Switch Off)

PARAMETER MEASUREMENT INFORMATION



V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.3 V, V_I = 2 V_{P-P}
V_{CC} = 3 V, V_I = 2.5 V_{P-P}
V_{CC} = 4.5 V, V_I = 4 V_{P-P}

Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC2G66DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66 Z	Samples
SN74LVC2G66DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66 Z	Samples
SN74LVC2G66DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66 Z	Samples
SN74LVC2G66DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	(66 ~ C66R) CZ	Samples
SN74LVC2G66DCURE4	ACTIVE	US8	DCU	8		TBD	Call TI	Call TI	-40 to 85		Samples
SN74LVC2G66DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R	Samples
SN74LVC2G66DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R	Samples
SN74LVC2G66DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R	Samples
SN74LVC2G66DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C66R	Samples
SN74LVC2G66YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(C62 ~ C67 ~ C6N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G66 :

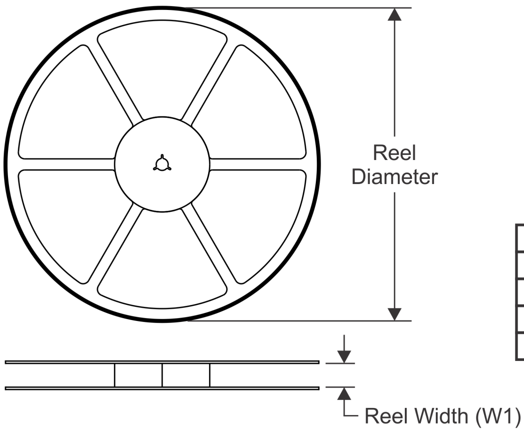
- Automotive: SN74LVC2G66-Q1

NOTE: Qualified Version Definitions:

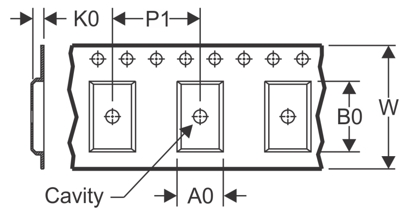
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

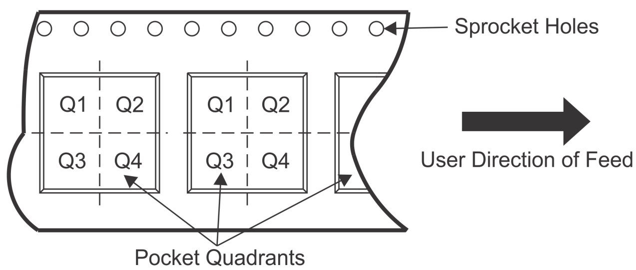


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

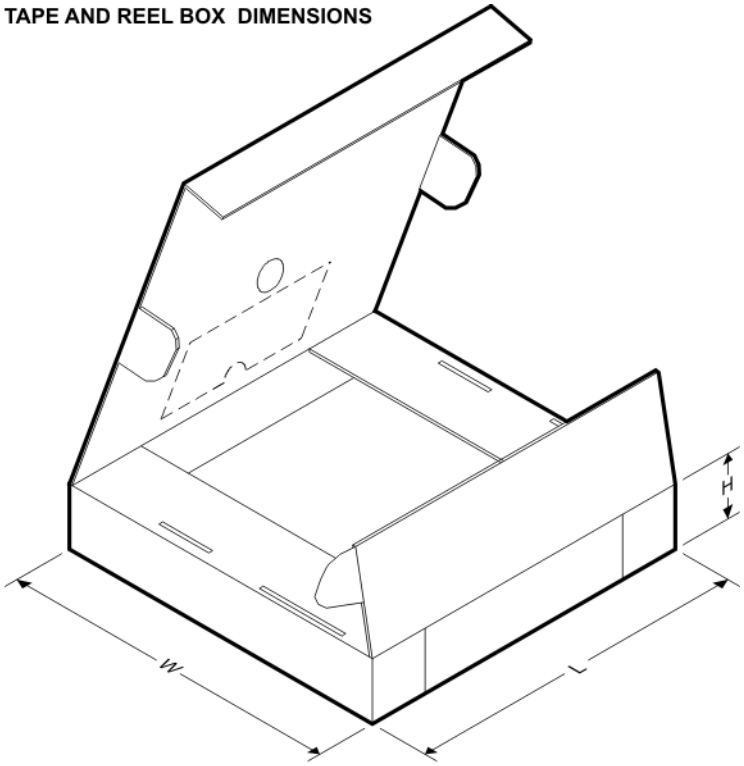
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G66DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G66DCURG4	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G66YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

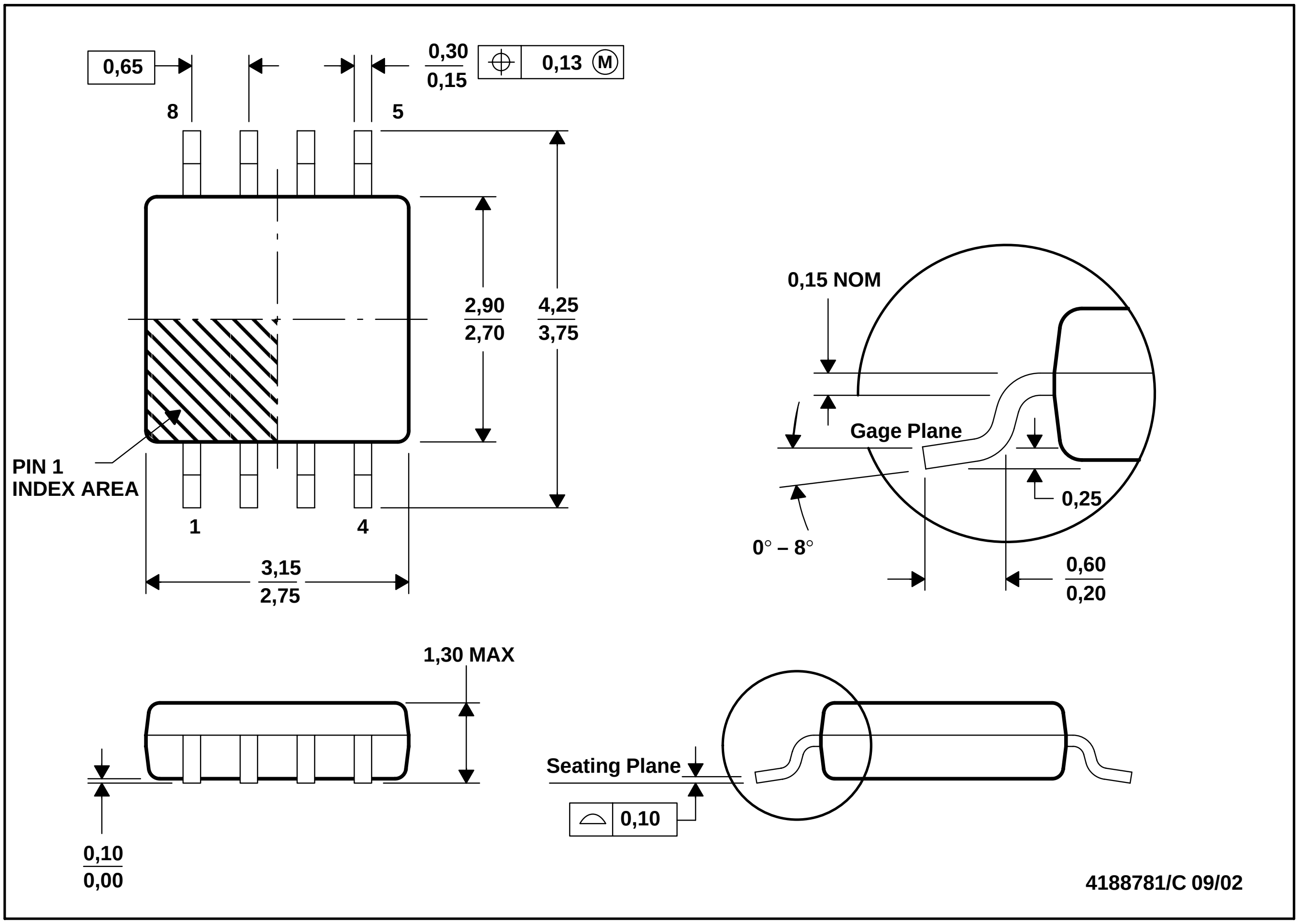
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

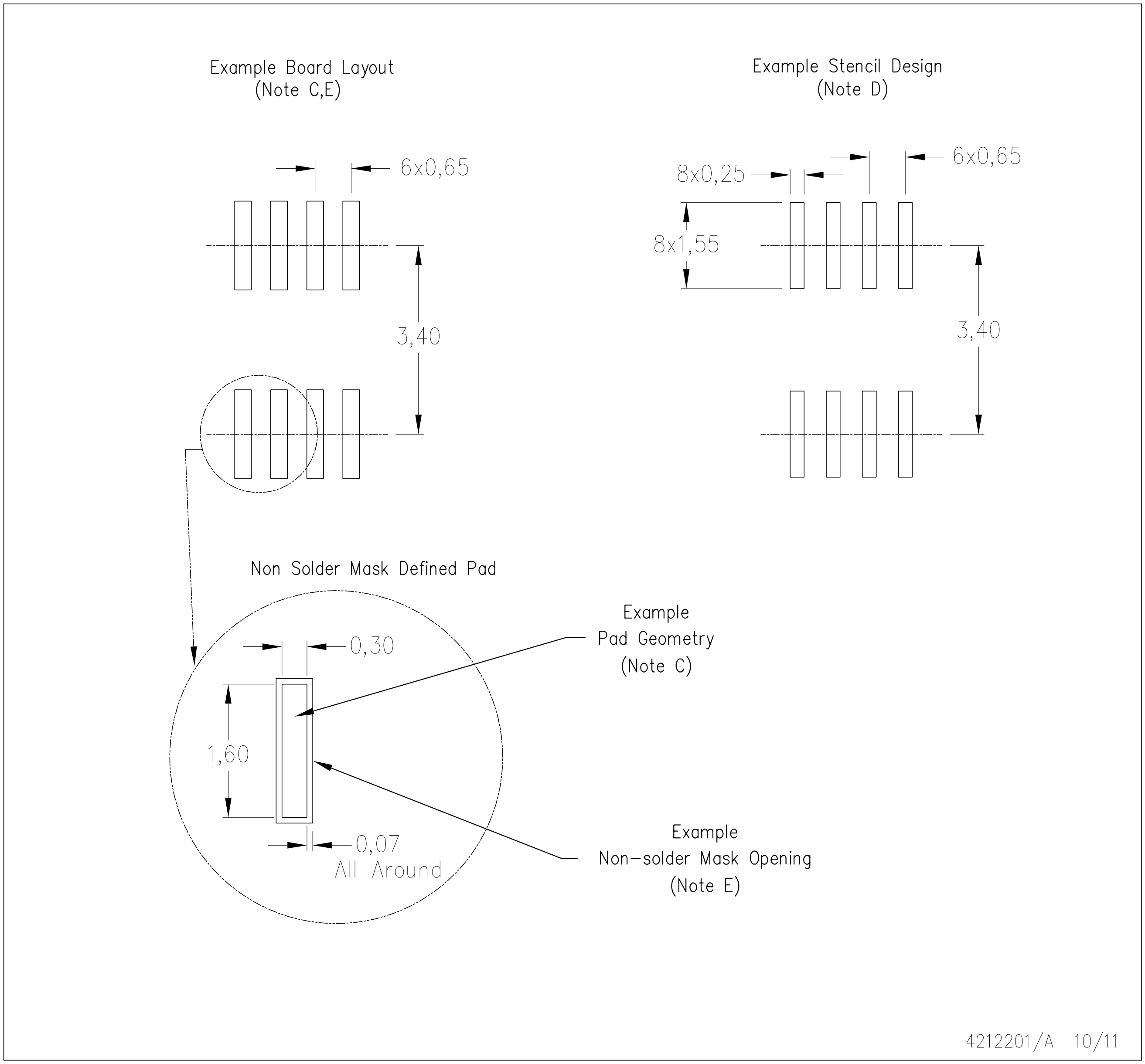
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G66DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G66DCURG4	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G66YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



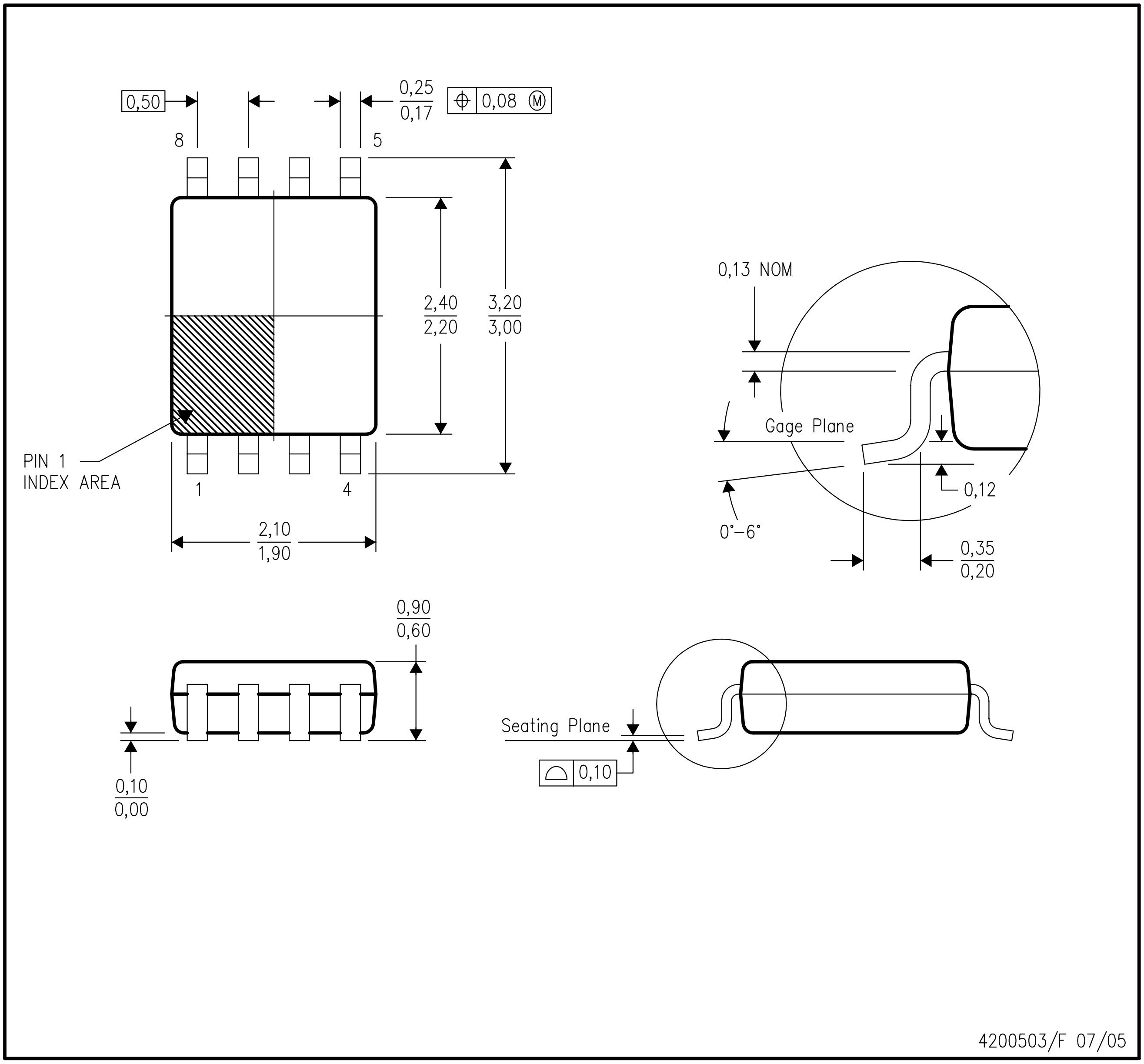
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8) PLASTIC SMALL OUTLINE



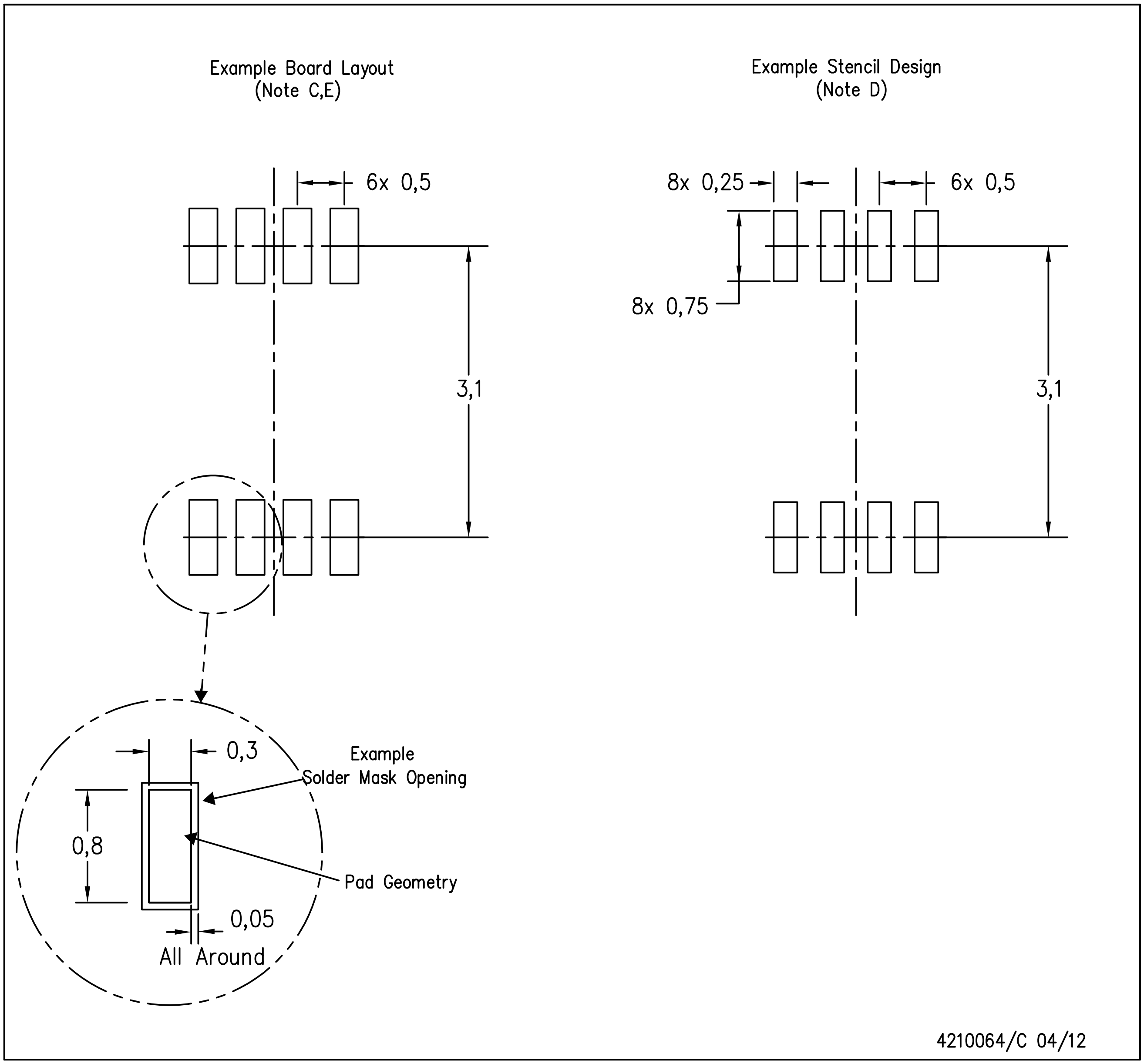
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



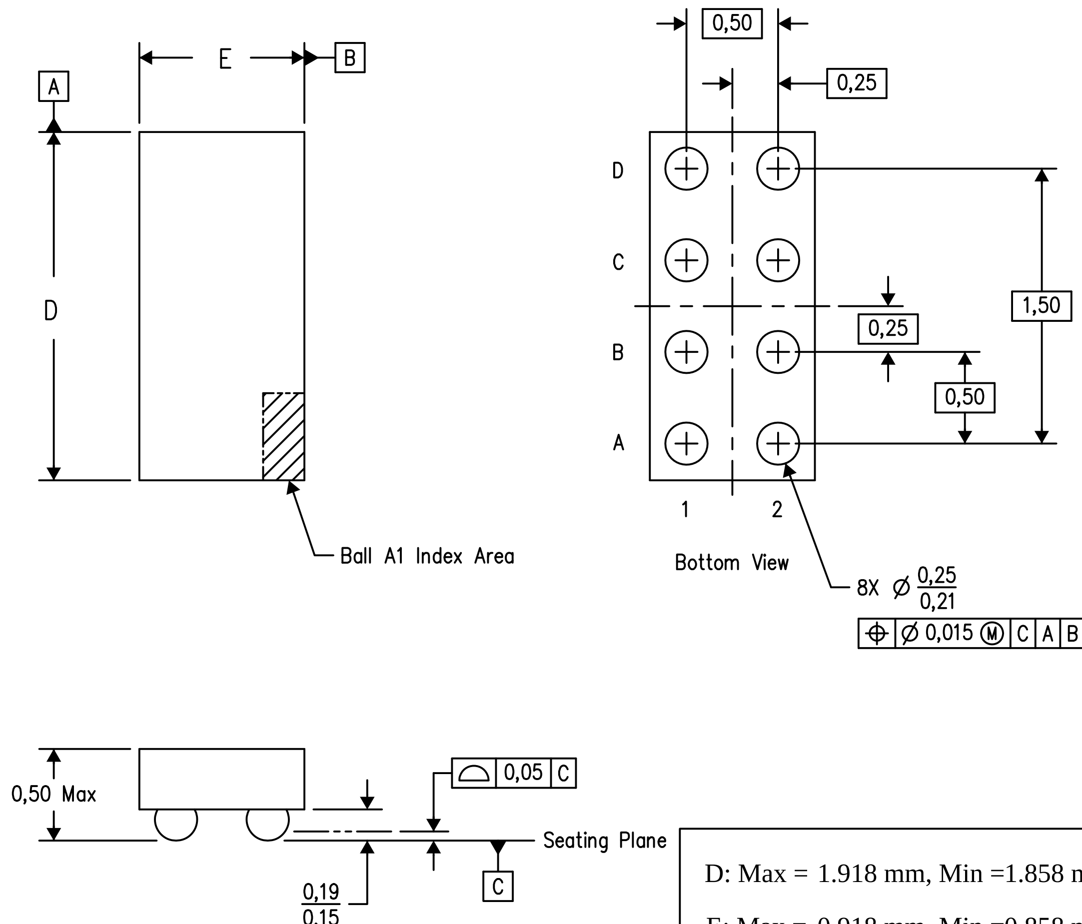
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4204741–5/K 05/13

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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