

FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer
- Chip-Select Inputs Gate Data Outputs From Changing State and Minimize System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in Unterminated Line
- Supports SSTL_18 Data Inputs
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on Control and $\overline{\text{RESET}}$ Inputs
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 5000-V Human-Body Model (A114-A)
 - 150-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL_18, except the LVCMOS reset ($\overline{\text{RESET}}$) and LVCMOS control (Cn) inputs. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL_18 specifications.

The SN74SSTU32864C operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and should not be used.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared and the data outputs are driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SN74SSTU32864C must ensure that the outputs remain low, thus ensuring no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTU32864CGKER	S864C
	LFBGA – ZKE	Tape and reel	SN74SSTU32864CZKER	S864C

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ is a trademark of Texas Instruments.

SN74SSTU32864C
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

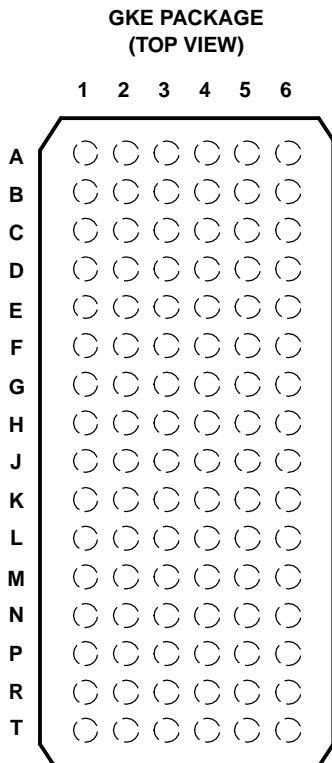
SCES542B–JANUARY 2004–REVISED APRIL 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ and Cn inputs always must be held at a valid logic high or logic low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn outputs function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and forces the output low. If the $\overline{\text{DCS}}$ control functionality is not desired, the $\overline{\text{CSR}}$ input can be hard-wired to ground, in which case the setup-time requirement for $\overline{\text{DCS}}$ is the same as for the other D data inputs.

The two V_{REF} pins (A3 and T3) are connected together internally by approximately 150 Ω . However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.



TERMINAL ASSIGNMENTS FOR 1:1 REGISTER (C0 = 0, C1 = 0)⁽¹⁾⁽²⁾⁽³⁾

	1	2	3	4	5	6
A	D1 (DCKE)	NC	V _{REF}	V _{CC}	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{CC}	V _{CC}	Q3	Q16
D	D4 (DODT)	NC	GND	GND	Q4 (QODT)	DNU
E	D5	D17	V _{CC}	V _{CC}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	<u>RESET</u>	V _{CC}	V _{CC}	C1	C0
H	CLK	D7 (DCS)	GND	GND	Q7 (QCS)	DNU
J	<u>CLK</u>	<u>CSR</u>	V _{CC}	V _{CC}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{CC}	V _{CC}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{CC}	V _{CC}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{CC}	V _{CC}	Q13	Q24
T	D14	D25	V _{REF}	V _{CC}	Q14	Q25

(1) Each pin name in parentheses indicates the DDR2 DIMM signal name.

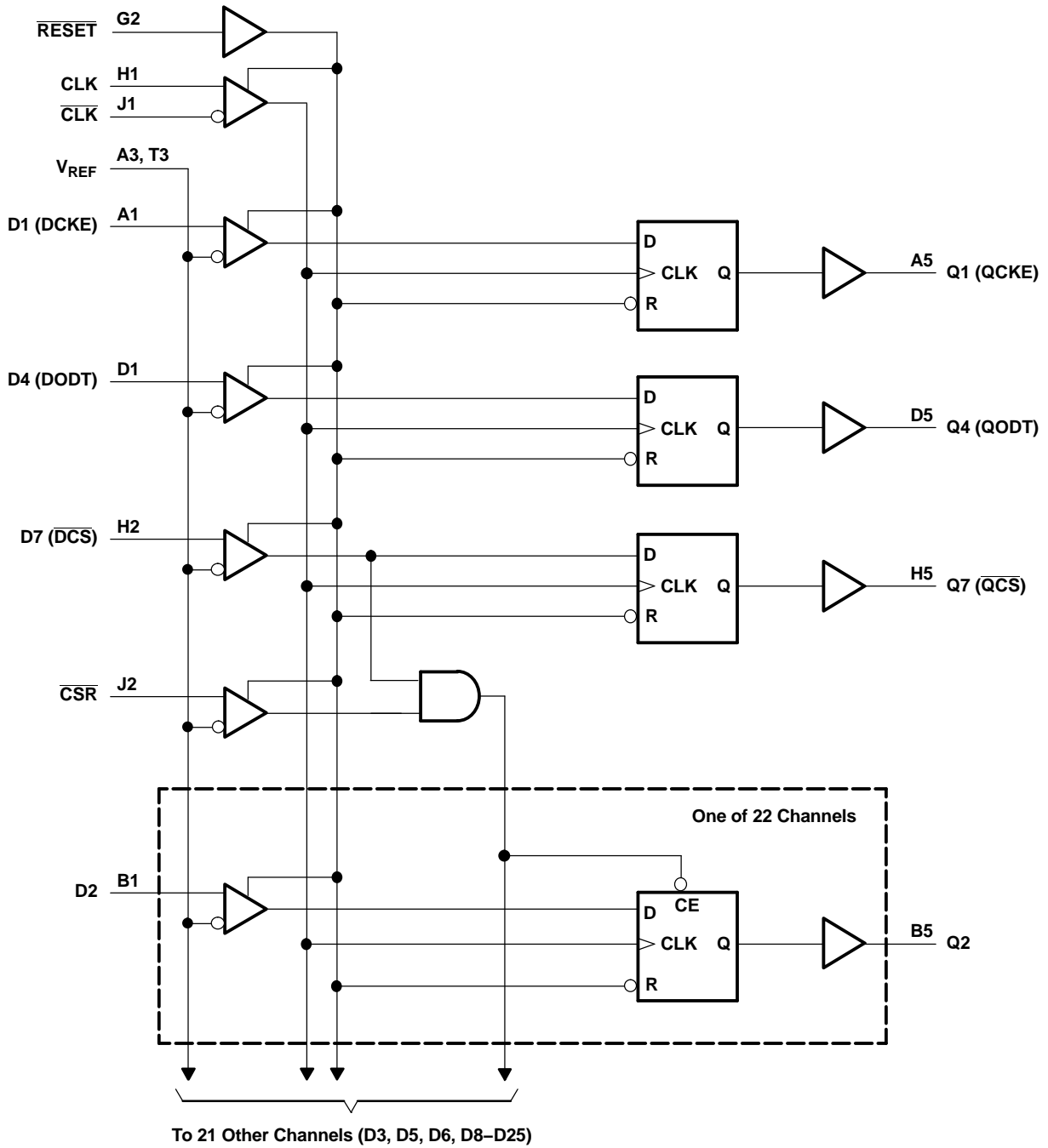
(2) NC - No internal connection

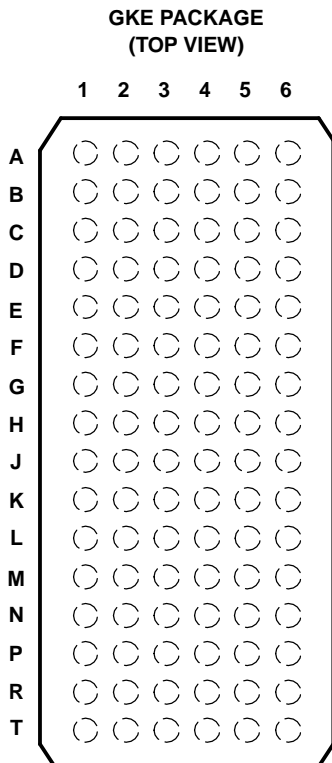
(3) DNU - Do not use

SN74SSTU32864C
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCES542B–JANUARY 2004–REVISED APRIL 2005

LOGIC DIAGRAM FOR 1:1 REGISTER CONFIGURATION (POSITIVE LOGIC)





TERMINAL ASSIGNMENTS FOR 1:2 REGISTER A (C0 = 0, C1 = 1)⁽¹⁾⁽²⁾⁽³⁾

	1	2	3	4	5	6
A	D1 (DCKE)	NC	V _{REF}	V _{CC}	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{CC}	V _{CC}	Q3A	Q3B
D	D4 (DODT)	NC	GND	GND	Q4A (QODTA)	Q4B (QODTB)
E	D5	DNU	V _{CC}	V _{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	<u>RESET</u>	V _{CC}	V _{CC}	C1	C0
H	CLK	D7 (DCS)	GND	GND	Q7A (QCSA)	Q7B (QCSB)
J	<u>CLK</u>	<u>CSR</u>	V _{CC}	V _{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{CC}	V _{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{CC}	V _{CC}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{CC}	V _{CC}	Q13A	Q13B
T	D14	DNU	V _{REF}	V _{CC}	Q14A	Q14B

(1) Each pin name in parentheses indicates the DDR2 DIMM signal name.

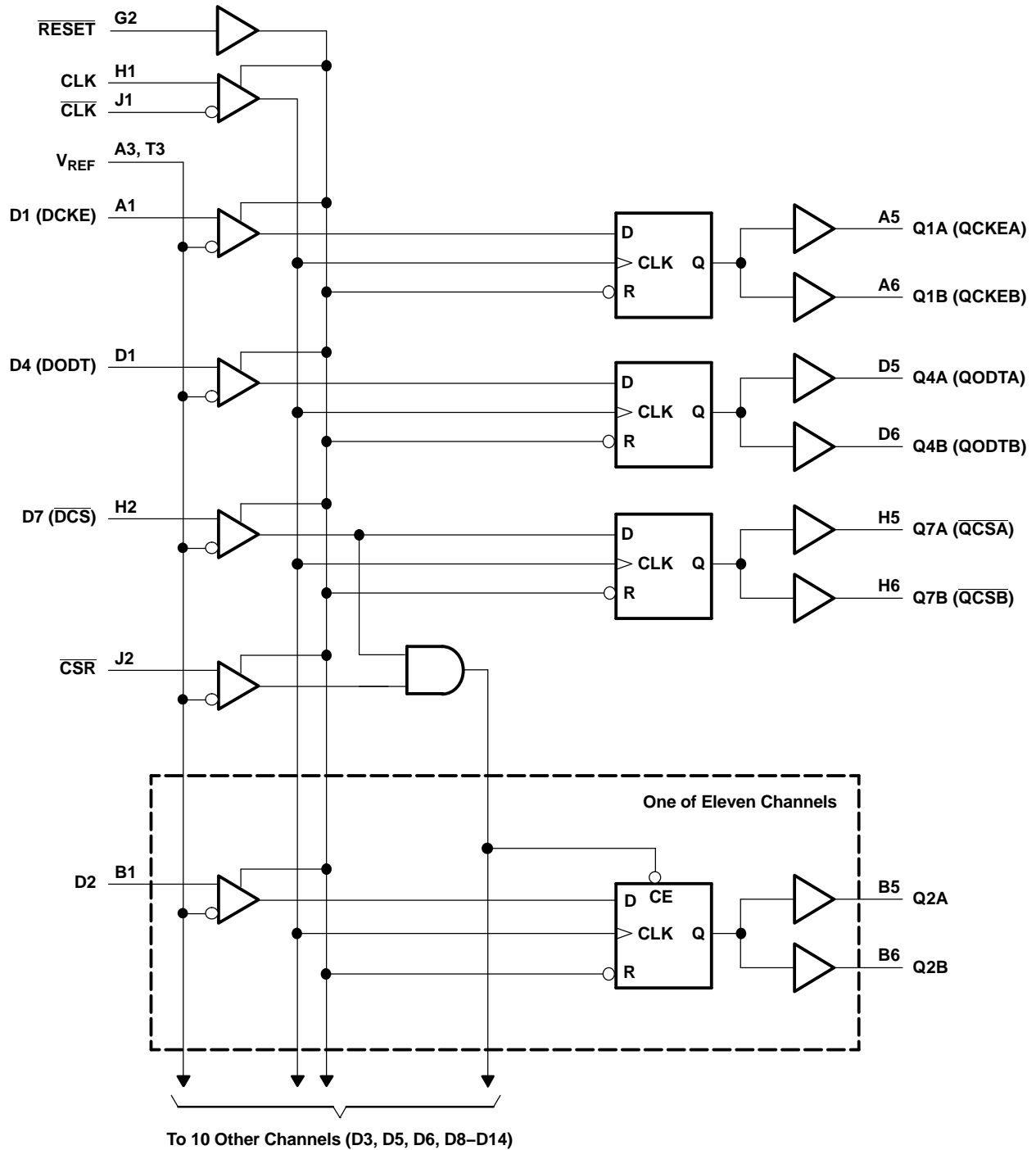
(2) NC - No internal connection

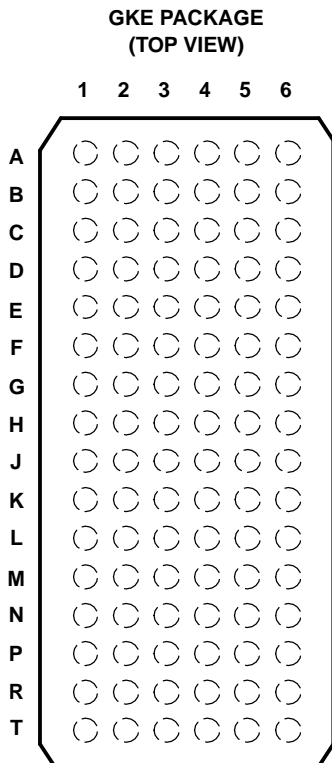
(3) DNU - Do not use

SN74SSTU32864C
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCES542B—JANUARY 2004—REVISED APRIL 2005

LOGIC DIAGRAM 1:2 REGISTER-A CONFIGURATION (POSITIVE LOGIC)





TERMINAL ASSIGNMENTS FOR 1:2 REGISTER B (C0 = 1, C1 = 1)⁽¹⁾⁽²⁾⁽³⁾

	1	2	3	4	5	6
A	D1	NC	V _{REF}	V _{CC}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{CC}	V _{CC}	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	V _{CC}	V _{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	<u>RESET</u>	V _{CC}	V _{CC}	C1	C0
H	CLK	D7 (DCS)	GND	GND	Q7A (<u>QCSA</u>)	Q7B (<u>QCSB</u>)
J	<u>CLK</u>	<u>CSR</u>	V _{CC}	V _{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{CC}	V _{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	V _{CC}	V _{CC}	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{CC}	V _{CC}	Q13A	Q13B
T	D14 (DCKE)	DNU	V _{REF}	V _{CC}	Q14A (QCKEA)	Q14B (QCKEB)

(1) Each pin name in parentheses indicates the DDR2 DIMM signal name.

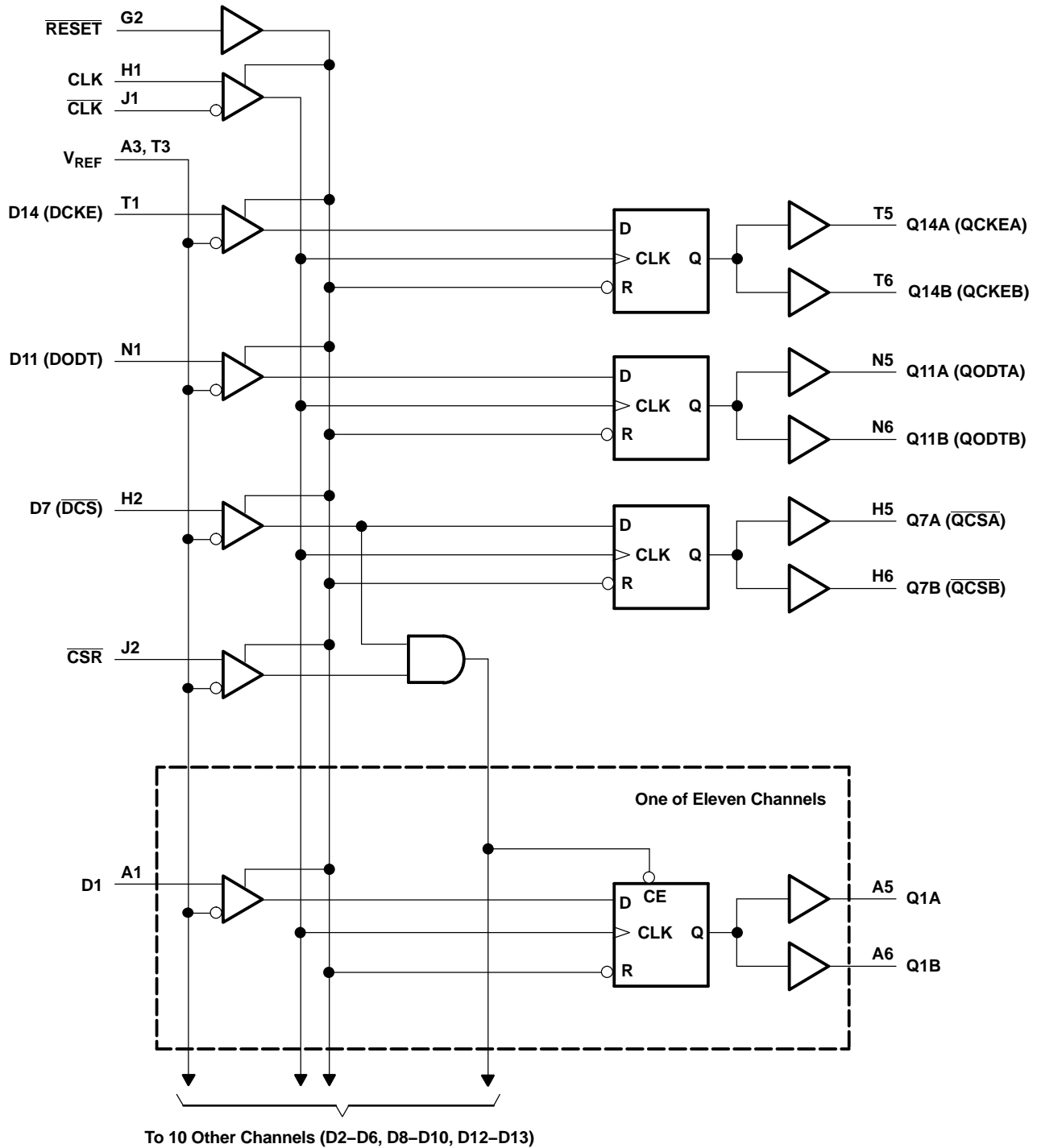
(2) NC - No internal connection

(3) DNU - Do not use

SN74SSTU32864C
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCES542B—JANUARY 2004—REVISED APRIL 2005

LOGIC DIAGRAM 1:2 REGISTER-B CONFIGURATION (POSITIVE LOGIC)



TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V _{CC}	Power-supply voltage	1.8 V nominal
V _{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{\text{CLK}}$	Negative master clock input	Differential input
C0, C1	Configuration control inputs – Register A, Register B, 1:1, 1:2 select	LVC MOS inputs
RESET	Asynchronous reset input – resets registers and disables V _{REF} data and clock differential-input receivers. When RESET is low, all Q outputs are forced low.	LVC MOS input
D1–D25	Data inputs – clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$	SSTL_18 inputs
$\overline{\text{CSR}}$, $\overline{\text{DCS}}$	Chip select inputs – disables register clocking ⁽¹⁾ when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
Q1–Q25 ⁽²⁾	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8-V CMOS outputs
$\overline{\text{QCS}}$	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8-V CMOS output
QODT	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8-V CMOS output
QCKE	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8-V CMOS output
NC	No internal connection	
DNU	Do not use – inputs are in standby-equivalent mode, and outputs are driven low.	

- (1) Data inputs = D2, D3, D5, D6, D8–D25 when C0 = 0 and C1 = 0
 Data inputs = D2, D3, D5, D6, D8–D14 when C0 = 0 and C1 = 1
 Data inputs = D1–D6, D8–D12, D13 when C0 = 1 and C1 = 1
- (2) Data outputs = Q2, Q3, Q5, Q6, Q8–when C0 = 0 and C1 = 0
 Data outputs = Q2, Q3, Q5, Q6, Q8–Q14 when C0 = 0 and C1 = 1
 Data outputs = Q1–Q6, Q8–Q10, Q12, Q13 when C0 = 1 and C1 = 1

FUNCTION TABLES

INPUTS						OUTPUT Qn
RESET	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CLK	$\overline{\text{CLK}}$	Dn	
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q ₀
H	X	X	L or H	L or H	X	Q ₀
L	X or floating	X or floating	X or floating	X or floating	X or floating	L

INPUTS				OUTPUTS
RESET	CLK	$\overline{\text{CLK}}$	DCKE, $\overline{\text{DCS}}$, DODT	QCKE, $\overline{\text{QCS}}$, QODT
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q ₀
L	X or floating	X or floating	X or floating	L

SN74SSTU32864C

25-BIT CONFIGURABLE REGISTERED BUFFER WITH SSTL_18 INPUTS AND OUTPUTS

SCES542B–JANUARY 2004–REVISED APRIL 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	2.5	V
V_I	Input voltage range ⁽²⁾⁽³⁾	–0.5	2.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±50 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±50 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±50 mA
	Continuous current through each V_{CC} or GND			±100 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			36 °C/W
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 2.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	1.7		1.9	V
V_{REF}	Reference voltage	$0.49 \times V_{CC}$	$0.5 \times V_{CC}$	$0.51 \times V_{CC}$	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs, \overline{CSR}		$V_{REF} + 250$ mV	V
V_{IL}	AC low-level input voltage	Data inputs, \overline{CSR}		$V_{REF} - 250$ mV	V
V_{IH}	DC high-level input voltage	Data inputs, \overline{CSR}		$V_{REF} + 125$ mV	V
V_{IL}	DC low-level input voltage	Data inputs, \overline{CSR}		$V_{REF} - 125$ mV	V
V_{IH}	High-level input voltage	\overline{RESET} , Cn		$0.65 \times V_{CC}$	V
V_{IL}	Low-level input voltage	\overline{RESET} , Cn		$0.35 \times V_{CC}$	V
V_{ICR}	Common-mode input voltage range	CLK, \overline{CLK}		0.675	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, \overline{CLK}		600	mV
I_{OH}	High-level output current			–8	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

- (1) The \overline{RESET} and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless \overline{RESET} is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	1.7 V to 1.9 V	V _{CC} - 0.2			V
		I _{OH} = -6 mA	1.7 V	1.3			
V _{OL}		I _{OL} = 100 μA	1.7 V to 1.9 V	0.2			V
		I _{OL} = 6 mA	1.7 V	0.4			
I _I	All inputs ⁽²⁾	V _I = V _{CC} or GND	1.9 V	±5			μA
I _{CC}	Static standby	RESET = GND	1.9 V	100			μA
	Static operating	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)}		40			mA
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching 50% duty cycle	1.8 V	33			μA/MHz
	Dynamic operating – per each data input, 1:1 configuration	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching 50% duty cycle,		19			μA/clock MHz/D input
	Dynamic operating – per each data input, 1:2 configuration	One data input switching at one-half clock frequency, 50% duty cycle		35			
I _{CCDLP}	Chip-select-enabled low-power active mode, clock only	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching 50% duty cycle	1.8 V	34			μA/MHz
	Chip-select-enabled low-power active mode, 1:1 configuration	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching 50% duty cycle,		2			μA/clock MHz/D input
	Chip-select-enabled low-power active mode, 1:2 configuration	One data input switching at one-half clock frequency, 50% duty cycle		2			
C _i	Data inputs, CSR	V _I = V _{REF} ± 250 mV	1.8 V	2.5	3	3.5	pF
	CLK, CLK	V _{ICR} = 0.9 V, V _{I(PP)} = 600 mV		2		3	
	RESET	V _I = V _{CC} or GND		2.5			

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C.

(2) Each V_{REF} pin (A3 or T3) should be tested independently, with the other (untested) pin open.

Timing Requirements⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
f _{clock}	Clock frequency	500		MHz
t _w	Pulse duration, CLK, CLK high or low	1		ns
t _{act}	Differential inputs active time ⁽²⁾	10		ns
t _{inact}	Differential inputs inactive time ⁽³⁾	15		ns
t _{su}	Setup time	DCS before CLK↑, CLK↓, CSR high; CSR before CLK↑, CLK↓, DCS high		0.6
		DCS before CLK↑, CLK↓, CSR low		0.5
		DODT, DCKE, and Data before CLK↑, CLK↓		0.5
t _h	Hold time	DCS, DODT, DCKE, and Data after CLK↑, CLK↓		0.5

(1) All input slew rates are 1 V/ns ±20%.

(2) V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max after RESET is taken high.

(3) V_{REF} data and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max after RESET is taken low.

SN74SSTU32864C
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCE542B–JANUARY 2004–REVISED APRIL 2005

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.1\text{ V}$		UNIT
			MIN	MAX	
f_{max}			500		MHz
$t_{pdm}^{(1)}$	CLK and $\overline{\text{CLK}}$	Q	1.4	2.4	ns
$t_{pdms}^{(1)}$	CLK and $\overline{\text{CLK}}$	Q		2.6	ns
$t_{RPHL}^{(1)}$	$\overline{\text{RESET}}$	Q		3	ns

(1) Includes 350-ps test-load transmission-line delay

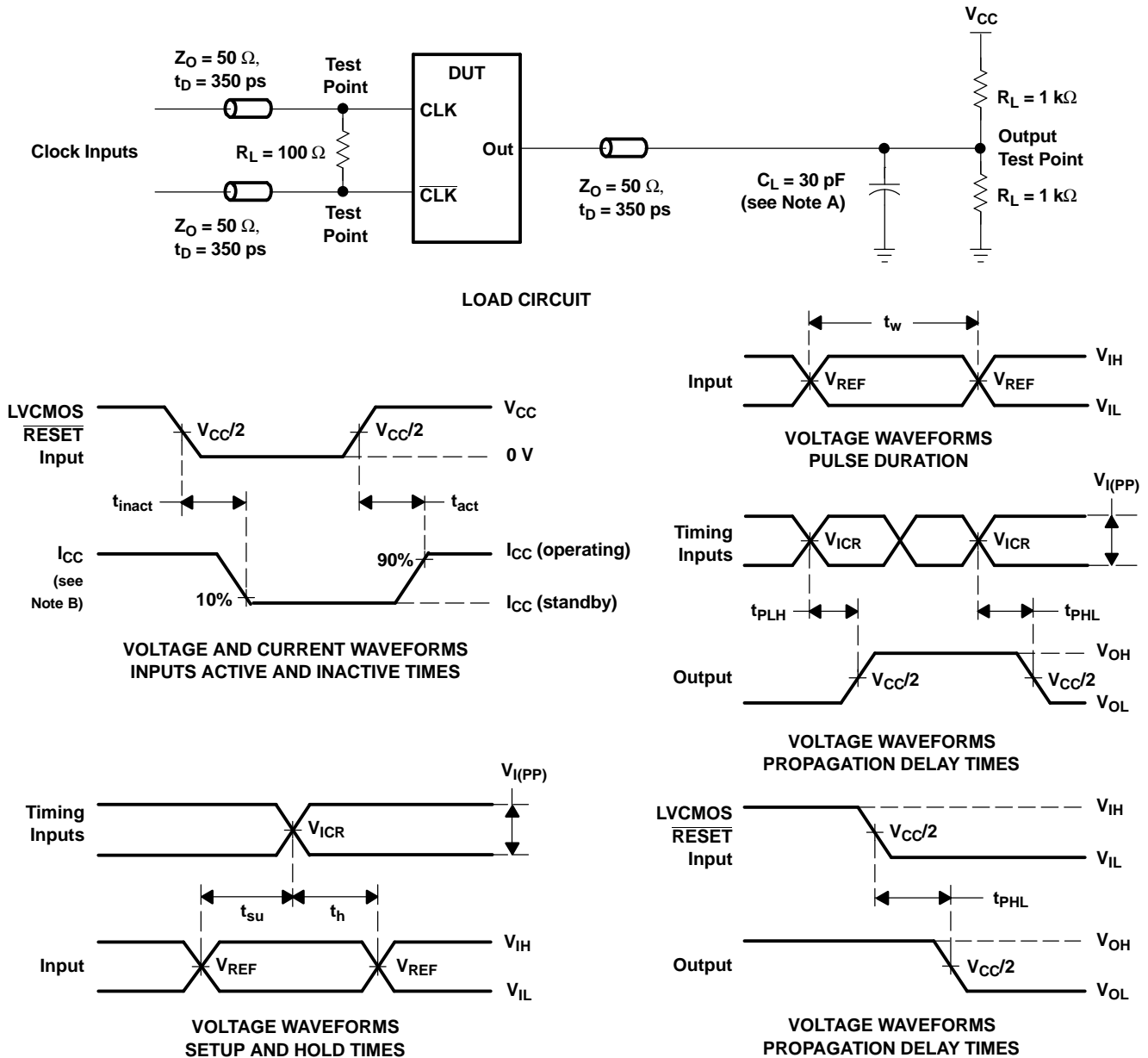
Output Slew Rates

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO	$V_{CC} = 1.8\text{ V}$ $\pm 0.1\text{ V}$		UNIT
			MIN	MAX	
dV/dt_r	20%	80%	1.9	4.9	V/ns
dV/dt_f	80%	20%	1.9	4.9	V/ns
$dV/dt_{\Delta}^{(1)}$	20% or 80%	80% or 20%		1.5	V/ns

(1) Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

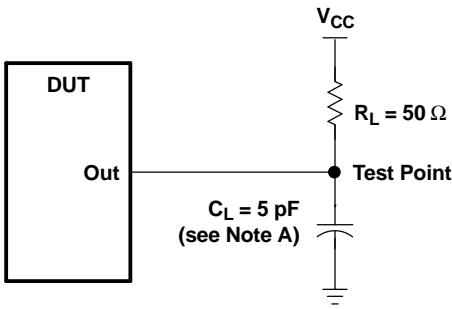
PARAMETER MEASUREMENT INFORMATION



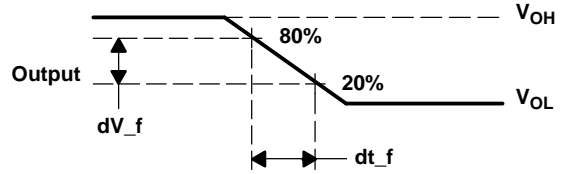
- NOTES:
- C_L includes probe and jig capacitance.
 - I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_O = 0 \text{ mA}$.
 - All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise noted).
 - The outputs are measured one at a time, with one transition per measurement.
 - $V_{\text{REF}} = V_{CC}/2$
 - $V_{IH} = V_{\text{REF}} + 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVC MOS input.
 - $V_{IL} = V_{\text{REF}} - 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.
 - $V_{I(\text{PP})} = 600 \text{ mV}$
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

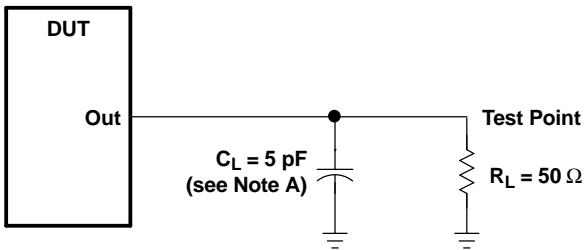
PARAMETER MEASUREMENT INFORMATION



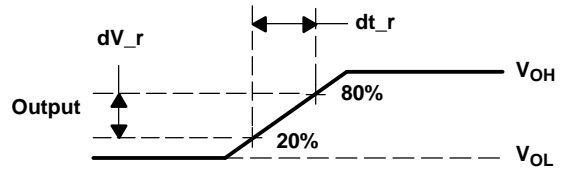
LOAD CIRCUIT
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT
LOW-TO-HIGH SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
LOW-TO-HIGH SLEW-RATE MEASUREMENT

- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics:
PRR \leq 10 MHz, $Z_O = 50 \Omega$, input slew rate = 1 V/ns \pm 20% (unless otherwise specified).

Figure 2. Output Slew-Rate Measurement Information

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74SSTU32864CZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	S864C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

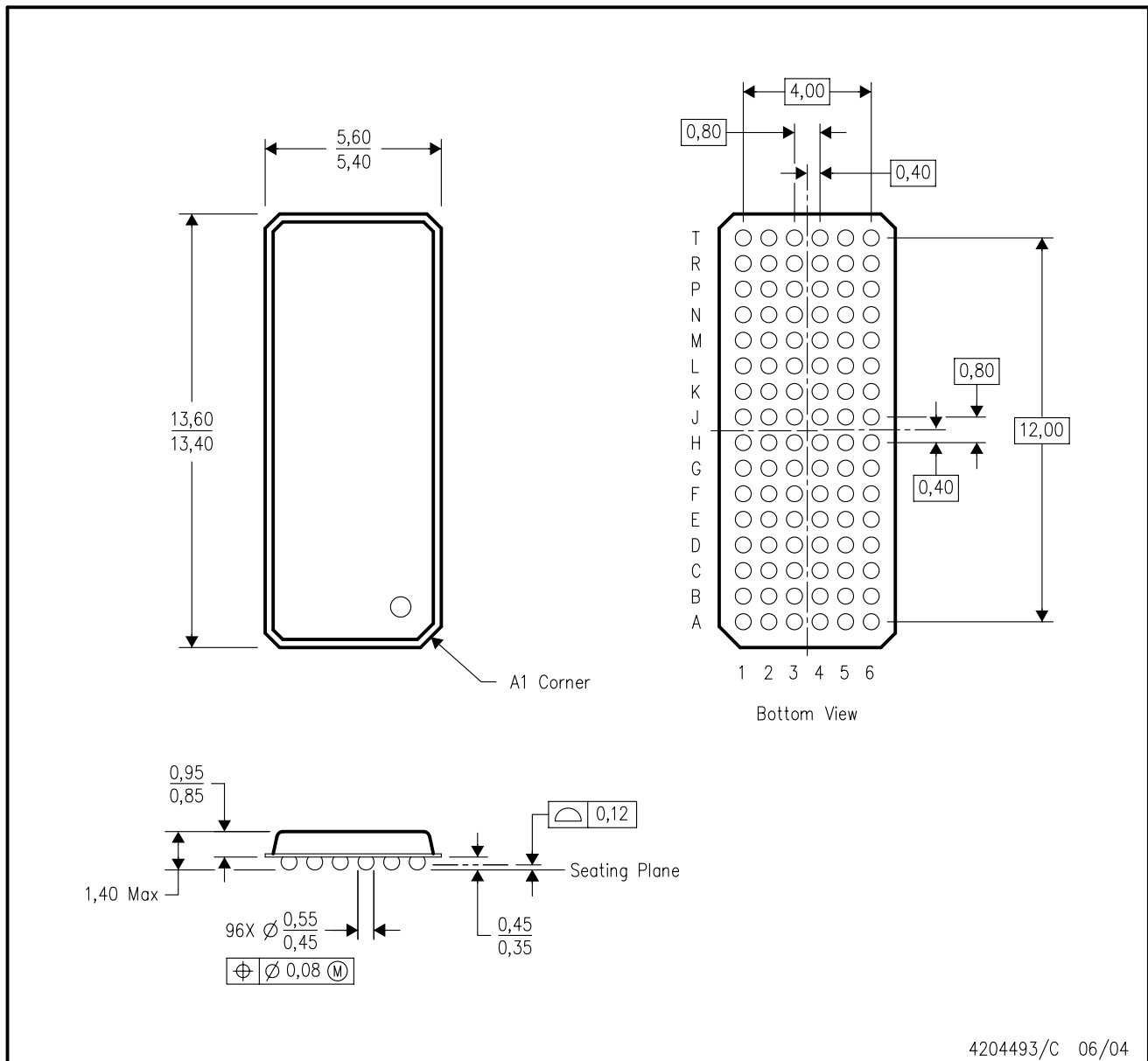
(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com