

#### FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree<sup>™</sup> Packages
- Control Inputs VIH/VIL Levels Are Referenced to V<sub>CCA</sub> Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- **Typical Max Data Rates** 
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 200 Mbps (<1.8-V to 3.3-V Translation)</li>
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### **DESCRIPTION/ORDERING INFORMATION**

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V<sub>CCA</sub>. V<sub>CCA</sub> accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V<sub>CCB</sub>. V<sub>CCB</sub> accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCH1T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

The SN74AVCH1T45 is designed so that the DIR input is powered by  $V_{CCA}$ .

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AVCH1T45YZPR	TF_
–40°C to 85°C	SOT (SOT-23) – DBV	Tape and reel	SN74AVCH1T45DBVR	ET1_
	SOT (SC-70) – DCK	Tape and reel	SN74AVCH1T45DCKR	TF_

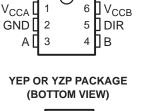
Package drawings, thermal data, and symbolization are available at www.ti.com/packaging. (1)

DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. (2)

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. NanoStar, NanoFree are trademarks of Texas Instruments.



**DBV OR DCK PACKAGE** 

(TOP VIEW)

А	03	40	В
GND			
$V_{\text{CCA}}$	01	60	$V_{CCB}$



**DESCRIPTION/ORDERING INFORMATION (CONTINUED)** 

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

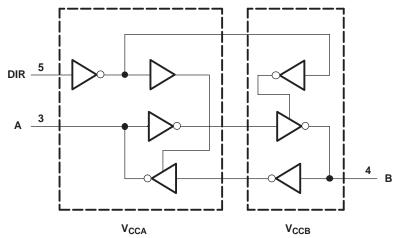
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

NanoFree<sup>™</sup> package technology is a major breakthrough in IC packaging concepts, using the die as the package.

INPUT DIR	OPERATION
L	B data to A bus
Н	A data to B bus

#### **FUNCTION TABLE**







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#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V <sub>CCA</sub> V <sub>CCB</sub>	Supply voltage range		-0.5	4.6	V	
		I/O ports (A port)	-0.5	4.6		
VI	Input voltage range <sup>(2)</sup>	I/O ports (B port)	-0.5	4.6	V	
		Control inputs	-0.5	4.6		
V	Voltage range applied to any output in the high-impedance or	A port	-0.5	4.6	V	
Vo	power-off state <sup>(2)</sup>	B port	-0.5	4.6	v	
	Values represented to one output in the high or low state $\binom{2}{3}$	A port	-0.5	V <sub>CCA</sub> + 0.5	V	
Vo	Voltage range applied to any output in the high or low state $^{(2)(3)}$	B port	-0.5	V <sub>CCB</sub> + 0.5	v	
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA	
I <sub>O</sub>	Continuous output current			±50	mA	
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA	
		DBV package		165		
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCK package		259	°C/W	
		YZP package	123		1	
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

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### Recommended Operating Conditions<sup>(1)(2)(3)(4)(5)</sup>

			V <sub>CCI</sub>	V <sub>cco</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V
			1.2 V to 1.95 V		$V_{CCI}  imes 0.65$		
VIH	High-level input voltage	Data inputs <sup>(4)</sup>	1.95 V to 2.7 V		1.6		V
	input voltage		2.7 V to 3.6 V		2		
			1.2 V to 1.95 V			$V_{CCI}  imes 0.35$	
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(4)</sup>	1.95 V to 2.7 V			0.7	V
	input voltage		2.7 V to 3.6 V			0.8	
			1.2 V to 1.95 V		$V_{CCA}  imes 0.65$		
VIH	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.95 V to 2.7 V		1.6		V
	input voltage		2.7 V to 3.6 V		2		
			1.2 V to 1.95 V			$V_{CCA}  imes 0.35$	
VIL	Low-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.95 V to 2.7 V			0.7	V
	input voltage	(referenced to vCCA)	2.7 V to 3.6 V			0.8	
VI	Input voltage	ł			0	3.6	V
	Quality of the sec	Active state			0	V <sub>CCO</sub>	
Vo	Output voltage	3-state			0	3.6	V
				1.2 V		-3	
				1.4 V to 1.6 V		-6	
I <sub>OH</sub>	High-level output cu	rrent		1.65 V to 1.95 V		-8	mA
				2.3 V to 2.7 V		-9	
				3 V to 3.6 V		-12	
				1.2 V		3	
				1.4 V to 1.6 V		6	
l <sub>OL</sub>	Low-level output cu	rrent		1.65 V to 1.95 V		8	mA
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise	or fall rate				5	ns/V
T <sub>A</sub>	Operating free-air te	emperature			-40	85	°C

V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V.
For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V.



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#### Electrical Characteristics<sup>(1)(2)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDU	TIONE	v	v	T <sub>A</sub> = 2	5°C	–40°C to 85	5°C	UNI	
PARAMETER	TEST CONDI	TIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN TY	P MAX	MIN	MAX		
	I <sub>OH</sub> = -100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V		V <sub>CCO</sub> - 0.2 V       0.95     1.05       1.05     1.2       1.75     2.3       0.15     2.3       0.15     1.05       1.05     2.3       0.15     1.3       1.01     1.3       0.15     1.3       1.01     1.3       1.01     1.3       1.01     1.3       1.025     ±0.25       25     1.3       1.0025     ±0.25       25     1.5       25     1.5       25     1.5       25     1.00       -25     1.00       -25     -115       1.00     -25       1.00     -25       1.00     1.125       2.00     3.00       5.0     1.25       1.00     5.00       -50     -1.25       -200     -300				
	I <sub>OH</sub> = -3 mA		1.2 V	1.2 V	0.9	95				
\ <i>\</i>	I <sub>OH</sub> =6 mA	., .,	1.4 V	1.4 V			1.05			
V <sub>OH</sub>	I <sub>OH</sub> =8 mA	$V_{I} = V_{IH}$	1.65 V	1.65 V			1.2		V	
	I <sub>OH</sub> = -9 mA		2.3 V	2.3 V			1.75			
	I <sub>OH</sub> = -12 mA		3 V	3 V			2.3		1	
	I <sub>OL</sub> = 100 A		1.2 V to 3.6 V	1.2 V to 3.6 V				0.2		
	I <sub>OL</sub> = 3 mA		1.2 V	1.2 V	0.1	15				
. /	I <sub>OL</sub> = 6 mA	., .,	1.4 V	1.4 V				0.35		
V <sub>OL</sub>	I <sub>OL</sub> = 8 mA	$V_{I} = V_{IL}$	1.65 V	1.65 V				0.45	V	
	I <sub>OL</sub> = 9 mA	1	2.3 V	2.3 V				0.55	t	
	I <sub>OL</sub> = 12 mA			3 V				0.7	t	
I <sub>I</sub> DIR	$V_I = V_{CCA}$ or GND	1	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.02	25 ±0.25		±1	μA	
	V <sub>I</sub> = 0.42 V		1.2 V	1.2 V	:	25				
	V <sub>I</sub> = 0.49 V		1.4 V	1.4 V			15			
I <sub>BHL</sub> <sup>(3)</sup>	V <sub>I</sub> = 0.58 V	V <sub>I</sub> = 0.58 V		1.65 V			25		μA	
	V <sub>I</sub> = 0.7 V		2.3 V	2.3 V			45			
	V <sub>I</sub> = 0.8 V		3.3 V	3.3 V			100			
	V <sub>I</sub> = 0.78 V		1.2 V	1.2 V	-:	25				
	V <sub>I</sub> = 0.91 V		1.4 V	1.4 V			-15			
I <sub>BHH</sub> <sup>(4)</sup>	V <sub>I</sub> = 1.07 V		1.65 V	1.65 V			-25		μA	
	V <sub>I</sub> = 1.6 V		2.3 V	2.3 V			-45			
	V <sub>1</sub> = 2 V		3.3 V	3.3 V			-100			
			1.2 V	1.2 V	Į	50				
			1.6 V	1.6 V			125		İ	
I <sub>BHLO</sub> <sup>(5)</sup>	$V_{I} = 0$ to $V_{CC}$		1.95 V	1.95 V			200		μA	
-			2.7 V	2.7 V			300			
			3.6 V	3.6 V			500			
			1.2 V	1.2 V		50				
			1.6 V	1.6 V			-125			
I <sub>BHHO</sub> <sup>(6)</sup>	$V_{I} = 0$ to $V_{CC}$		1.95 V	1.95 V			-200		μA	
		2.7 V	2.7 V					-		
		3.6 V	3.6 V	1		-500		ł		

(1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

(5) An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

(6) An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.



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#### Electrical Characteristics<sup>(1)(2)</sup> (Continued)

over recommended operating free-air temperature range (unless otherwise noted)

	AMETER			V	V	Τ <sub>4</sub>	∖ = 25°C		–40°C to	85°C	UNIT
PAR	AMETER	TEST CONDIT	IONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNIT
	A port			0 V	0 to 3.6 V		±0.1	±1		±5	۸
l <sub>off</sub>	B port	$V_{\rm I}$ or $V_{\rm O}$ = 0 to 3.6 V		0 to 3.6 V	0 V		±0.1 ±1			±5	μA
	B port	$V_0 = V_{CCO}$ or GND, $V_1 = V_{CCI}$ or GND		0 V	3.6 V		±0.5	±2.5		5	۸
I <sub>OZ</sub>	A port			3.6 V	0 V		±0.5	±2.5		5	μA
				1.2 V to 3.6 V	1.2 V to 3.6 V					10	
I <sub>CCA</sub>		$V_I = V_{CCI}$ or GND,	$I_{O} = 0$	0 V	3.6 V					-2	μA
				3.6 V	0 V					10	
				1.2 V to 3.6 V	1.2 V to 3.6 V					10	
I <sub>CCB</sub>		$V_I = V_{CCI}$ or GND,	$I_{O} = 0$	0 V	3.6 V					10	μA
				3.6 V	0 V					-2	
I <sub>CCA</sub> +	I <sub>CCB</sub>	$V_I = V_{CCI}$ or GND,	$I_{O} = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					20	μA
Ci	Control inputs	V <sub>1</sub> = 3.3 V or GND		3.3 V	3.3 V		2.5				pF
C <sub>io</sub>	A or B port	$V_{O} = 3.3 \text{ V or GND}$		3.3 V	3.3 V		6				pF

 $\begin{array}{ll} \mbox{(1)} & V_{CCO} \mbox{ is the } V_{CC} \mbox{ associated with the output port.} \\ \mbox{(2)} & V_{CCI} \mbox{ is the } V_{CC} \mbox{ associated with the input port.} \end{array}$ 

#### **Switching Characteristics**

over recommended operating free-air temperature range, V<sub>CCA</sub> = 1.2 V (see Figure 11)

PARAMETER	FROM	то	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V	V <sub>CCB</sub> = 1.8 V	V <sub>CCB</sub> = 2.5 V	V <sub>CCB</sub> = 3.3 V	UNIT						
PARAMETER	(INPUT)	(OUTPUT)	ТҮР	ТҮР	ТҮР	ТҮР	ТҮР	UNIT						
t <sub>PLH</sub>	А	В	3.3	2.7	2.4	2.3	2.4							
t <sub>PHL</sub>	A	Б	3.3	2.7	2.4	2.3	2.4	ns						
t <sub>PLH</sub>	В	А	3.3	3.1	2.9	2.8	2.7							
t <sub>PHL</sub>	D	A	3.3	3.1	2.9	2.8	2.7	ns						
t <sub>PHZ</sub>	DIR	А	5.1	5.2	5.3	5.2	3.7	20						
t <sub>PLZ</sub>	DIK	A	5.1	5.2	5.3	5.2	3.7	ns						
t <sub>PHZ</sub>	DIR	В	5.3	4.3	4	3.3	3.7							
t <sub>PLZ</sub>	DIR	В	5.3	4.3	4	3.3	3.7	ns						
t <sub>PZH</sub> <sup>(1)</sup>	DIR		8.5	6.9	6.4	5.5	6.1							
t <sub>PZL</sub> <sup>(1)</sup>	DIR	A	8.5	6.9	6.4	5.5	6.1	ns						
t <sub>PZH</sub> <sup>(1)</sup>	DID	<b>D</b>	8.3	7.8	7.7	7.5	5.9							
t <sub>PZL</sub> <sup>(1)</sup>	DIR	DIR	DIR	В	B	В	В	B	8.3	7.8	7.7	7.5	5.9	ns

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

#### SN74AVCH1T45 SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS SCES598D-JULY 2004-REVISED JANUARY 2008

### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT			
	(INPUT)	(001201)	ТҮР	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
t <sub>PLH</sub>	٨	В	2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8				
t <sub>PHL</sub>	A	Б	2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	ns			
t <sub>PLH</sub>	В	А	2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	ns			
t <sub>PHL</sub>	D	A	2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	115			
t <sub>PHZ</sub>	סוס	А	3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9				
t <sub>PLZ</sub>	DIR	DIR	A	3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	ns		
t <sub>PHZ</sub>	DIR	В	5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	20			
t <sub>PLZ</sub>	DIK	Б	5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	ns			
t <sub>PZH</sub> <sup>(1)</sup>	סוס	А	7.7		13.6		12.4		9.6		9.3	20			
t <sub>PZL</sub> <sup>(1)</sup>	DIR	A	7.7		13.6		12.4		9.6		9.3	ns			
t <sub>PZH</sub> <sup>(1)</sup>	DIR	DIR	DIR	DIR	Р	6.7		12.3		12		11.1		10.7	
t <sub>PZL</sub> <sup>(1)</sup>					DIR	В	6.7		12.3		12		11.1		10.7

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

#### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1		V <sub>ССВ</sub> = ± 0.1		V <sub>ССВ</sub> = ± 0.2		V <sub>CCB</sub> = ± 0.3		UNIT												
	(INFUT)	(001201)	ТҮР	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX													
t <sub>PLH</sub>	А	В	2.8	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	20												
t <sub>PHL</sub>	A	Б	2.8	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	ns												
t <sub>PLH</sub>	В	А	2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	20												
t <sub>PHL</sub>	Б	A	2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	ns												
t <sub>PHZ</sub>	פוס	А	3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	20												
t <sub>PLZ</sub>	DIR	DIK	DIK	A	3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	ns										
t <sub>PHZ</sub>	DIR	В	5	1.8	7.7	1.4	6.8	1	4.4	1.4	4.3	20												
t <sub>PLZ</sub>	DIR	Б	5	1.89	7.7	1.4	6.8	1	4.4	1.4	4.3	ns												
t <sub>PZH</sub> <sup>(1)</sup>	DID	DID	DID		^	7.3		12.9		11.8		9		8.7	20									
t <sub>PZL</sub> <sup>(1)</sup>	DIR	DIR A	7.3		12.9		11.8		9		8.7	ns												
t <sub>PZH</sub> <sup>(1)</sup>	DIR	– DIR	В	6.5		11.2		10.9		9.8		9.4	20											
t <sub>PZL</sub> <sup>(1)</sup>			DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	В	6.5		11.2		10.9		9.8	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.



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#### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 0.1		V <sub>CCB</sub> = 0.15		V <sub>CCB</sub> = 0.2		V <sub>CCB</sub> = 0.3		UNIT			
	(INFUT)	(001201)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
t <sub>PLH</sub>	А	В	2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	20			
t <sub>PHL</sub>	A	Б	2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	ns			
t <sub>PLH</sub>	В	А	2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	20			
t <sub>PHL</sub>	Б	A	A	A	2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	ns	
t <sub>PHZ</sub>	DIR	А	2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	20			
t <sub>PLZ</sub>		DIR	DIR	A	2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	ns	
t <sub>PHZ</sub>	DIR	В	4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	20			
t <sub>PLZ</sub>	DIR	Б	4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	ns			
t <sub>PZH</sub> <sup>(1)</sup>		^	7.1		11.8		10.3		7.5		7.3	20			
t <sub>PZL</sub> <sup>(1)</sup>	DIR	A	7.1		11.8		10.3		7.5		7.3	ns			
t <sub>PZH</sub> <sup>(1)</sup>	DIR	DIR	DIR	DIR	D	5.4		8.6		8.1		7		6.6	
t <sub>PZL</sub> <sup>(1)</sup>					DIR	В	5.4		8.6		8.1		7		6.6

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

#### **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 0.1	1.5 V V	V <sub>ССВ</sub> = 0.15		V <sub>CCB</sub> = 0.2		V <sub>CCB</sub> = 0.3		UNIT															
	(INFUT)	(001201)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX																
t <sub>PLH</sub>	А	В	2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	20															
t <sub>PHL</sub>	A	Б	2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	ns															
t <sub>PLH</sub>	В	•	2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	20															
t <sub>PHL</sub>	D	A	2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	ns															
t <sub>PHZ</sub>	סוס	А	3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	20															
t <sub>PLZ</sub>	DIR	DIR	A	3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	ns														
t <sub>PHZ</sub>	DIR	В	4	0.7	7.4	0.6	6.5	0.7	4	1.5	3.9	20															
t <sub>PLZ</sub>	DIR	D	4	0.7	7.4	0.6	6.5	0.7	4	1.5	3.9	ns															
t <sub>PZH</sub> <sup>(1)</sup>	סוס	•	6.2		11.2		9.9		7		6.7	20															
t <sub>PZL</sub> <sup>(1)</sup>	DIR	8 A -	6.2		11.2		9.9		7		6.7	ns															
t <sub>PZH</sub> <sup>(1)</sup>	DIR	DIR	В	5.7		8.9		8.5		7.2		6.8	20														
t <sub>PZL</sub> <sup>(1)</sup>			DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	D	5.7		8.9		8.5		7.2	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

#### **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

P	ARAMETER	TEST CONDITIONS	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	UNIT	
			TYP	TYP	TYP	TYP	TYP		
<b>c</b> (1)	A-port input, B-port output	C <sub>L</sub> = 0 pF, f = 10 MHz,	3	3	3	3	4	~ <b>F</b>	
CpdA	C <sub>pdA</sub> <sup>(1)</sup> B-port output B-port input, A-port output	$t_r = t_f = 1 \text{ ns}$	14	14	14	15	16	pF	
<b>C</b> (1)	A-port input, B-port output	C <sub>L</sub> = 0 pF, f = 10 MHz,	14	14	14	15	16	ъĘ	
	B-port input, A-port output	$t_r = t_f = 1 \text{ ns}$	3	3	3	3	4	pF	

(1) Power-dissipation capacitance per transceiver

#### **Power-Up Considerations**

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

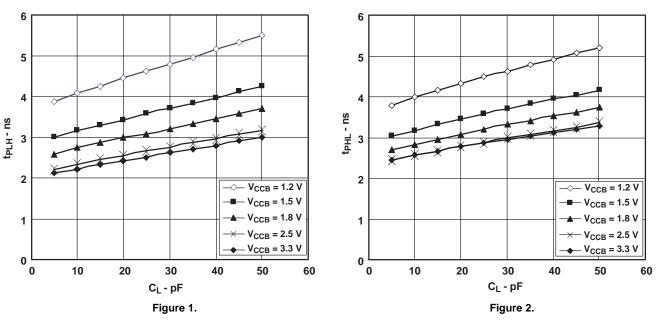
- 1. Connect ground before any supply voltage is applied.
- 2. Power up  $V_{CCA}$ .
- 3.  $V_{CCB}$  can be ramped up along with or after  $V_{CCA}$ .

V	V <sub>CCA</sub>											
V <sub>CCB</sub>	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	UNIT					
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5						
1.2 V	<0.5	<1	<1	<1	<1	1						
1.5 V	<0.5	<1	<1	<1	<1	1						
1.8 V	<0.5	<1	<1	<1	<1	<1	μA					
2.5 V	<0.5	1	<1	<1	<1	<1						
3.3 V	<0.5	1	<1	<1	<1	<1						

#### Table 1. Typical Total Static Power Consumption (I<sub>CCA</sub> + I<sub>CCB</sub>)

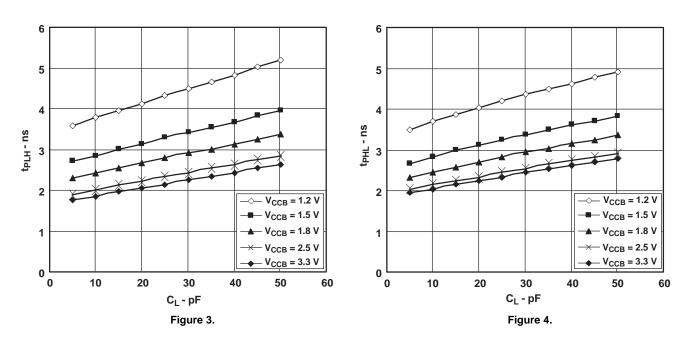


#### **TYPICAL CHARACTERISTICS**



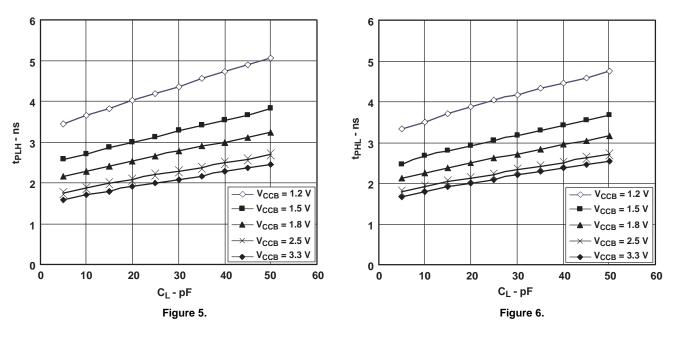
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,  $T_{\rm A}$  = 25°C,  $V_{\rm CCA}$  = 1.2 V

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,  $T_{\rm A}$  = 25°C,  $V_{\rm CCA}$  = 1.5 V



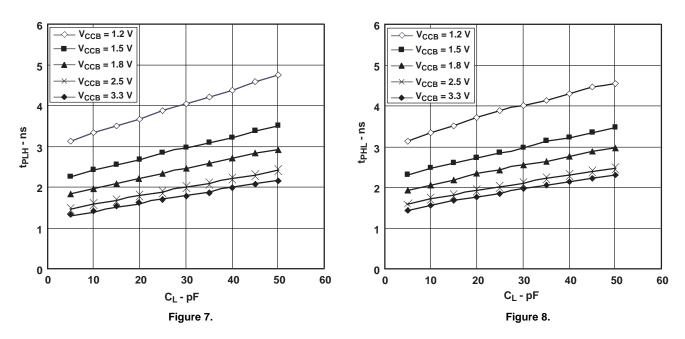


#### **TYPICAL CHARACTERISTICS**



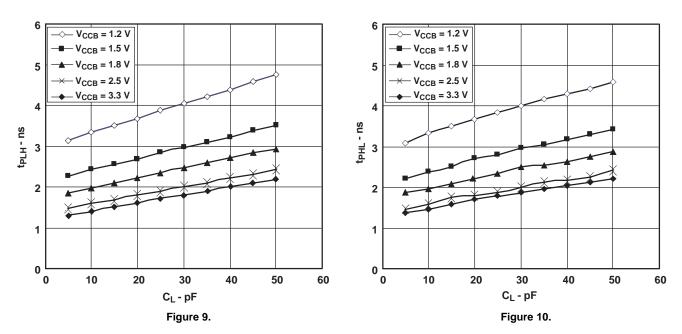
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,  $T_{A}$  = 25°C,  $V_{CCA}$  = 1.8 V

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,  $T_{\rm A}$  = 25°C,  $V_{\rm CCA}$  = 2.5 V





#### **TYPICAL CHARACTERISTICS**

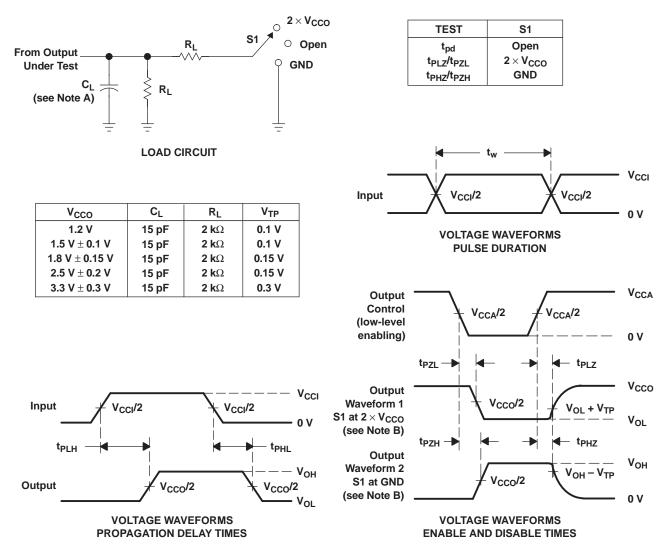


# TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, $T_{\text{A}}$ = 25°C, $V_{\text{CCA}}$ = 3.3 V

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SCES598D-JULY 2004-REVISED JANUARY 2008



PARAMETER MEASUREMENT INFORMATION

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>0</sub> = 50  $\Omega$ , dv/dt  $\geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

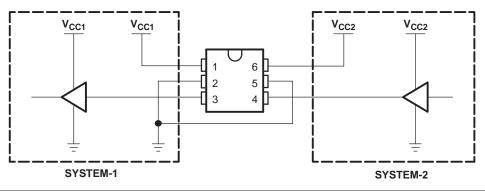
#### Figure 11. Load Circuit and Voltage Waveforms

#### SN74AVCH1T45 SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS SCES598D-JULY 2004-REVISED JANUARY 2008



**APPLICATION INFORMATION** 

Figure 12 shows an example of the SN74AVCH1T45 being used in a unidirectional logic level-shifting application.



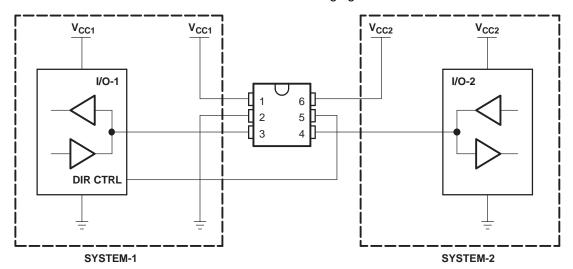
PIN	NAME	FUNCTION	DESCRIPTION
1	V <sub>CCA</sub>	V <sub>CC1</sub>	SYSTEM-1 supply voltage (1.2 V to 3.36 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V <sub>CC1</sub> voltage.
4	В	IN	Input threshold value depends on V <sub>CC2</sub> voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V <sub>CCB</sub>	V <sub>CC2</sub>	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

Figure 12. Unidirectional Logic Level-Shifting Application

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#### APPLICATION INFORMATION

Figure 13 shows the SN74AVCH1T45 being used in a bidirectional logic level-shifting application. Since the SN74AVCH1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	Н	Out	In	SYSTEM-1 data to SYSTEM-2
2	н	Hi–Z	Hi–Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Hi–Z	Hi–Z	DIR bit is flipped. I/O-1 and I/O02 still are disabled. The bus-line state depends on bus hold.
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

#### Figure 13. Bidirectional Logic Level-Shifting Application

Following is a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

#### **Enable Times**

Calculate the enable times for the SN74AVCH1T45 using the following formulas:

- $t_{PZH}$  (DIR to A) =  $t_{PLZ}$  (DIR to B) +  $t_{PLH}$  (B to A)
- $t_{PZL}$  (DIR to A) =  $t_{PHZ}$  (DIR to B) +  $t_{PHL}$  (B to A)
- $t_{PZH}$  (DIR to B) =  $t_{PLZ}$  (DIR to A) +  $t_{PLH}$  (A to B)
- $t_{PZL}$  (DIR to B) =  $t_{PHZ}$  (DIR to A) +  $t_{PHL}$  (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVCH1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.



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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74AVCH1T45DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCH1T45DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH1T45DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH1T45DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH1T45DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCH1T45YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

# PACKAGE OPTION ADDENDUM



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30-Jan-2012

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

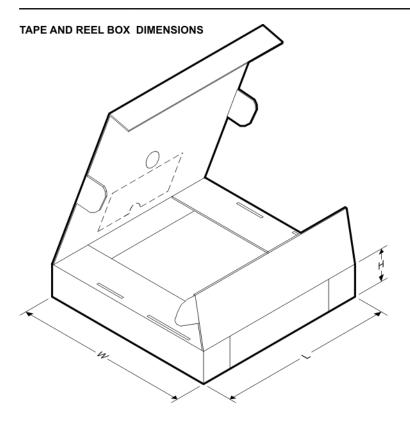
*All dimensions are nominal												-
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.52	1.2	4.0	8.0	Q3
SN74AVCH1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74AVCH1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74AVCH1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.52	1.2	4.0	8.0	Q3
SN74AVCH1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

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# PACKAGE MATERIALS INFORMATION

3-Apr-2012



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH1T45DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AVCH1T45DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AVCH1T45DCKR	SC70	DCK	6	3000	214.0	199.0	55.0
SN74AVCH1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AVCH1T45DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AVCH1T45DCKT	SC70	DCK	6	250	214.0	199.0	55.0
SN74AVCH1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- È. Falls within JEDEC MO-178 Variation AB, except minimum lead width.



### LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.



# LAND PATTERN DATA



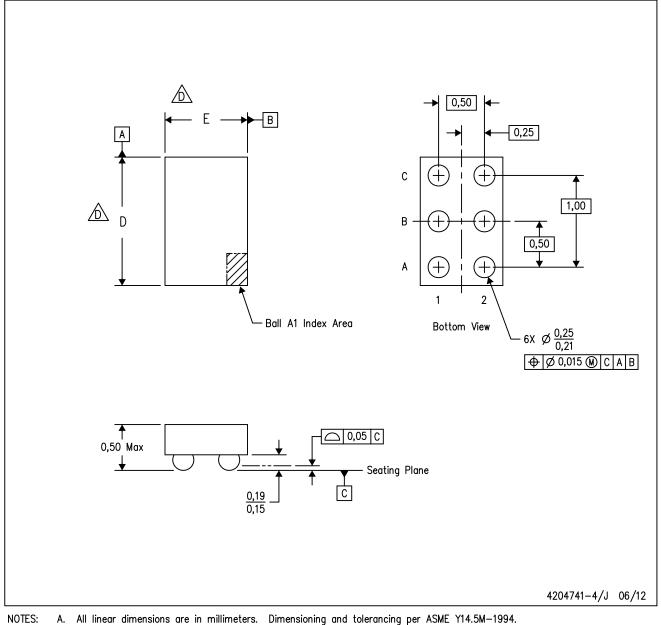
NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.





20-May-2013

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	· · · · ·	Op Temp (°C)	Device Marking	Samples
74AVCH1T45DBVRE4	(1) ACTIVE	SOT-23	DBV	6	3000	(2) Green (RoHS & no Sb/Br)	CU NIPDAU	(3) Level-1-260C-UNLIM	-40 to 85	(4/5) (ET1F ~ ET1R)	Samples
74AVCH1T45DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F ~ ET1R)	Samples
74AVCH1T45DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F ~ ET1R)	Samples
74AVCH1T45DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F ~ ET1R)	Samples
74AVCH1T45DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF ~ TFR)	Samples
74AVCH1T45DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF ~ TFR)	Samples
74AVCH1T45DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF ~ TFR)	Samples
74AVCH1T45DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF ~ TFR)	Samples
SN74AVCH1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F ~ ET1R)	Samples
SN74AVCH1T45DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F ~ ET1R)	Samples
SN74AVCH1T45DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF ~ TFR)	Samples
SN74AVCH1T45DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF ~ TFR)	Samples
SN74AVCH1T45YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TE2 ~ TE7 ~ TEN)	Samples

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



# PACKAGE OPTION ADDENDUM

20-May-2013

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(<sup>5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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# PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74AVCH1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.52	1.2	4.0	8.0	Q3
SN74AVCH1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74AVCH1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.52	1.2	4.0	8.0	Q3
SN74AVCH1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

26-Jan-2013



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH1T45DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AVCH1T45DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AVCH1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AVCH1T45DCKR	SC70	DCK	6	3000	214.0	199.0	55.0
SN74AVCH1T45DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AVCH1T45DCKT	SC70	DCK	6	250	214.0	199.0	55.0
SN74AVCH1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- È. Falls within JEDEC MO-178 Variation AB, except minimum lead width.



### LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.



# LAND PATTERN DATA



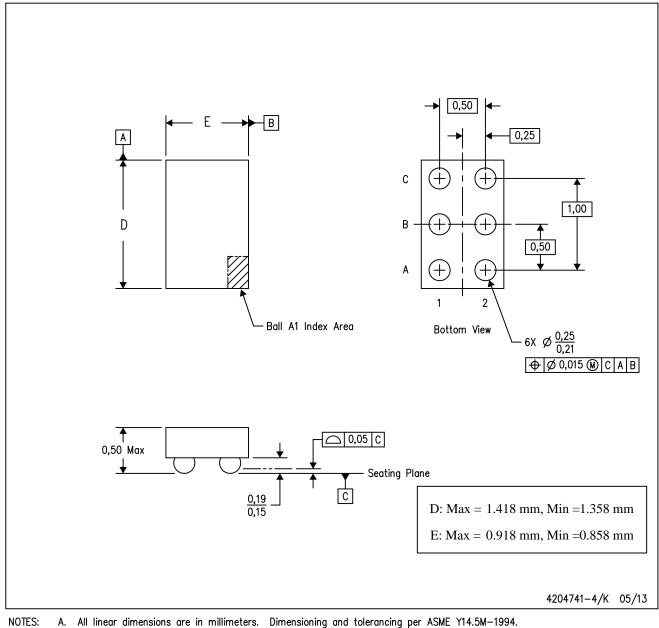
NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- Α.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

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