

IEC LEVEL 4 ESD-PROTECTED 0.75-Ω SPDT ANALOG SWITCH WITH 1.8-V COMPATIBLE INPUT LOGIC

Check for Samples: [TS5A12301E](#)

FEATURES

- Low ON-State Resistance (0.75 Ω)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Isolation in Power-Down Mode, $V_{+} = 0$
- Specified Break-Before-Make Switching
- 2.25-V to 5.5-V Power Supply (V_{+})
- 6-MΩ Input Pulldown Allows Control Input (IN) to Be Unconnected
- 1.8-V Compatible Control Input Threshold Independent of V_{+}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 3000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- ESD Performance COM Port to GND
 - 8000-V Human-Body Model (A114-B, Class II)
 - ±8-kV Contact Discharge (IEC 61000-4-2)
 - ±15-kV Air-Gap Discharge (IEC 61000-4-2)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- MP3 Players
- Portable Media Players

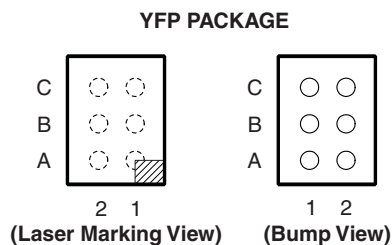


Table 1. TERMINAL ASSIGNMENTS

C	V_{+}	NC
B	COM	GND
A	IN	NO
	2	1

DESCRIPTION/ORDERING INFORMATION

The TS5A12301E is a single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers a low ON-state resistance with an excellent channel-to-channel ON-state resistance matching, and the break-before-make feature to prevent signal distortion during the transferring of a signal from one path to another.

The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. The control input (IN) pin can be connected to low-voltage GPIOs, allowing it to be controlled by 1.8-V signals.

The TS5A12301E has ±15-kV Air-Gap Discharge and ±8-kV Contact Discharge ESD protection for the COM port to GND, which make it compliant with the IEC Level 4 ESD standard (IEC 61000-4-2).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 2. ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	WCSP (DSBGA) 0.4-mm Pitch – YFP (Pb-free)	Tape and reel	TS5A12301EYFPR	___3W_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

SUMMARY OF CHARACTERISTICS⁽¹⁾

Configuration	2:1 Multiplexer/Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance (r _{on})	0.75 Ω max
ON-state resistance match (Δr _{on})	0.1 Ω max
ON-state resistance flatness (r _{on(flat)})	0.1 Ω max
Turn-on/turn-off time (t _{ON} /t _{OFF})	110 ns/100 ns
Break-before-make time (t _{BBM})	10 ns
Charge injection (Q _C)	97 pC
Bandwidth (BW)	55 MHz
OFF isolation (O _{ISO})	-63 dB at 1 MHz
Crosstalk (X _{TALK})	-63 dB at 1 MHz
Total harmonic distortion (THD)	0.003%
Leakage current (I _{NO(OFF)} /I _{NC(OFF)})	20 nA
Package option	6-pin WCSP, 0.4-mm pitch

(1) V₊ = 5 V, T_A = 25°C

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L or Open	ON	OFF
H	OFF	ON

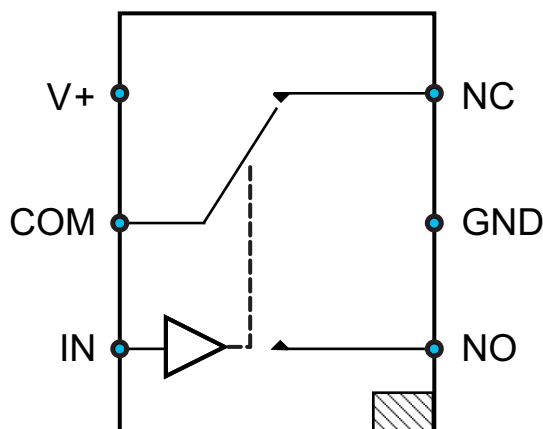


Figure 1. Logic Diagram

ABSOLUTE MAXIMUM RATINGS^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range ⁽³⁾		-0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range ^{(3) (4) (5)}		-0.5	$V_+ + 0.5$	V
I_{IK}	Analog port diode current	$V_+ < V_{NC}, V_{NO}, V_{COM}$ or $V_{NC}, V_{NO}, V_{COM} < 0$	-50	50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	$V_{NC}, V_{NO}, V_{COM} = 0$ to V_+	-450	450	mA
	On-state peak switch current ⁽⁶⁾		-700	700	
V_I	Digital input voltage range ^{(3) (4)}		-0.5	6.5	V
I_{IK}	Digital input clamp current	$V_I < 0$	-50		mA
I_+ I_{GND}	Continuous current through V_+ or GND		-100	100	mA
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle

THERMAL IMPEDANCE RATINGS

			UNIT	
θ_{JA}	Package thermal impedance ⁽¹⁾	YFP package	154.2	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY⁽¹⁾
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V
ON-state resistance	r_{on}	V_{NO} or $V_{NC} = 2.5\text{ V}$, $I_{COM} = -100\text{ mA}$, See Figure 15	25°C Full	4.5 V		0.5	0.75 0.8	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or $V_{NC} = 2.5\text{ V}$, $I_{COM} = -100\text{ mA}$, See Figure 15	25°C Full	4.5 V		0.05	0.1 0.1	Ω
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100\text{ mA}$, See Figure 15	25°C	4.5 V		0.15		Ω
		V_{NO} or $V_{NC} = 1\text{ V}, 1.5\text{ V}, 2.5\text{ V}$, $I_{COM} = -100\text{ mA}$, See Figure 15	25°C Full			0.1 0.25		
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 1\text{ V}, 4.5\text{ V}$, $V_{COM} = 4.5\text{ V}, 1\text{ V}$, $V_{NC} = \text{Open}$, or $V_{NO} = 1\text{ V}, 4.5\text{ V}$, $V_{COM} = 4.5\text{ V}, 1\text{ V}$, $V_{NC} = \text{Open}$, See Figure 16	25°C	5.5 V	-20	2	20	nA
			Full		-100		100	
	$I_{NO(PWROFF)}, I_{NC(PWROFF)}$	V_{NO} or $V_{NC} = 0$ to 5.5 V , $V_{COM} = 5.5\text{ V to }0$	25°C	0 V	-10		10	μA
			Full		-10		10	
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}, 4.5\text{ V}$, $V_{COM}, V_{NC} = \text{Open}$, or $V_{NC} = 1\text{ V}, 4.5\text{ V}$, $V_{COM}, V_{NO} = \text{Open}$, See Figure 17	25°C	5.5 V	-20	2	20	nA
			Full		-200		200	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}, 4.5\text{ V}$, V_{NO} and $V_{NC} = \text{Open}$, or $V_{COM} = 1\text{ V}, 4.5\text{ V}$, V_{NO} or $V_{NC} = \text{Open}$, See Figure 17	25°C	5.5 V	-20	2	20	nA
			Full		-200		200	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{NO} or $V_{NC} = 0$ to 5.5 V , $V_{COM} = 5.5\text{ V to }0$, See Figure 16	25°C	0 V	-10		10	μA
			Full		-10		10	
Digital Control Input (IN)								
Input logic high	V_{IH}		Full	5.5 V	1.05		5.5	V
Input logic low	V_{IL}		Full	5.5 V	0		0.65	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 1.95\text{ V or }0$	Full	5.5 V	-0.05		0.5	μA
Input resistance	r_{IN}	$V_I = 1.95\text{ V}$	Full	5.5 V		6		M Ω

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY⁽¹⁾ (continued)
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 19	25°C	5 V	110	225	ns	
				Full	4.5 V		250		
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 19	25°C	5 V	100	215	ns	
				Full	4.5 V		225		
Break-before-make time	t_{BBM}	$V_{COM} = V_+$, $R_L = 50 \Omega$,	$C_L = 35 \text{ pF}$, See Figure 20	25°C	5 V	1	10	15	ns
				Full	4.5 V	1		20	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1 \text{ nF}$, See Figure 24	25°C	5 V		97	pC	
NO OFF capacitance	$C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 18	25°C	5 V		28	pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 18	25°C	5 V		112	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 18	25°C	5 V		112	pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 18	25°C	5 V		3	pF	
Bandwidth	BW	$R_L = 50 \Omega$, Switch ON,	See Figure 21	25°C	5 V		55	MHz	
OFF isolation	O_{ISO}	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 22	25°C	5 V		-63	dB	
Crosstalk	X_{TALK}	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 23	25°C	5 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 25	25°C	5 V		0.003	%	
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND		Full	5.5 V		10	μA	

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY⁽¹⁾
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Analog Switch									
Analog signal range	V_{COM}, V_{NO}				0		V_+	V	
ON-state resistance	r_{on}	V_{NO} or $V_{NC} = 2\text{ V}$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C Full	3 V		0.75	0.9 1.2	Ω	
ON-state resistance match between channels	Δr_{on}	V_{NO} or $V_{NC} = 2\text{ V}, 0.8\text{ V}$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C Full	3 V		0.1	0.15 0.15	Ω	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C Full	3 V		0.2 0.1	0.2 0.2	Ω	
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 1\text{ V}, 3\text{ V}$, $V_{COM} = 3\text{ V}, 1\text{ V}$, $V_{NC} = \text{Open}$, or $V_{NC} = 1\text{ V}, 3\text{ V}$, $V_{COM} = 3\text{ V}, 1\text{ V}$, $V_{NO} = \text{Open}$, Switch OFF, See Figure 16	25°C	3.6 V		-20	2	20	nA
			Full						
	$I_{NO(PWROFF)}, I_{NC(PWROFF)}$	V_{NO} or $V_{NC} = 0$ to 3.6 V , $V_{COM} = 3.6\text{ V to }0$	25°C	0 V		-10		10	μA
			Full						
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}, 3\text{ V}$, V_{NC} and $V_{COM} = \text{Open}$, or $V_{NC} = 1\text{ V}, 3\text{ V}$, V_{NO} and $V_{COM} = \text{Open}$, Switch ON, See Figure 17	25°C	3.6 V		-20	2	20	nA
			Full						
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$, V_{NO} and $V_{NC} = \text{Open}$, or $V_{COM} = 3\text{ V}$, V_{NO} and $V_{NC} = \text{Open}$, See Figure 17	25°C	3.6 V		-20	2	20	nA
			Full						
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{NO} or $V_{NC} = 0$ to 3.6 V , $V_{COM} = 3.6\text{ V to }0$, See Figure 16	25°C	0 V		-10		10	μA
			Full						
Digital Control Input (IN)									
Input logic high	V_{IH}		Full	3.6 V	1.05		5.5	V	
Input logic low	V_{IL}		Full	3.6 V	0		0.65	V	
Input leakage current	I_{IH}, I_{IL}	$V_I = 1.95\text{ V or }0$	Full	3.6 V	-0.05		0.5	μA	
Input resistance	r_{IN}	$V_I = 1.95\text{ V}$	Full	3.6 V		6		M Ω	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY⁽¹⁾ (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 19	25°C	3.3 V	72	175	ns	
				Full	3 V		185		
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 19	25°C	3.3 V	105	165	ns	
				Full	3 V		170		
Break-before-make time	t_{BBM}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 20	25°C	3.3 V	1	16	30	ns
				Full	3 V	1		35	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1\text{ nF}$, See Figure 24	25°C	3.3V		97	pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 18	25°C	3.3 V		28	pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 18	25°C	3.3 V		115	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 18	25°C	3.3 V		115	pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 18	25°C	3.3 V		3	pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 21	25°C	3.3 V		54	MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	See Figure 22	25°C	3.3 V		-63	dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	See Figure 23	25°C	3.3 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 25	25°C	3.3 V		0.004	%	
Supply									
Positive supply current	I_+	$V_I = 1.95\text{ V or GND}$		25°C	3.6 V		10	μA	

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY⁽¹⁾
 $V_+ = 2.25\text{ V to }2.75\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Analog Switch									
Analog signal range	V_{COM}, V_{NO}				0		V_+	V	
ON-state resistance	r_{on}	V_{NO} or $V_{NC} = 1.8\text{ V}$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C Full	2.25 V		1.1	1.3 1.6	Ω	
ON-state resistance match between channels	Δr_{on}	V_{NO} or $V_{NC} = 1.8\text{ V}$, 0.8 V , $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C Full	2.25 V		0.15	0.2 0.2	Ω	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C	2.25 V		0.4		Ω	
		V_{NO} or $V_{NC} = 0.8\text{ V}, 1\text{ V}, 1.8\text{ V}$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 15	25°C Full			0.25	0.5 0.6		
NO, NC OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NO} = 0.5\text{ V}, 2.2\text{ V}$, $V_{COM} = 2.2\text{ V}, 0.5\text{ V}$, $V_{NC} = \text{Open}$, or $V_{NC} = 0.5\text{ V}, 2.2\text{ V}$, $V_{COM} = 2.2\text{ V}, 0.5\text{ V}$, $V_{NO} = \text{Open}$, Switch OFF, See Figure 16	25°C	2.75 V		-20	2	20	nA
			Full			-50		50	
NC, NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0.5\text{ V}, 2.2\text{ V}$, V_{NC} and $V_{COM} = \text{Open}$, or $V_{NC} = 2.2\text{ V}, 0.5\text{ V}$, V_{NO} and $V_{COM} = \text{Open}$, Switch ON, See Figure 17	25°C	2.75 V		-20	2	20	nA
			Full			-100		100	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 0.5\text{ V}$, V_{NO} and $V_{NC} = \text{Open}$, or $V_{COM} = 2.2\text{ V}$, V_{NO} and $V_{NC} = \text{Open}$, Switch ON, See Figure 17	25°C Full	2.75 V		-20	2	20	nA
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{NO} or $V_{NC} = 0$ to 2.75 V , $V_{COM} = 2.75\text{ V}$ to 0 , See Figure 16	25°C Full	0 V		-10		10	μA
						-10		10	μA
Digital Control Input (IN)									
Input logic high	V_{IH}		Full	2.75 V	1.05		5.5	V	
Input logic low	V_{IL}		Full	2.75 V	0		0.65	V	
Input leakage current	I_{IH}, I_{IL}	$V_I = 1.95\text{ V}$ or 0	Full	2.75 V	-0.05		0.5	μA	
Input resistance	r_{IN}	$V_I = 1.95\text{ V}$	Full	2.75 V		6		M Ω	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY⁽¹⁾ (continued)
 $V_+ = 2.25\text{ V to }2.75\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 19	25°C	2.5 V	97	170	ns	
				Full	2.25 V		175		
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 19	25°C	2.5 V	80	155	ns	
				Full	2.25 V		160		
Break-before-make time	t_{BBM}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 20	25°C	2.5 V	5	18	35	ns
				Full	2.25 V	5		40	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1\text{ nF}$, See Figure 24	25°C	2.5 V	82		pC	
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 18	25°C	2.5 V	29		pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 18	25°C	2.5 V	116		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 18	25°C	2.5 V	116		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 18	25°C	2.5 V	3		pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 21	25°C	2.5 V	54		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	See Figure 22	25°C	2.5 V	-63		dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	See Figure 23	25°C	2.5 V	-63		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 25	25°C	2.5 V	0.008		%	
Supply									
Positive supply current	I_+	$V_I = 1.95\text{ V or GND}$	Full	2.75 V			10	μA	

TYPICAL PERFORMANCE

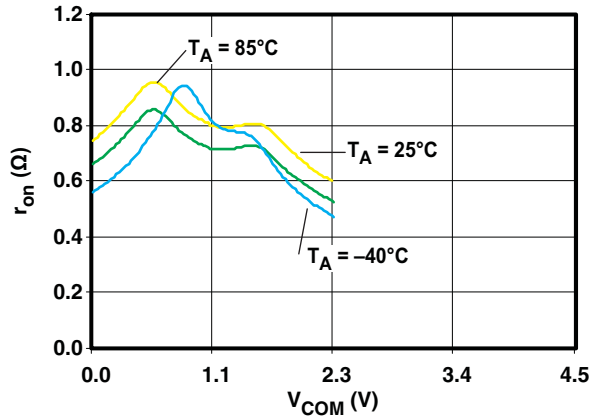


Figure 2. r_{on} vs V_{COM} ($V_+ = 2.25$ V)

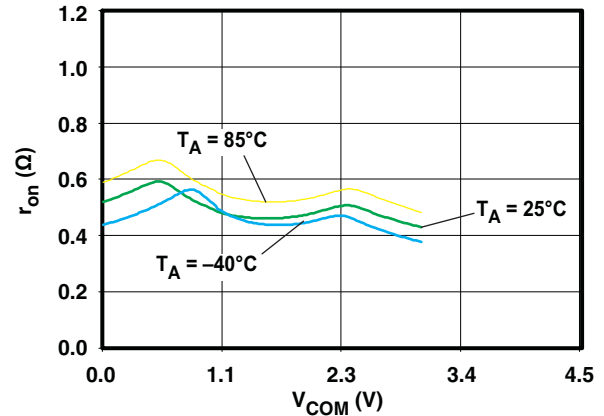


Figure 3. r_{on} vs V_{COM} ($V_+ = 3$ V)

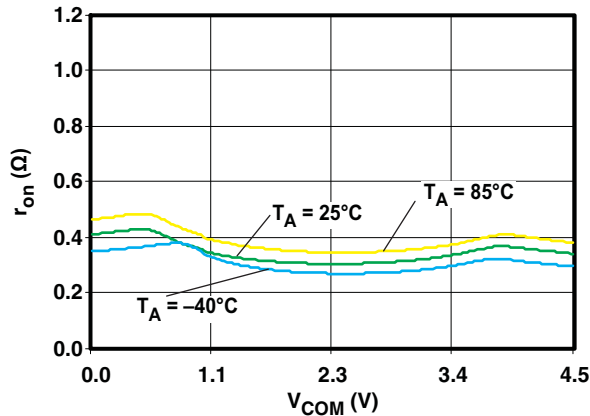


Figure 4. r_{on} vs V_{COM} ($V_+ = 4.5$ V)

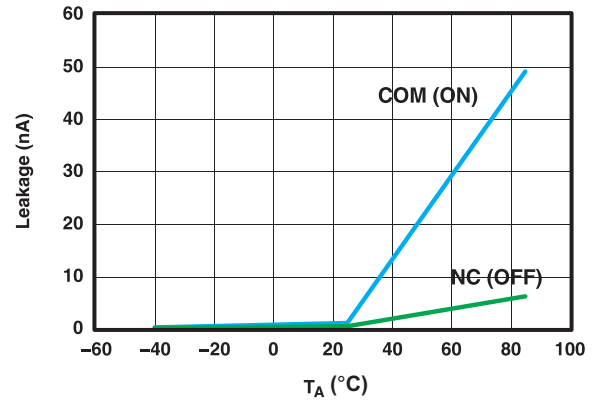


Figure 5. Leakage Current vs Temperature ($V_+ = 5$ V)

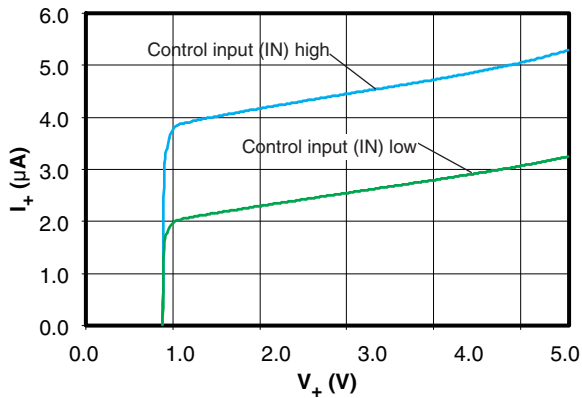


Figure 6. I_+ vs V_+ ($T_A = 25^\circ\text{C}$)

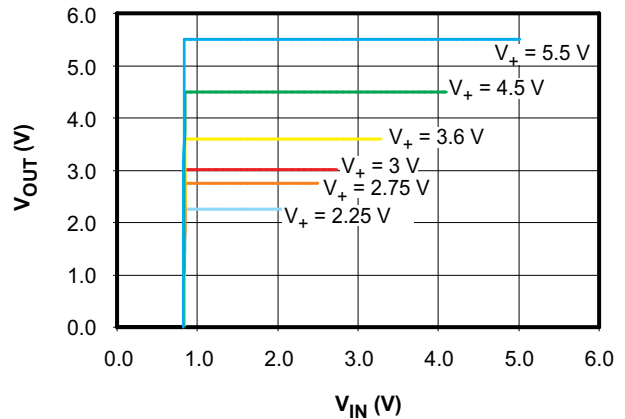


Figure 7. Control Input Thresholds

TYPICAL PERFORMANCE (continued)

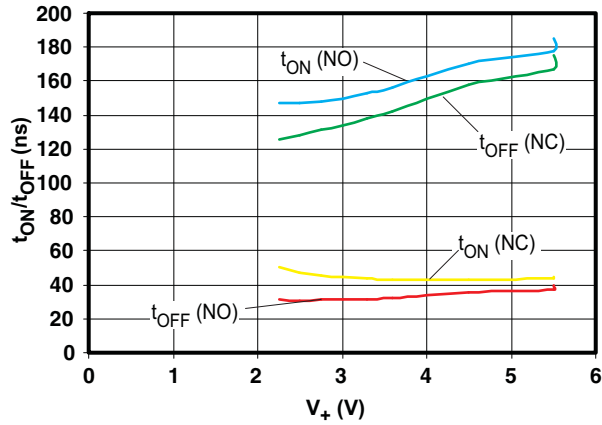


Figure 8. t_{ON}/t_{OFF} vs Supply Voltage

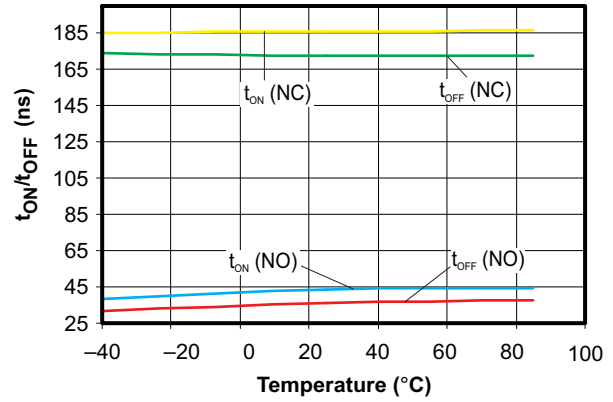


Figure 9. t_{ON}/t_{OFF} vs Temperature

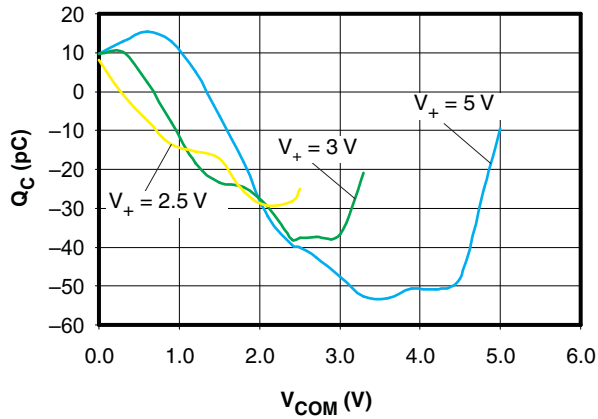


Figure 10. Charge Injection (Q_C) vs V_{COM}

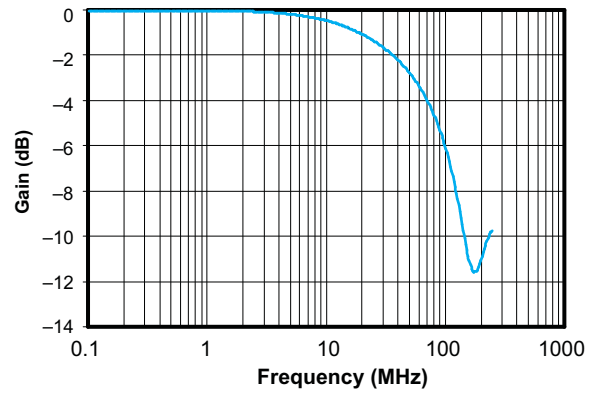


Figure 11. Gain vs Frequency

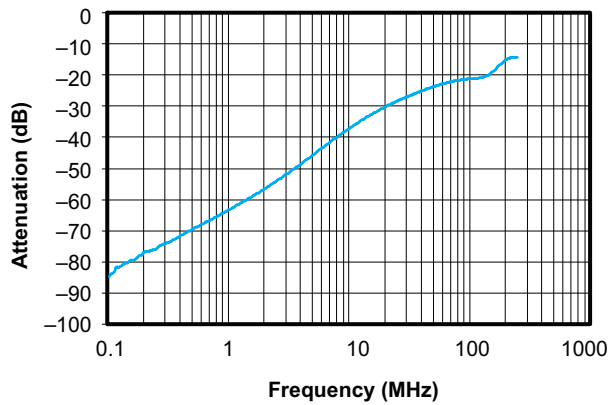


Figure 12. OFF Isolation vs Frequency

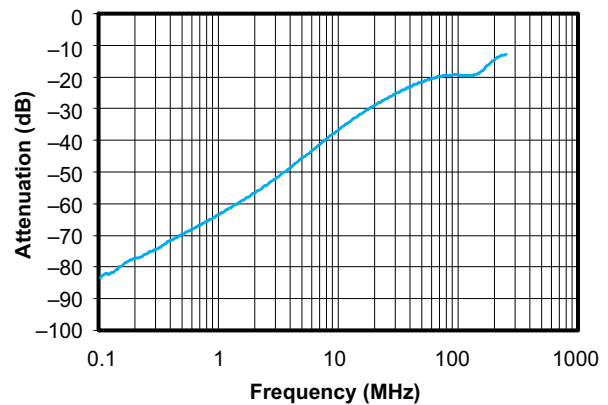


Figure 13. Crosstalk vs Frequency

TYPICAL PERFORMANCE (continued)

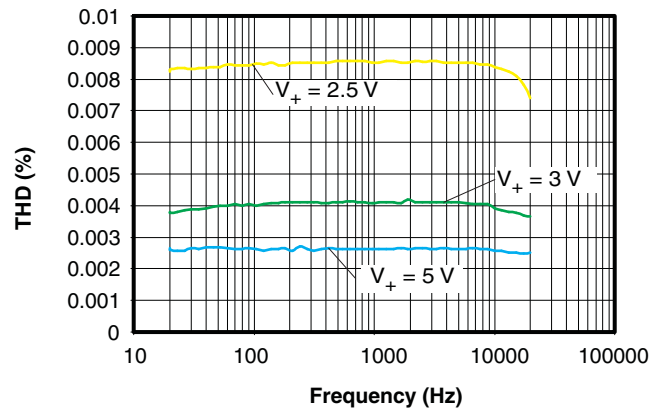


Figure 14. Total Harmonic Distortion (THD) vs Frequency

PARAMETER MEASUREMENT INFORMATION

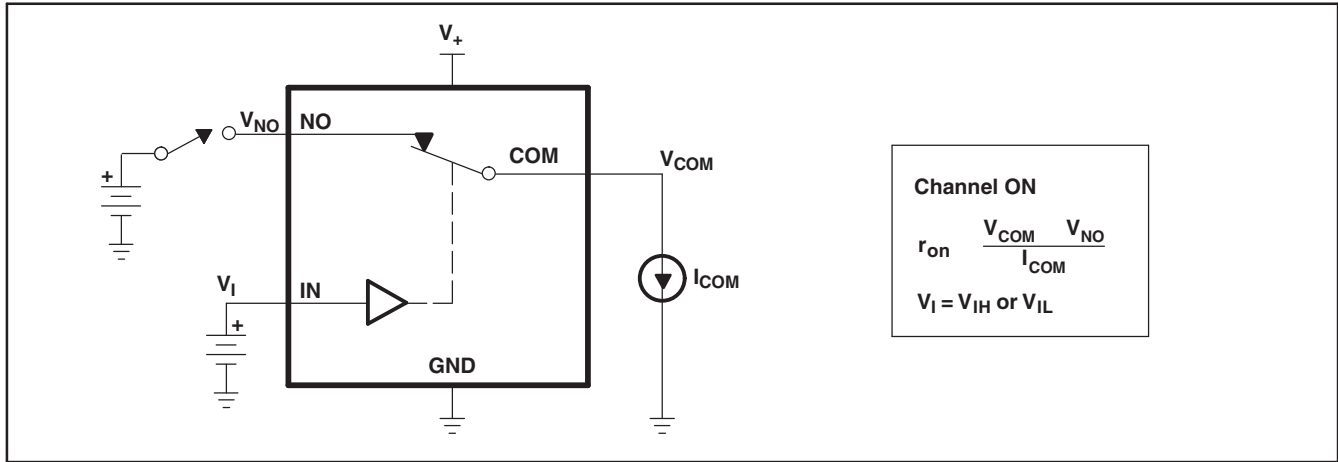


Figure 15. ON-State Resistance (r_{on})

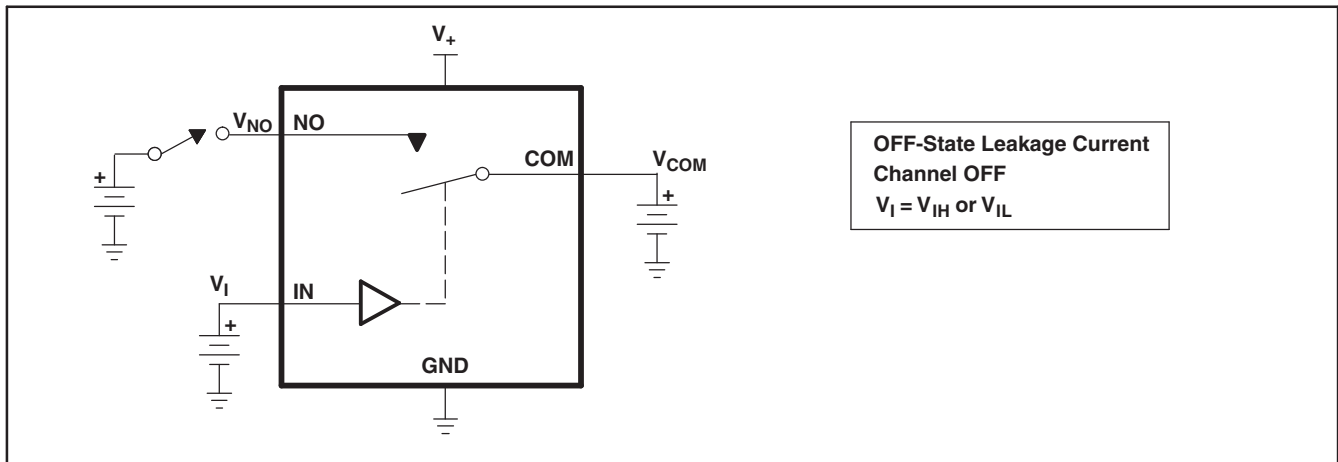


Figure 16. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWRFF)}$)

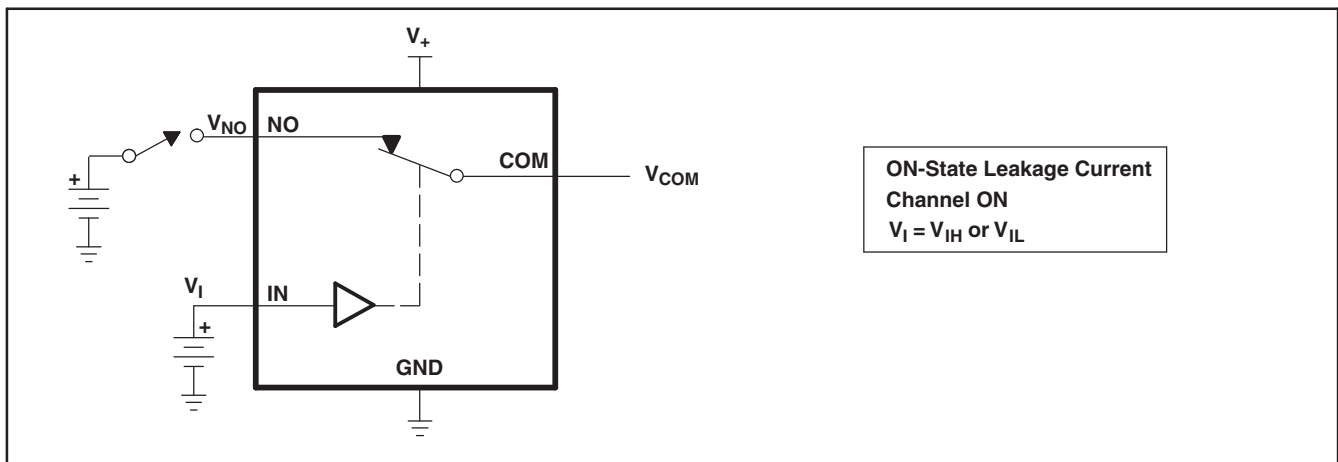


Figure 17. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

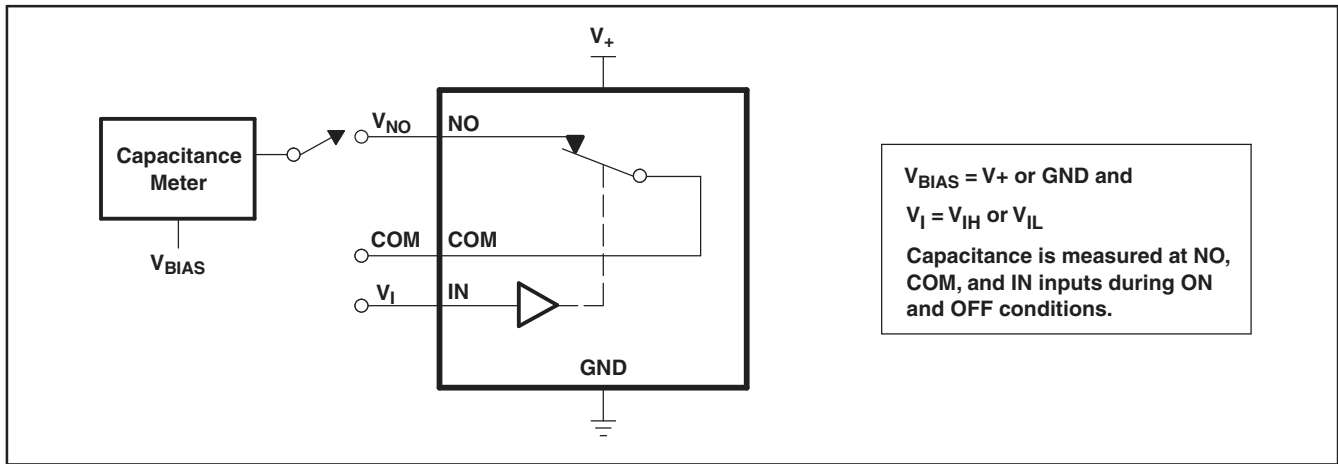
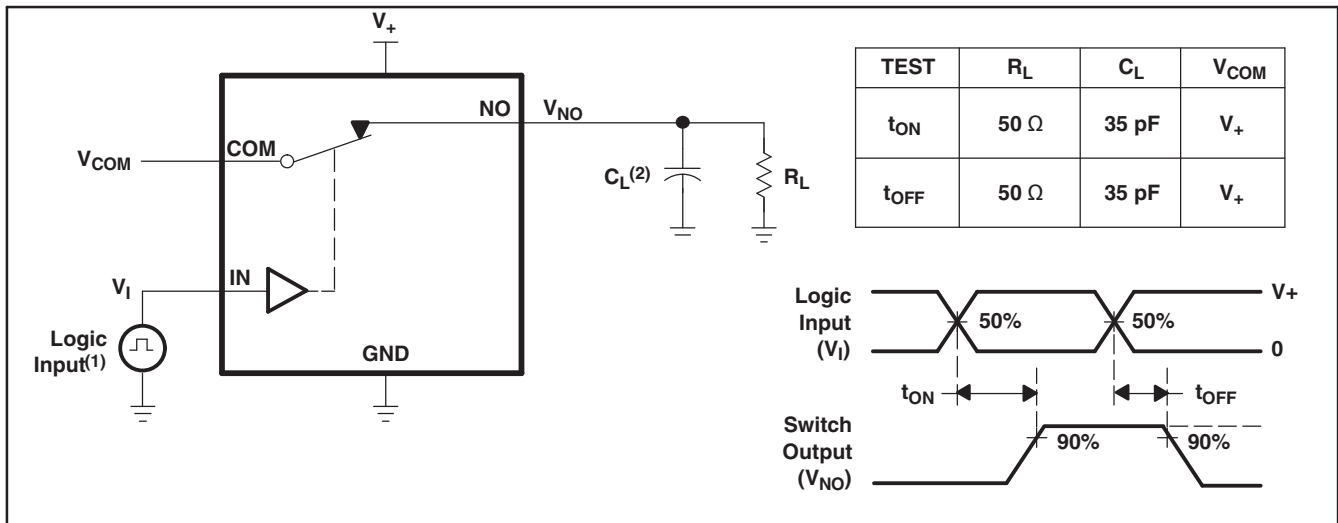


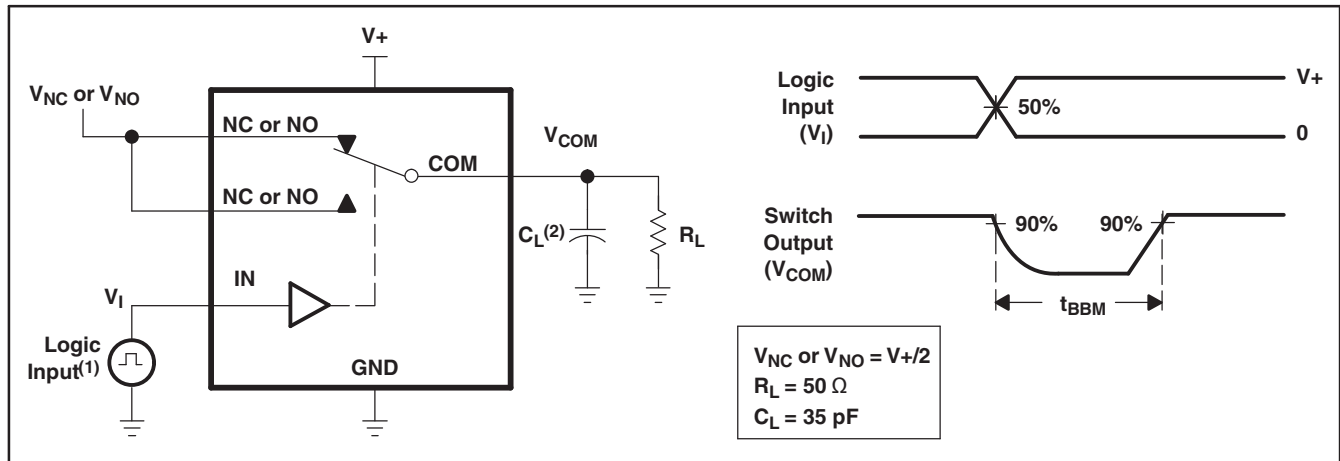
Figure 18. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 19. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

Figure 20. Break-Before-Make Time (t_{BBM})

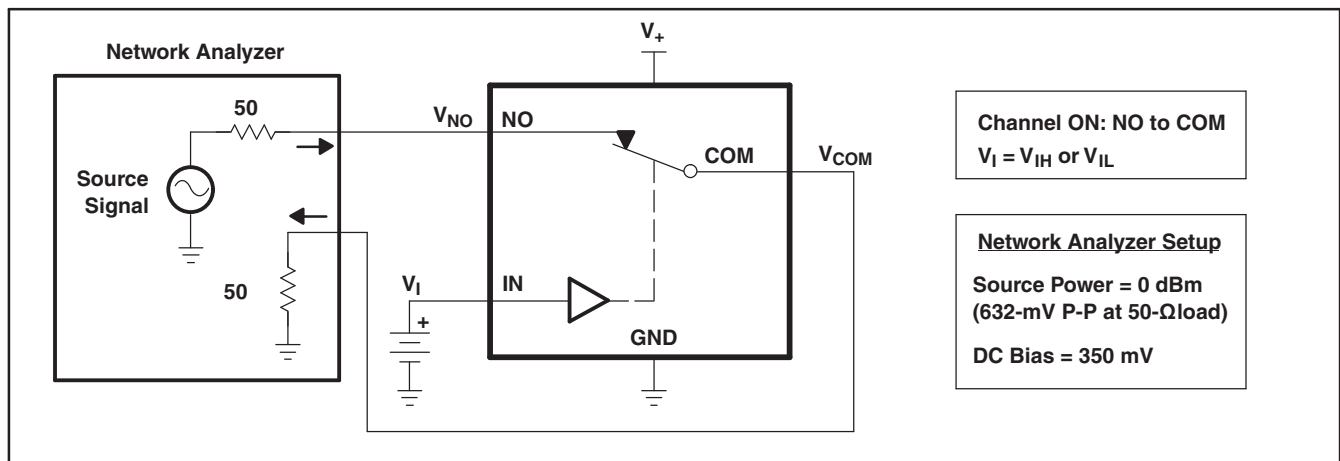


Figure 21. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

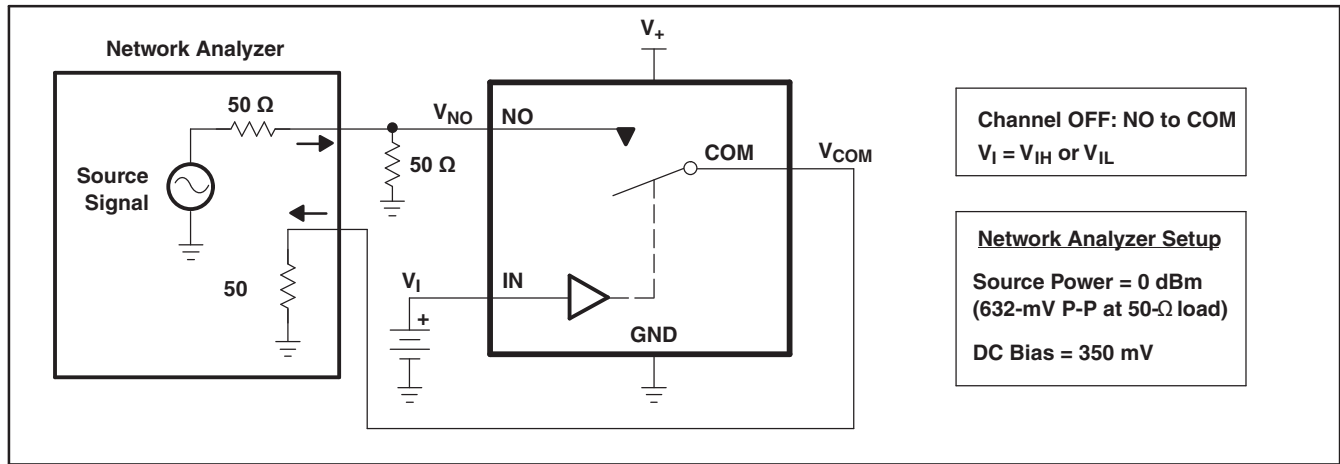


Figure 22. OFF Isolation (O_{ISO})

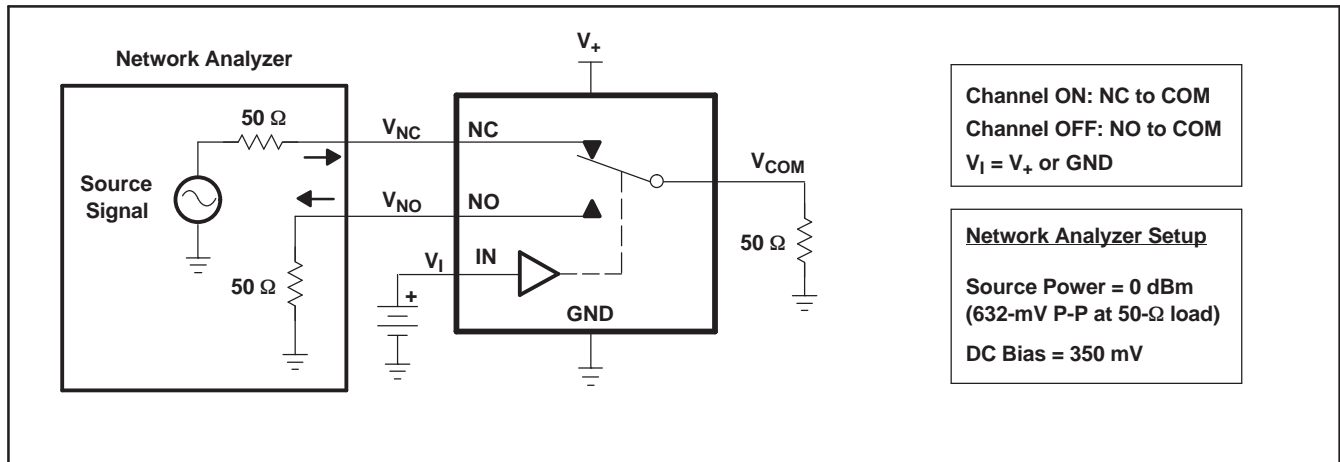
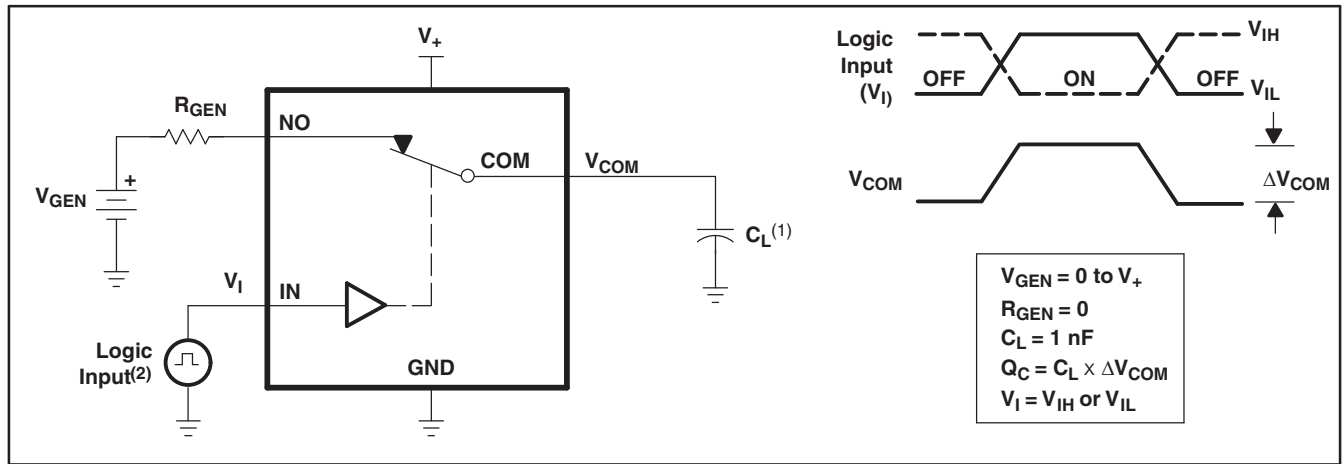


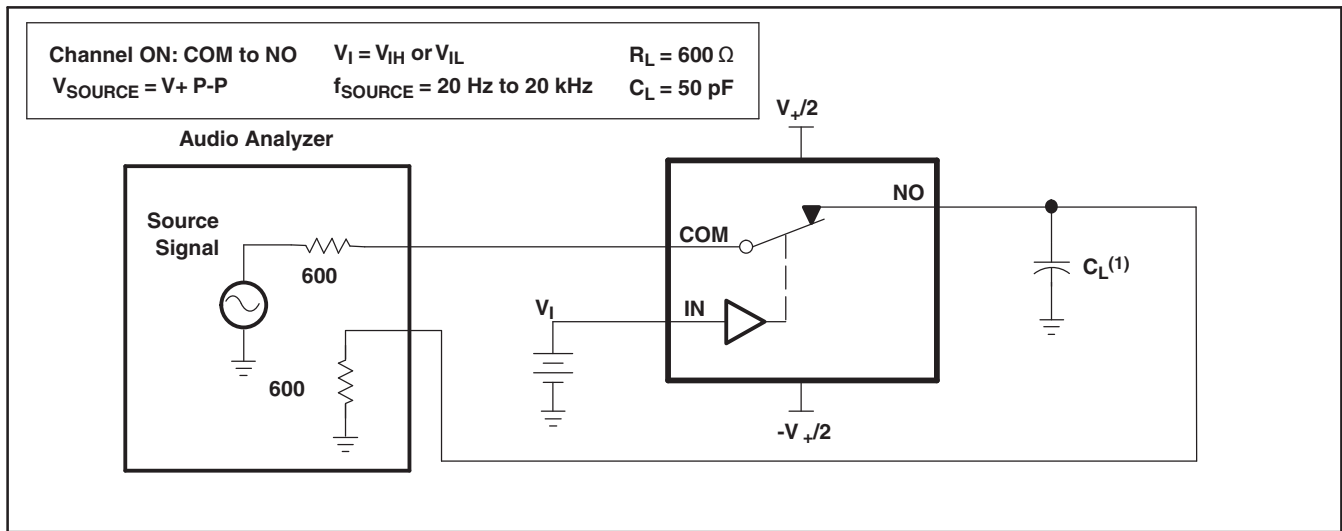
Figure 23. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

Figure 24. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

Figure 25. Total Harmonic Distortion (THD)

REVISION HISTORY

Changes from Revision A (December 2009) to Revision B	Page
• Added Logic Diagram.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A12301EYFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(3W2 ~ 3W7 ~ 3WN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A12301EYFPR	DSBGA	YFP	6	3000	180.0	8.4	0.89	1.29	0.62	4.0	8.0	Q1
TS5A12301EYFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A12301EYFPR	DSBGA	YFP	6	3000	220.0	220.0	34.0
TS5A12301EYFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

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