

# SINGLE POSITIVE EDGE TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

#### **FEATURES**

- Controlled Baseline
  - One Assembly Site
  - One Test Site
  - One Fabrication Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Supports 5-V V<sub>CC</sub> Operation
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 7.9 ns at 3.3 V
- Low Power Consumption, 10 μA Max I<sub>CC</sub>
- ±24 mA Output Drive at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial Power Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### DCU PACKAGE (TOP VIEW)



#### DESCRIPTION/ORDERING INFORMATION

This single positive edge triggered D-type flip-flop is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial power down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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## ORDERING INFORMATION(1)

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING (3)
-55°C to 125°C	VSSOP - DCU	Reel of 250	SN74LVC2G74MDCUTEP	CHB

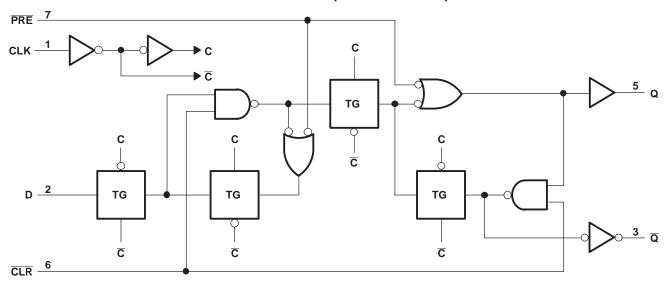
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCU: The actual top-side marking has one additional character that designates the assembly/test site.

#### **FUNCTION TABLE**

INPUTS			OUTI	PUTS	
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	Χ	L	Н
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
Н	Н	<b>↑</b>	Н	Н	L
Н	Н	<b>↑</b>	L	L	Н
Н	Н	L	X	$Q_0$	$\overline{Q}_{0}$

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

## **LOGIC DIAGRAM (POSITIVE LOGIC)**





# Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
$V_{I}$	Input voltage range <sup>(2)</sup>		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-	impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
Vo	Voltage range applied to any output in the high	or low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCU package		227	°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



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# Recommended Operating Conditions<sup>(1)</sup>

		<u>.</u>	MIN	MAX	UNIT
.,	Complexionality	Operating	1.65	5.5	
$V_{CC}$	Supply voltage	Data retention only	1.5		V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			
\	High lavel input valtage				
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
\	Low lovel input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V <sub>I</sub>	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
$I_{OH}$	High-level output current	level output current V <sub>CC</sub> = 3 V		-16	mA
				-24	
		V <sub>CC</sub> = 4.5 V		-24	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2V		16	mA
		$V_{CC} = 3 V$		24	
		V <sub>CC</sub> = 4.5 V		24	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
T <sub>A</sub>	Operating free-air temperature	·	-55	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

Р	PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN TYP <sup>(1)</sup> MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2	
\/		I <sub>OH</sub> = -8 mA	2.3 V	1.9	V
V <sub>OH</sub>		$I_{OH} = -16 \text{ mA}$	3 V	2.4	V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3	
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.8	
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1	
		I <sub>OL</sub> = 4 mA	1.65 V	0.45	
\/		I <sub>OL</sub> = 8 mA	2.3 V	0.3	V
V <sub>OL</sub>		I <sub>OL</sub> = 16 mA	3 V	0.4	V
		I <sub>OL</sub> = 24 mA	3 V	0.55	
		I <sub>OL</sub> = 24 mA	4.5 V	0.55	
I <sub>I</sub>	Data or control inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	±5	μΑ
I <sub>off</sub>		$V_I$ or $V_O = 5.5 \text{ V}$	0	±10	μΑ
I <sub>CC</sub>		$V_1 = 5.5 \text{ V or GND}, \qquad I_0 = 0$	1.65 V to 5.5 V	10	μΑ
$\Delta I_{\text{CC}}$		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V	500	μΑ
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V	5	pF

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

# **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V	
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>				175		200	MHz
	Dulas dimetias	CLK	2.7		2		
t <sub>w</sub>	Pulse duration	PRE or CLR low	2.7		2		ns
	Octor Cocc hafana Olika	Data	1.3		1.1		
t <sub>su</sub>	t <sub>su</sub> Setup time, before CLK↑	PRE or CLR inactive	1.2		1.2		ns
t <sub>h</sub>	Hold time, data after CLK↑		1.2		0.5		ns

## **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER FROM		TO	V <sub>CC</sub> = ± 0.3	3.3 V 3 V	V <sub>CC</sub> = ± 0.5	5 V 5 V	UNIT
	(INPUT)	INPUT) (OUTPUT)	MIN	MAX	MIN	MAX	
f <sub>max</sub>			175		200		MHz
	CLK	Q	2.2	7.9	1.4	6.1	
t <sub>pd</sub>	CLK	ā	2.6	8.2	1.6	6.4	ns
	PRE or CLR	Q or Q	1.7	7.9	1.6	6.1	

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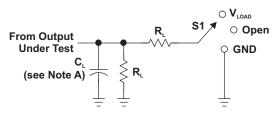
# **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 3.3 V TYP	V <sub>CC</sub> = 5 V TYP	UNIT
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	37	40	pF



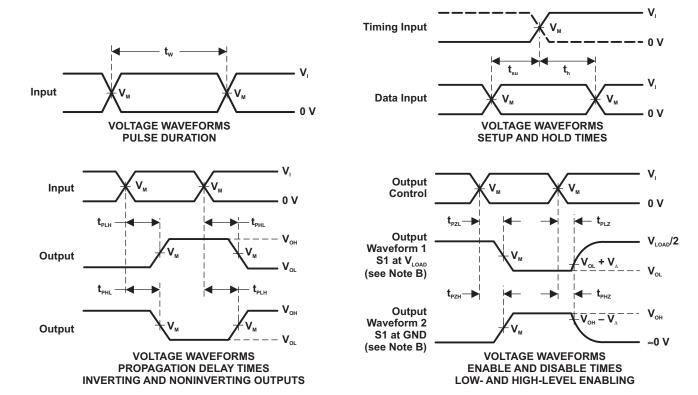
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

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.,	INI	PUTS	V V			-	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>L</sub>	$R_{\scriptscriptstyle L}$	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
$2.5~V~\pm~0.2~V$	$V_{cc}$	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>500</b> Ω	0.15 V
$3.3~V~\pm~0.3~V$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V
5 V ± 0.5 V	$V_{cc}$	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	<b>500</b> Ω	0.3 V



NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{o}$  = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $\dot{t}_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{\text{PZL}}$  and  $t_{\text{PZH}}$  are the same as  $t_{\text{en}}$ .
- G.  $t_{\mbox{\tiny PLH}}$  and  $t_{\mbox{\tiny PHL}}$  are the same as  $t_{\mbox{\tiny pd}}.$
- H. All parameters and waveforms are not applicable to all devices.

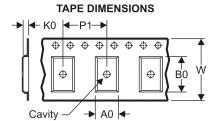
Figure 1. Load Circuit and Voltage Waveforms

# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G74MDCUTEP	US8	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G74MDCUTEP	US8	DCU	8	250	202.0	201.0	28.0

# DCU (R-PDSO-G8)

# PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



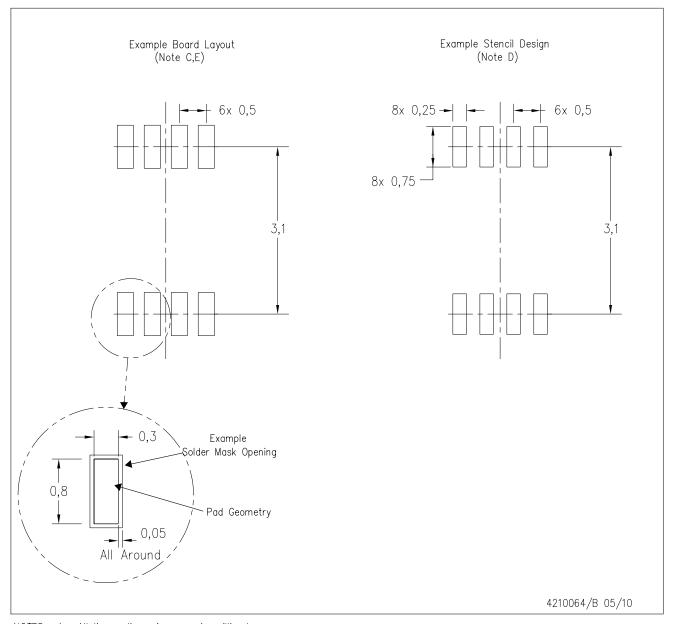
NOTES:

- : A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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