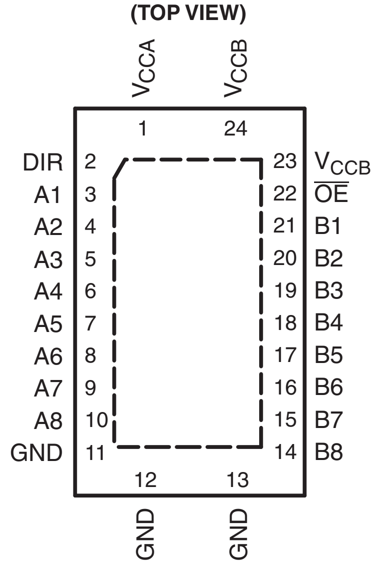
8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: SN74AVC8T245-Q1

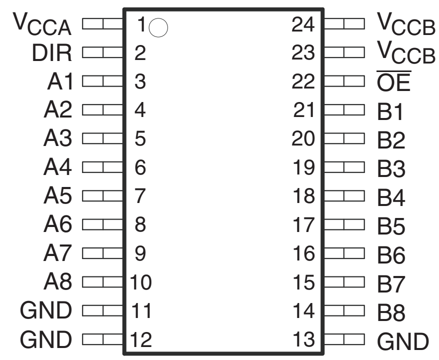
FEATURES

- Qualified for Automotive Applications
- AEC Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Control Inputs V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All I/O Ports Are in the High-Impedance State
- I_{off} Supports Partial Power-Down-Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- Maximum Data Rates
  - 170 Mbps (V_{CCA} < 1.8 V or V_{CCB} < 1.8 V)
  - 320 Mbps (V_{CCA} ≥ 1.8 V and V_{CCB} ≥ 1.8 V)
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II

RHL PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 8-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVC8T245 operation is optimimal with V_{CCA} and V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA} and V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC8T245 design enables asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. one can use the output-enable ($\overline{OE}$) input to disable the outputs so the buses are effectively isolated.

In the SN74AVC8T245 design, V_{CCA}supplies the control pins (DIR and $\overline{OE}$).

The SN74AVC8T245 solution is compatible with a single-supply system, which a '245 function can replace later with minimal printed-circuit-board redesign.

This device specification covers partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through a powered-down device.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

ORDERING INFORMATION[1]

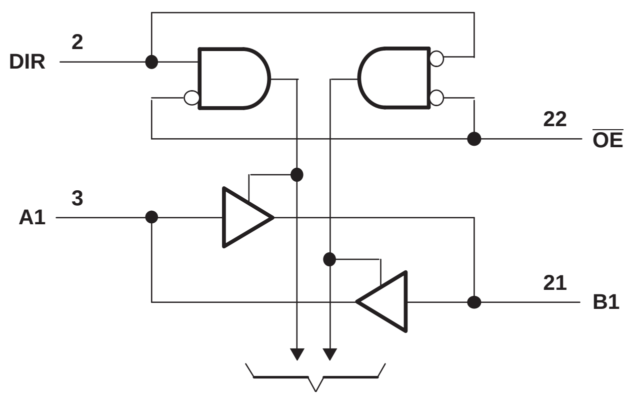
T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	QFN – RHL	Reel of 1000	CAVC8T245QRHLRQ1	WE245Q
	TSSOP – PW	Reel of 2000	SN74AVC8T245QPWRQ1	WE245Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (Each 8-Bit Section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All outputs Hi-Z

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

V_{CCA} V_{CCB}	Supply voltage range		–0.5 V to 4.6 V
V_I	Input voltage range[2]	I/O ports (A port)	–0.5 V to 4.6 V
		I/O ports (B port)	–0.5 V to 4.6 V
		Control inputs	–0.5 V to 4.6 V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5 V to 4.6 V
		B port	–0.5 V to 4.6 V
V_O	Voltage range applied to any output in the high or low state[2] [3]	A port	–0.5 V to (V_{CCA} + 0.5) V
		B port	–0.5 V to (V_{CCB} + 0.5) V
I_{IK}	Input clamp current	$V_I < 0$	–50 mA
I_{OK}	Output clamp current	$V_O < 0$	–50 mA
I_O	Continuous output current		±50 mA
	Continuous current through V_{CCA}, V_{CCB}, or GND		±100 mA
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electrostatic discharge	Human-body model (HBM) AEC-Q100 Classification Level H2	2 kV
		Charged-device model (CDM) AEC-Q100 Classification Level C3B	750 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The device withstands voltages in excess of input voltage and output negative-voltage ratings while operating within the input and output current ratings.
(3) The device withstands voltages in excess of the output positive-voltage rating up to 4.6 V maximum while operating within the output current rating.

THERMAL INFORMATION

THERMAL METRIC[1]		SN74AVC8T245-Q1	UNIT
		RHL	
		24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	35	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	39.9	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	13.8	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS[(1) (2) (3)]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt / Δv	Input transition rise or fall rate					5	ns / V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Hold all unused data inputs of the device at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS[1] [2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.15				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1		±5	µA
				0 V to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ} [3]	A or B port	$V_O = V_{CCO}$ or GND, $\overline{V_I} = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND[4], I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					15	µA
				0 V	3.6 V					–2	
				3.6 V	0 V					15	
I_{CCB}		$V_I = V_{CCI}$ or GND[4], I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					15	µA
				0 V	3.6 V					15	
				3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					25	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5				pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6				pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) Hold all unused data inputs of the device at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.1	2.6	2.5	3	3.5	ns
t_{PHL}			3.1	2.6	2.5	3	3.5	
t_{PLH}	B	A	3.1	2.7	2.5	2.4	2.3	ns
t_{PHL}			3.1	2.7	2.5	2.4	2.3	
t_{PZH}	$\overline{OE}$	A	5.3	5.3	5.3	5.3	5.3	ns
t_{PZL}			5.3	5.3	5.3	5.3	5.3	
t_{PZH}	$\overline{OE}$	B	5.1	4	3.5	3.2	3.1	ns
t_{PZL}			5.1	4	3.5	3.2	3.1	
t_{PHZ}	$\overline{OE}$	A	4.8	4.8	4.8	4.8	4.8	ns
t_{PLZ}			4.8	4.8	4.8	4.8	4.8	
t_{PHZ}	$\overline{OE}$	B	4.7	4	4.1	4.3	5.1	ns
t_{PLZ}			4.7	4	4.1	4.3	5.1	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.5	14.7	0.5	13.3	0.5	13.9	0.5	17.2	ns
t_{PHL}			2.7	0.5	14.7	0.5	13.3	0.5	13.9	0.5	17.2	
t_{PLH}	B	A	2.6	0.5	14.7	0.5	14.2	0.5	13.5	0.5	13.2	ns
t_{PHL}			2.6	0.5	14.7	0.5	14.2	0.5	13.5	0.5	13.2	
t_{PZH}	$\overline{OE}$	A	3.7	0.5	20.5	0.5	20.5	0.5	20.5	0.5	20.5	ns
t_{PZL}			3.7	0.5	20.5	0.5	20.5	0.5	20.5	0.5	20.5	
t_{PZH}	$\overline{OE}$	B	4.8	0.5	18.6	0.5	17.7	0.5	15.1	0.5	14.4	ns
t_{PZL}			4.8	0.5	18.6	0.5	17.7	0.5	15.1	0.5	14.4	
t_{PHZ}	$\overline{OE}$	A	3.1	0.5	20.3	0.5	20.3	0.5	20.3	0.5	20.3	ns
t_{PLZ}			3.1	0.5	20.3	0.5	20.3	0.5	20.3	0.5	20.3	
t_{PHZ}	$\overline{OE}$	B	4.1	0.5	20.0	0.5	18.6	0.5	17.9	0.5	18.9	ns
t_{PLZ}			4.1	0.5	20.0	0.5	18.6	0.5	17.9	0.5	18.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.5	14.2	0.5	13.0	0.5	12.3	0.5	12.1	ns
t_{PHL}			2.5	0.5	14.2	0.5	13.0	0.5	12.3	0.5	12.1	
t_{PLH}	B	A	2.5	0.5	13.3	0.5	13.0	0.5	12.1	0.5	11.8	ns
t_{PHL}			2.5	0.5	13.3	0.5	13.0	0.5	12.1	0.5	11.8	
t_{PZH}	$\overline{OE}$	A	3	0.5	17.2	0.5	17.2	0.5	17.2	0.5	17.2	ns
t_{PZL}			3	0.5	17.2	0.5	17.2	0.5	17.2	0.5	17.2	
t_{PZH}	$\overline{OE}$	B	4.6	0.5	19.6	0.5	17.0	0.5	14.2	0.5	13.2	ns
t_{PZL}			4.6	0.5	19.6	0.5	17.0	0.5	14.2	0.5	13.2	
t_{PHZ}	$\overline{OE}$	A	2.8	0.5	17.7	0.5	17.7	0.5	17.7	0.5	17.7	ns
t_{PLZ}			2.8	0.5	17.7	0.5	17.7	0.5	17.7	0.5	17.7	
t_{PHZ}	$\overline{OE}$	B	3.9	0.5	18.9	0.5	17.3	0.5	15.8	0.5	15.4	ns
t_{PLZ}			3.9	0.5	18.9	0.5	17.3	0.5	15.8	0.5	15.4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.4	0.5	13.5	0.5	12.1	0.5	10.7	0.5	10.2	ns
t_{PHL}			2.4	0.5	13.5	0.5	12.1	0.5	10.7	0.5	10.2	
t_{PLH}	B	A	3	0.5	13.9	0.5	12.3	0.5	10.7	0.5	10.4	ns
t_{PHL}			3	0.5	13.9	0.5	12.3	0.5	10.7	0.5	10.4	
t_{PZH}	$\overline{OE}$	A	2.2	0.5	13.7	0.5	13.7	0.5	13.7	0.5	13.7	ns
t_{PZL}			2.2	0.5	13.7	0.5	13.7	0.5	13.7	0.5	13.7	
t_{PZH}	$\overline{OE}$	B	4.5	0.5	19.1	0.5	16.5	0.5	13.3	0.5	12.3	ns
t_{PZL}			4.5	0.5	19.1	0.5	16.5	0.5	13.3	0.5	12.3	
t_{PHZ}	$\overline{OE}$	A	1.8	0.5	14.2	0.5	14.2	0.5	14.2	0.5	14.2	ns
t_{PLZ}			1.8	0.5	14.2	0.5	14.2	0.5	14.2	0.5	14.2	
t_{PHZ}	$\overline{OE}$	B	3.6	0.5	17.7	0.5	16.3	0.5	14.2	0.5	12.1	ns
t_{PLZ}			3.6	0.5	17.7	0.5	16.3	0.5	14.2	0.5	12.1	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	0.5	13.2	0.5	11.1	0.5	10.4	0.5	9.7	ns
t_{PHL}			2.3	0.5	13.2	0.5	11.1	0.5	10.4	0.5	9.7	
t_{PLH}	B	A	3.5	0.5	17.2	0.5	12.1	0.5	10.2	0.5	9.7	ns
t_{PHL}			3.5	0.5	17.2	0.5	12.1	0.5	10.2	0.5	9.7	
t_{PZH}	$\overline{OE}$	A	2	0.5	12.3	0.5	12.3	0.5	12.3	0.5	12.3	ns
t_{PZL}			2	0.5	12.3	0.5	12.3	0.5	12.3	0.5	12.3	
t_{PZH}	$\overline{OE}$	B	4.5	0.5	18.9	0.5	16.1	0.5	13.2	0.5	12.1	ns
t_{PZL}			4.5	0.5	18.9	0.5	16.1	0.5	13.2	0.5	12.1	
t_{PHZ}	$\overline{OE}$	A	1.7	0.5	12.3	0.5	12.3	0.5	12.3	0.5	12.3	ns
t_{PLZ}			1.7	0.5	12.3	0.5	12.3	0.5	12.3	0.5	12.3	
t_{PHZ}	$\overline{OE}$	B	3.4	0.5	17.4	0.5	15.8	0.5	13.7	0.5	12.6	ns
t_{PLZ}			3.4	0.5	17.4	0.5	15.8	0.5	13.7	0.5	12.6	

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	1	1	1	1	1	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		12	12	12	13	14	
		Outputs disabled		1	1	1	1	1	
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	12	12	12	13	14	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	1	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver

Table 1. Typical Total Static Current Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	µA
1.2 V	<0.5	<1	<1	<1	<1	1	µA
1.5 V	<0.5	<1	<1	<1	<1	1	µA
1.8 V	<0.5	<1	<1	<1	<1	<1	µA
2.5 V	<0.5	1	<1	<1	<1	<1	µA
3.3 V	<0.5	1	<1	<1	<1	<1	µA

TYPICAL CHARACTERISTICS

Typical Propagation Delay (A to B) Versus Load Capacitance
T_A = 25°C, V_{CCA} = 1.2 V

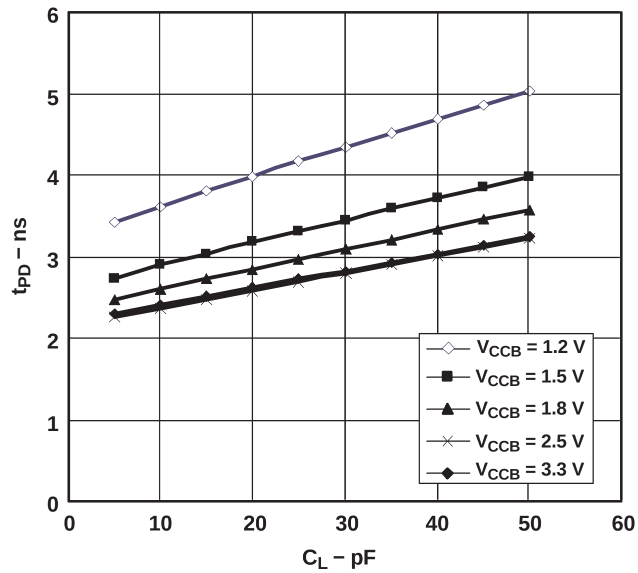


Figure 1.

Typical Propagation Delay (A to B) Versus Load Capacitance
T_A = 25°C, V_{CCA} = 1.5 V

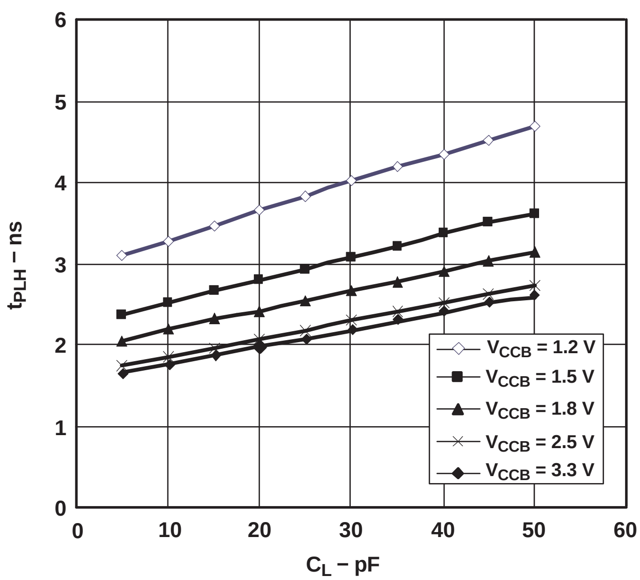


Figure 2.

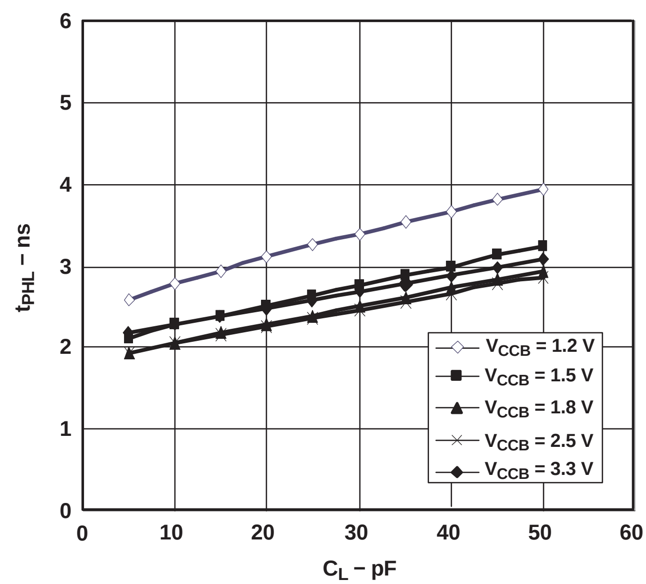


Figure 3.

TYPICAL CHARACTERISTICS (continued)

Typical Propagation Delay (A to B) Versus Load Capacitance
T_A = 25°C, V_{CCA} = 1.8 V

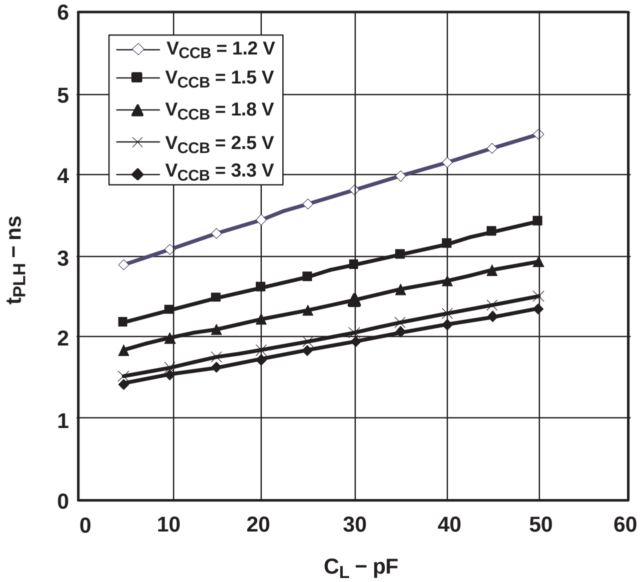


Figure 4.

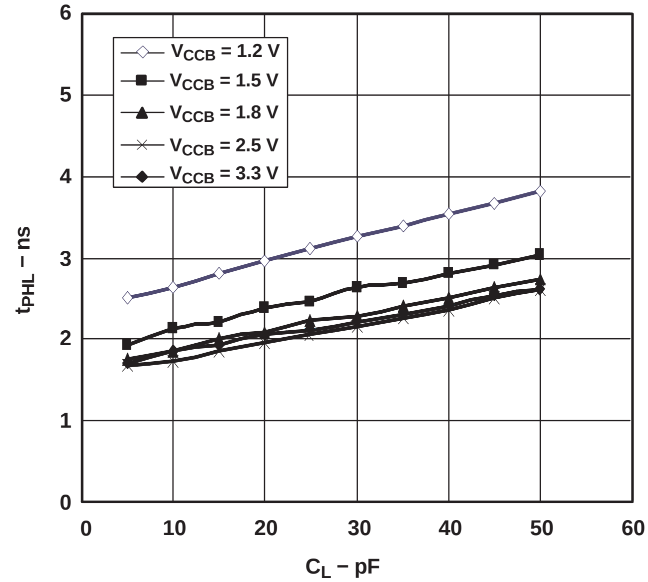


Figure 5.

Typical Propagation Delay (A to B) Versus Load Capacitance
T_A = 25°C, V_{CCA} = 2.5 V

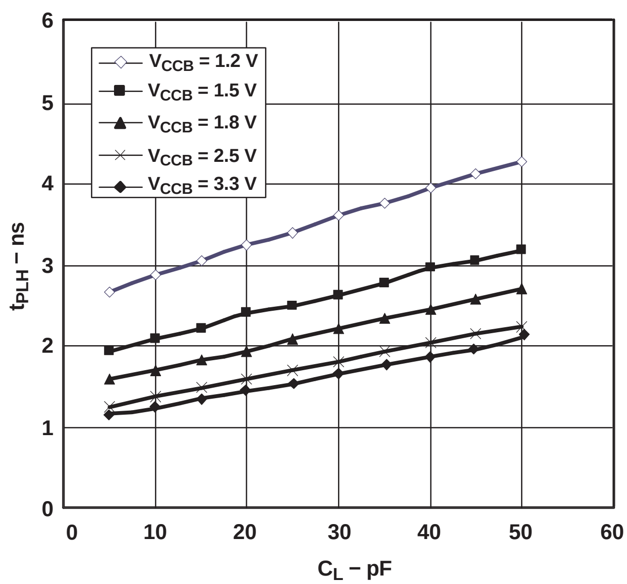


Figure 6.

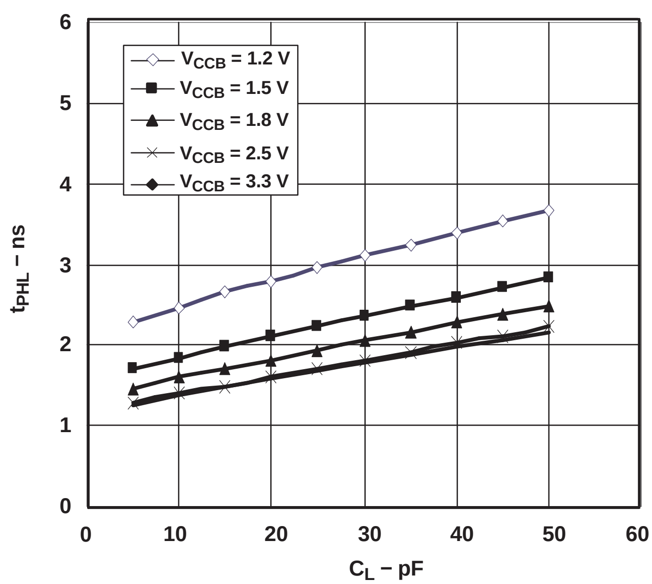


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Typical Propagation Delay (A to B) Versus Load Capacitance
T_A = 25°C, V_{CCA} = 3.3 V

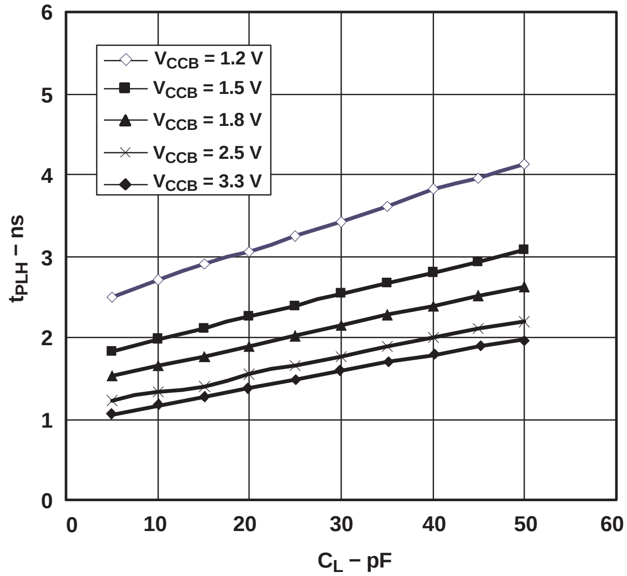


Figure 8.

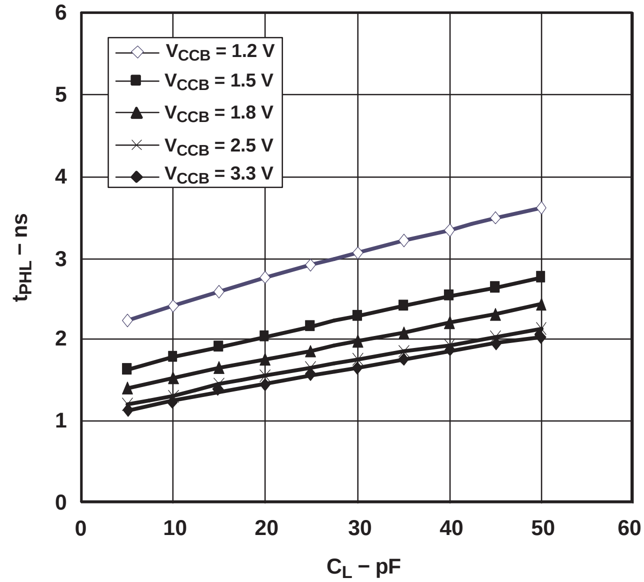
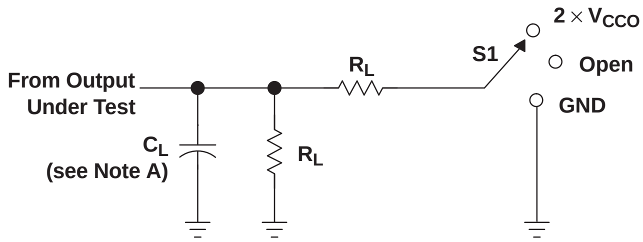


Figure 9.

PARAMETER MEASUREMENT INFORMATION

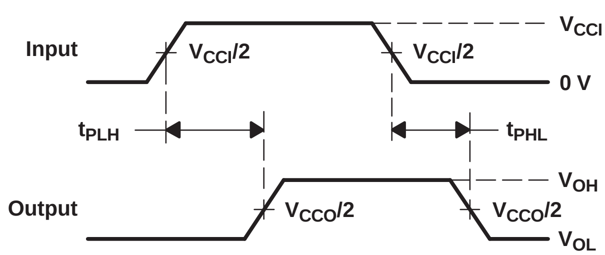


LOAD CIRCUIT

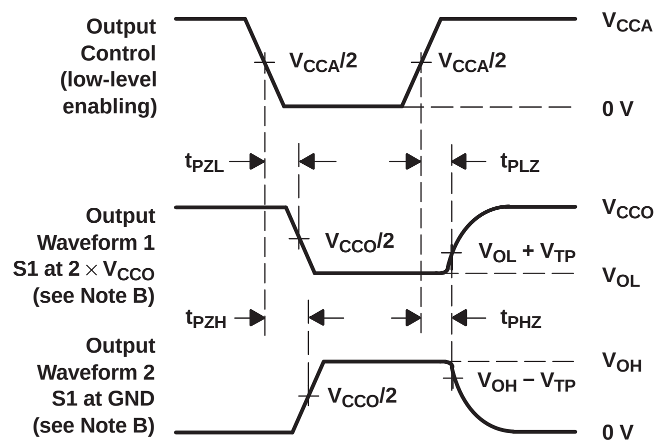
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

VOLTAGE WAVEFORMS
PULSE DURATION

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 10. Load Circuit and Voltage Waveforms

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CAVC8T245QRHLRQ1	ACTIVE	QFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WE245Q	Samples
SN74AVC8T245QPWRQ1	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	WE245Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74AVC8T245-Q1 :

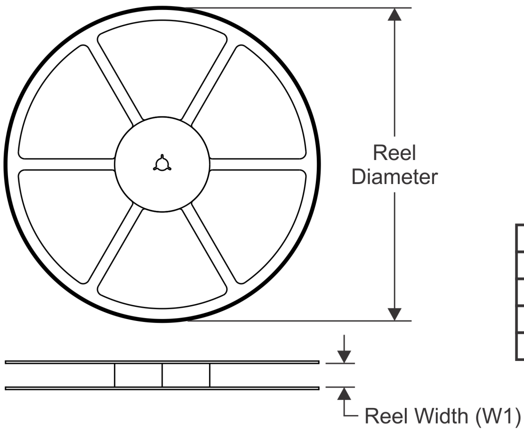
- Catalog: SN74AVC8T245

NOTE: Qualified Version Definitions:

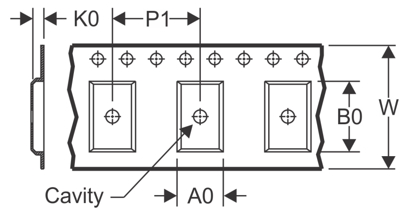
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

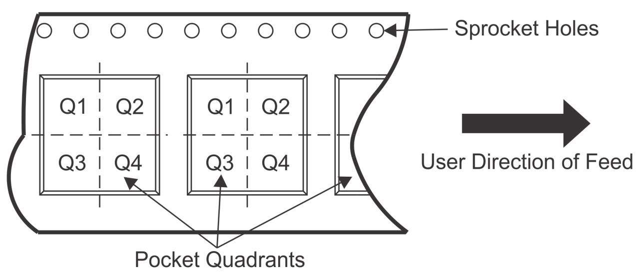


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

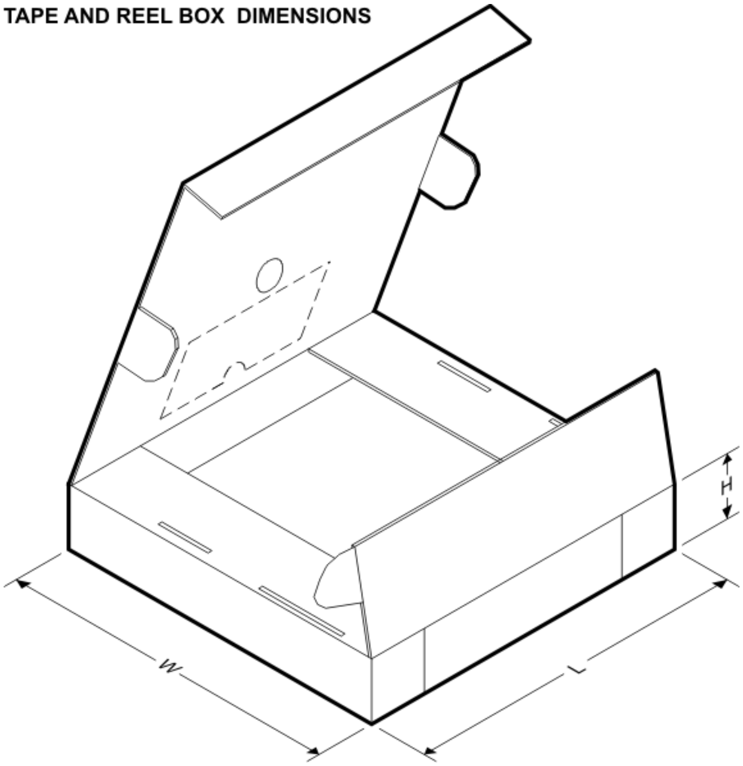
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVC8T245QRHLRQ1	QFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AVC8T245QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

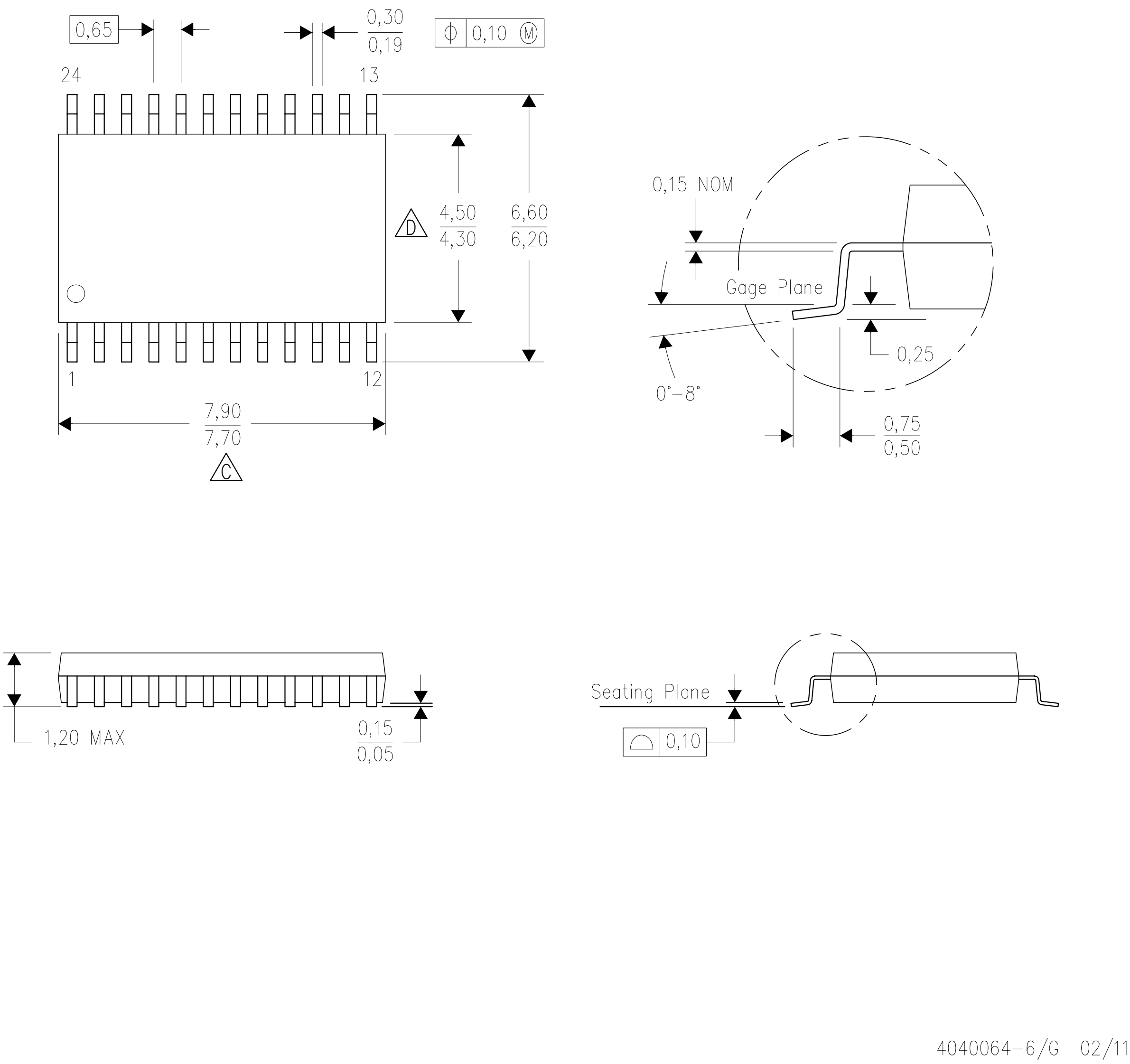
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

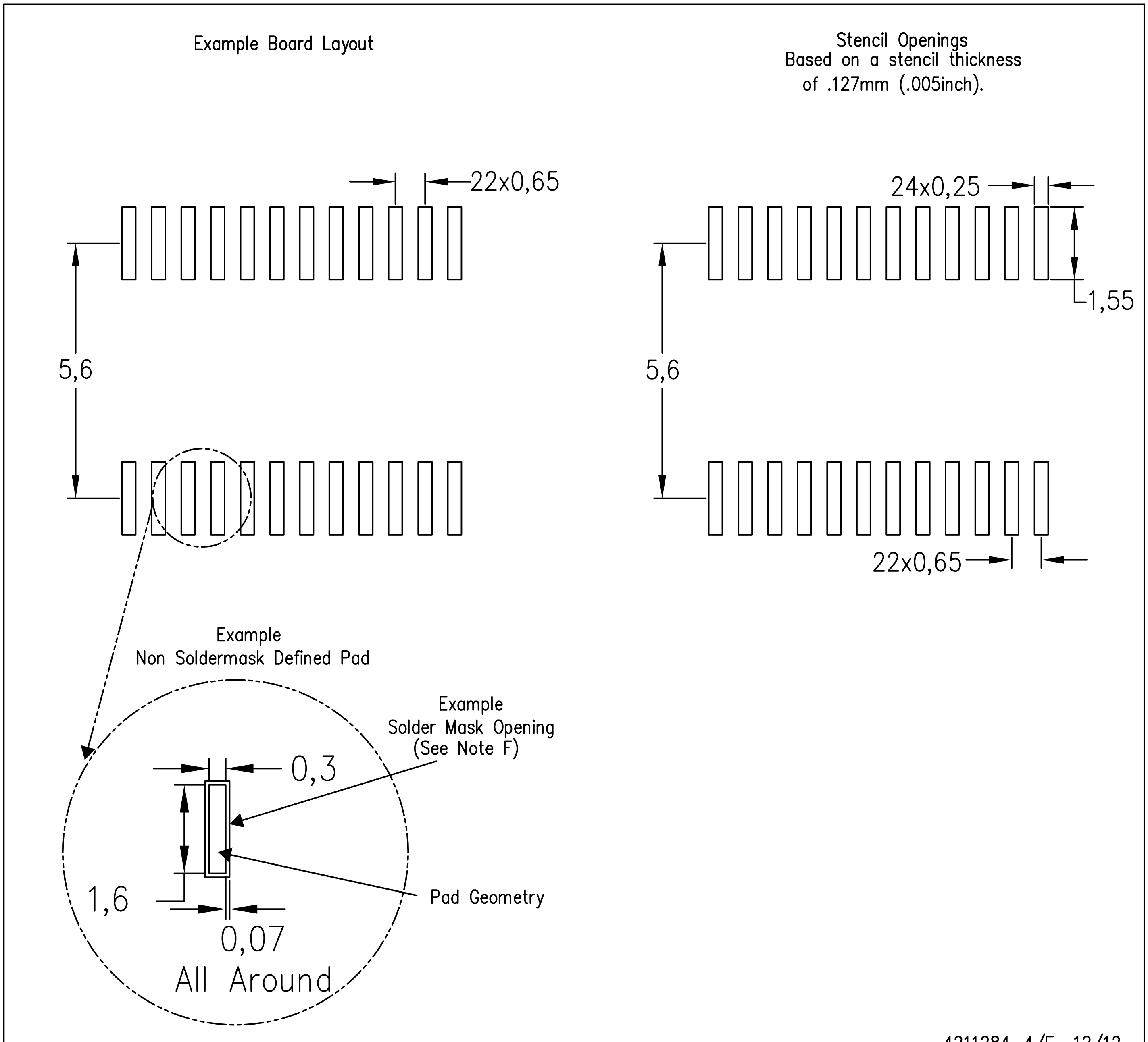
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVC8T245QRHLRQ1	QFN	RHL	24	1000	210.0	185.0	35.0
SN74AVC8T245QPWRQ1	TSSOP	PW	24	2000	367.0	367.0	38.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

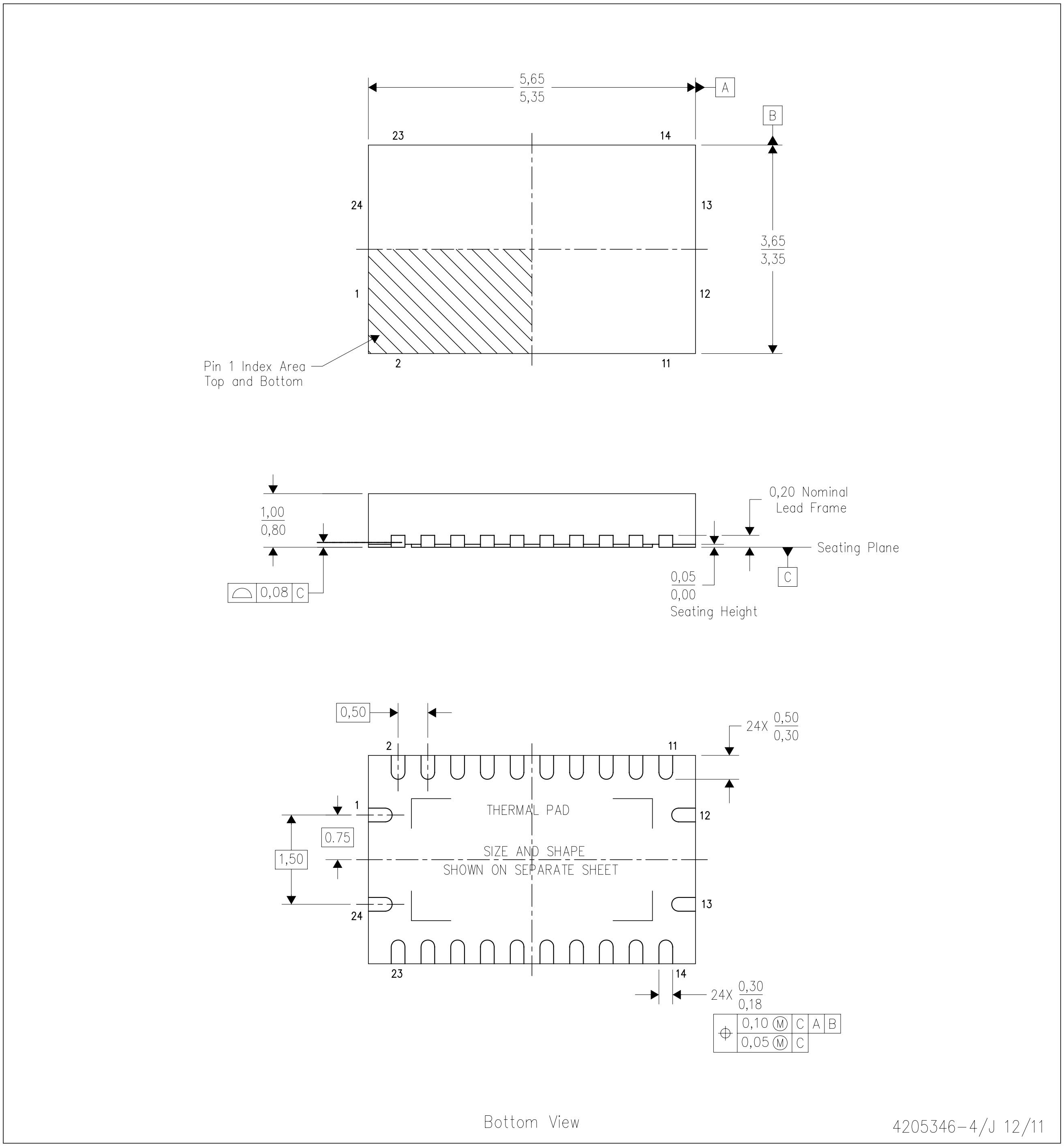
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4211284–4/F 12/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. JEDEC MO-241 package registration pending.

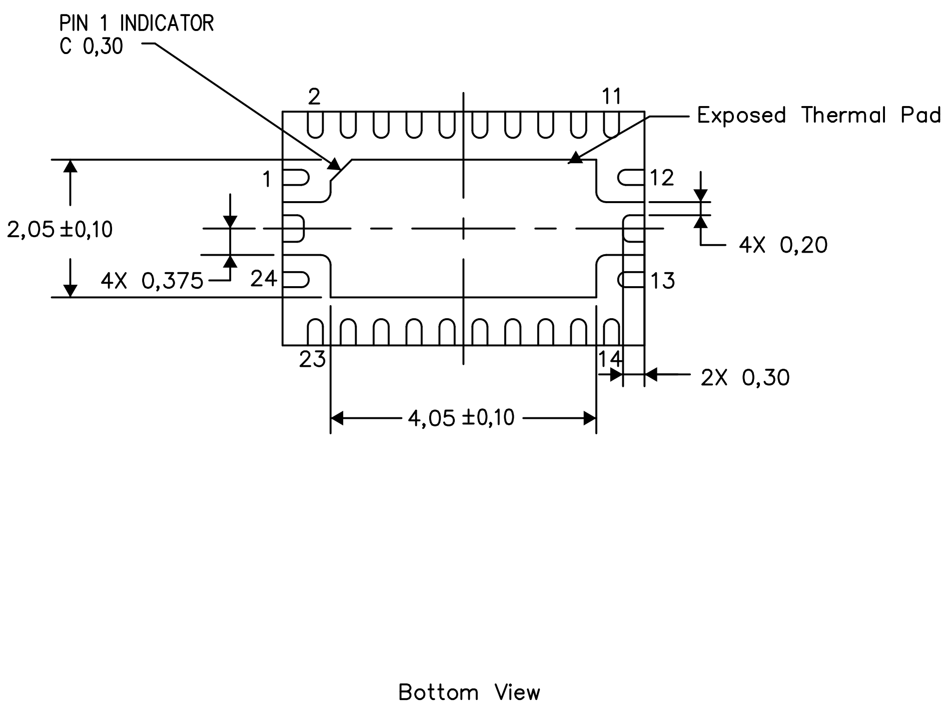
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

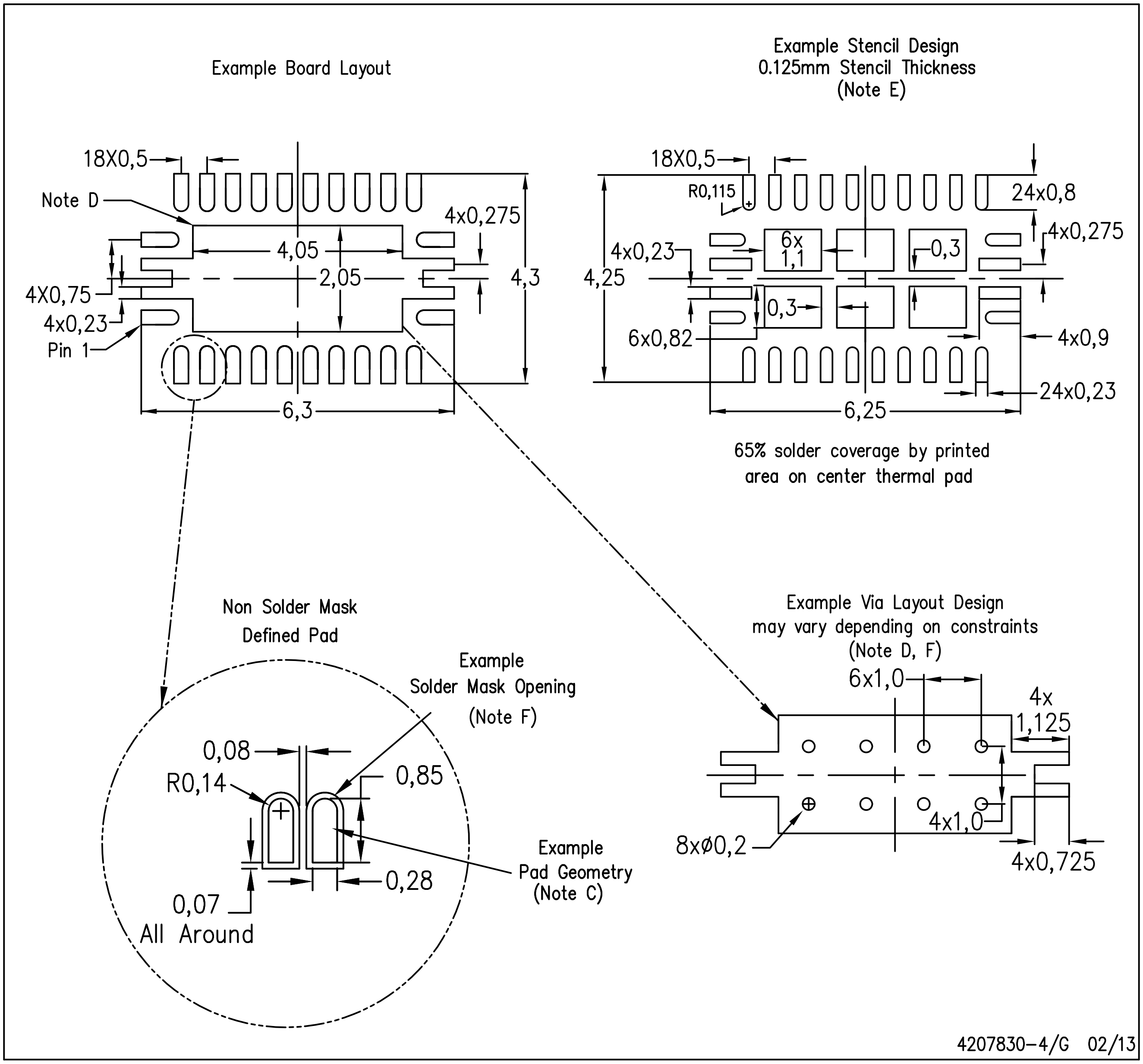


Exposed Thermal Pad Dimensions

4206363–4/M 08/12

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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