TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS098D – Revised October 2003

# CD40107B Types

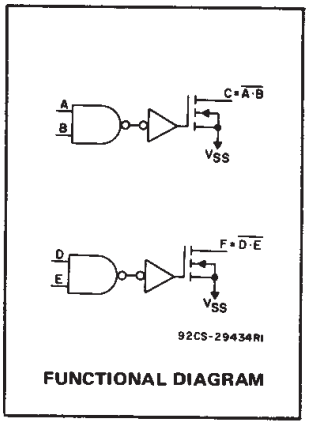
## CMOS Dual 2-Input NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

The CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at $V_{DD}$ = 10 V, $V_{DS}$ = 1 V). The CD40107B is supplied in 8-lead hermetic dual-in-line ceramic packages (F3A suffix), 8-lead dual-in-line plastic packages (E suffix), 8-lead small-outline packages (M, M96, MT, and PSR suffixes), and 8-lead thin shrink small-outline packages (PW and PWR suffixes).

*Features:*

- 32 times standard B-Series output current drive sinking capability — 136 mA typ. @ $V_{DD}$ = 10 V, $V_{DS}$ = 1 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range, $R_L$ to $V_{DD}$ = 10 kΩ:
  1 V at $V_{DD}$ = 5 V
  2 V at $V_{DD}$ = 10 V
  2.5 V at $V_{DD}$ = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"




FUNCTIONAL DIAGRAM

*Applications*

- Driving relays, lamps, LEDs
- Line driver
- Level shifter (up or down)

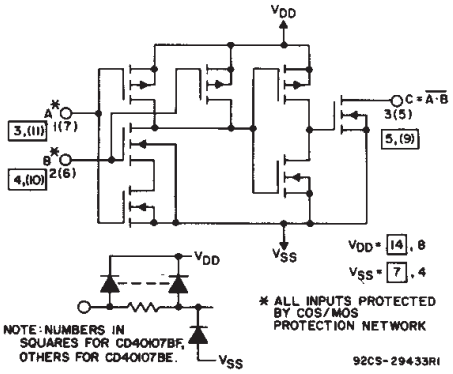



*Fig.1 — Schematic diagram of CD40107B (one of 2 gates)*

TRUTH TABLE

| A | B | C | |
|---|---|---|---|
| 0 | 0 | 1* | Z# |
| 1 | 0 | 1* | Z# |
| 0 | 1 | 1* | Z# |
| 1 | 1 | 0 | |

*Requires external pull-up resistor ($R_L$) to $V_{DD}$.

#Without pull-up resistor (3-state).

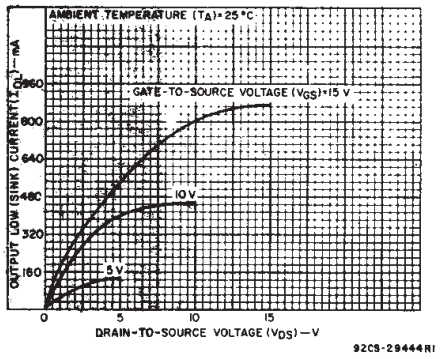



*Fig.2 — Typical output low (sink) current characteristics.*

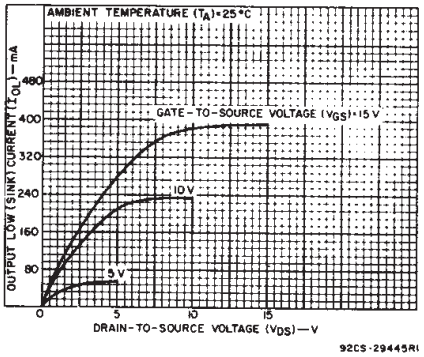



*Fig.3 — Minimum output low (sink) current characteristics.*

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
  Voltages referenced to $V_{SS}$ Terminal) ..... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
  For $T_A$ = −55°C to +100°C ..... 500mW
  For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) .....−55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) .....−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

**RECOMMENDED OPERATING CONDITIONS**

*For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$= Full Package-Temperature Range) | 3 | 18 | V |

## DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns

| CHARACTERISTIC | TEST CONDITIONS | $V_{DD}$ Volts | LIMITS Typ. | LIMITS Max. | UNITS |
|---|---|---|---|---|---|
| Propagation Delay: High-to-Low, $t_{PHL}$ | $R_L$* = 120 Ω | 5 | 100 | 200 | ns |
| | | 10 | 45 | 90 | |
| | | 15 | 30 | 60 | |
| Low-to-High, $t_{PLH}$ | $R_L$* = 120 Ω | 5 | 100 | 200 | ns |
| | | 10 | 60 | 120 | |
| | | 15 | 50 | 100 | |
| Transition Time: High-to-Low, $t_{THL}$ | $R_L$* = 120 Ω | 5 | 50 | 100 | ns |
| | | 10 | 20 | 40 | |
| | | 15 | 10 | 20 | |
| Low-to-High, $t_{TLH}$ | $R_L$* = 120 Ω | 5 | 50 | 100 | ns |
| | | 10 | 35 | 70 | |
| | | 15 | 25 | 50 | |
| Average Input Capacitance, $C_{IN}$ | Any Input | | 5 | 7.5 | pF |
| Average Output Capacitance, $C_{OUT}$ | Any Output | | 30 | – | pF |

* $R_L$ is external pull-up resistor to $V_{DD}$.

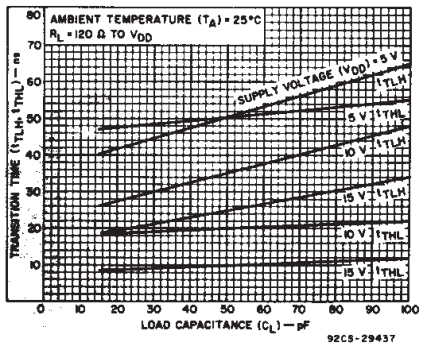



*Fig.4 – Typical transition time as a function of load capacitance.*

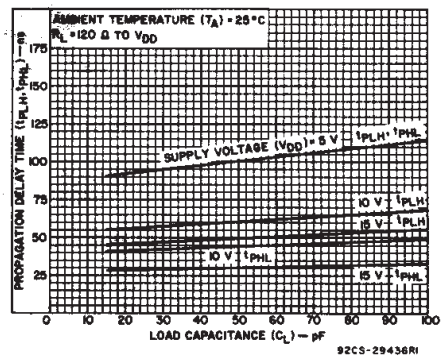



*Fig.5 – Typical propagation delay time as a function of load capacitance.*

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | –55 | –40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Quiescent Device Current $I_{DD}$ Max. | – | 0,5 | 5 | 1 | 1 | 30 | 30 | – | 0.02 | 1 | μA |
| | – | 0,10 | 10 | 2 | 2 | 60 | 60 | – | 0.02 | 2 | |
| | – | 0,15 | 15 | 4 | 4 | 120 | 120 | – | 0.02 | 4 | |
| | – | 0,20 | 20 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 21 | 20 | 14 | 12 | 16 | 32 | – | mA |
| | 1 | 0,5 | 5 | 44 | 42 | 30 | 25 | 34 | 68 | – | |
| | 0.5 | 0,10 | 10 | 49 | 46 | 32 | 28 | 37 | 74 | – | |
| | 1 | 0,10 | 10 | 89 | 85 | 60 | 51 | 68 | 136 | – | |
| | 0.5 | 0,15 | 15 | 66 | 63 | 44 | 38 | 50 | 100 | – | |
| Output High (Source) Current $I_{OH}$ Min. | No Internal Pull-Up Device | | | | | | | | | | |
| Input Low Voltage $V_{IL}$ Max.* | 4.5 | – | 5 | | 1.5 | | | – | – | 1.5 | V |
| | 9 | – | 10 | | 3 | | | – | – | 3 | |
| | 13.5 | – | 15 | | 4 | | | – | – | 4 | |
| Input High Voltage $V_{IH}$ Min.* | 0.5,4.5 | – | 5 | | 3.5 | | | 3.5 | – | – | |
| | 1,9 | – | 10 | | 7 | | | 7 | – | – | |
| | 1.5,13.5 | – | 15 | | 11 | | | 11 | – | – | |
| Input Current $I_{IN}$ Max. | – | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $±10^{-5}$ | ±0.1 | μA |
| Output Leakage Current $I_{OZ}$ Max. | 18 | 0,18 | 18 | 2 | 2 | 20 | 20 | – | $10^{-4}$ | 2 | μA |

* Measured with external pull-up resistor, $R_L$ = 10 kΩ to $V_{DD}$.

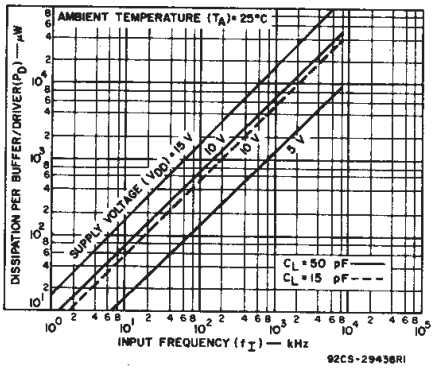



*Fig.6 – Typical power dissipation as a function of input frequency.*

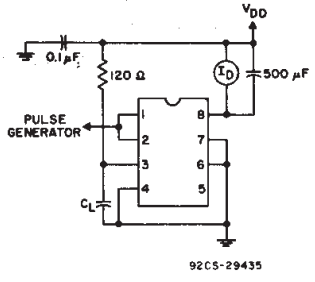
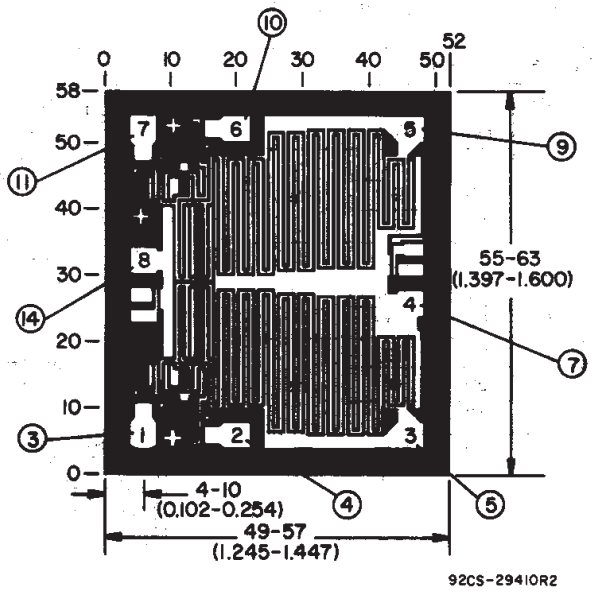



*Fig. 7 – Power-dissipation test circuit for CD40107BE.*




NOTE: NOS. IN PADS FOR CD40107BE
NOS. OUTSIDE CHIP FOR CD40107BF

*Dimensions and Pad Layout for CD40107BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

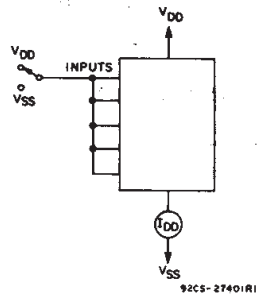



*Fig.8 – Quiescent-device current test circuit.*

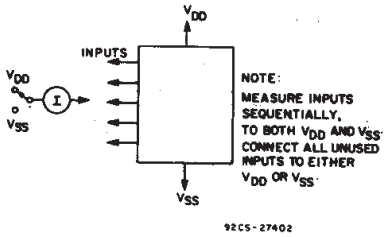



*Fig. 9 – Input-current test circuit.*

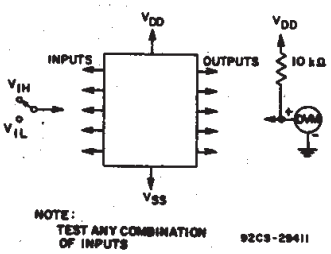
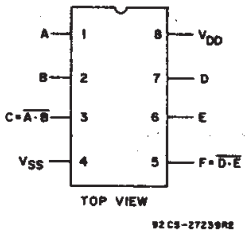
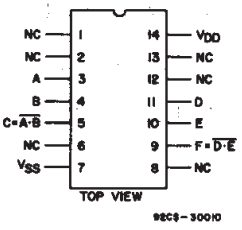



*Fig.10 – Input-voltage test circuit.*




CD40107BE




CD40107BF

**TERMINAL ASSIGNMENTS**

**Special Considerations for CD40107B**

1. **Limiting Capacitive Currents for CL > 500 pF, $V_{DD}$ > 15 V.**
   For $V_{DD}$ > 15 V, and load capacitance ($C_L$) from output to ground > 500 pF, an external 25 Ω series limiting resistor should be inserted between the output terminal and $C_L$. No external resistor is necessary if $C_L$ < 500 pF or $V_{DD}$ < 15 V.
2. **Driving Inductive Loads**
   When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD40107BE | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD40107BE | Samples |
| CD40107BEE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD40107BE | Samples |
| CD40107BF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD40107BF | Samples |
| CD40107BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD40107BF3A | Samples |
| CD40107BM | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BM96 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BM96E4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BM96G4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BME4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BMG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BMT | ACTIVE | SOIC | D | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BMTE4 | ACTIVE | SOIC | D | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BMTG4 | ACTIVE | SOIC | D | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107 | Samples |
| CD40107BPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD40107BPWE4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPWRE4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |
| CD40107BPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM0107B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD40107B, CD40107B-MIL :**

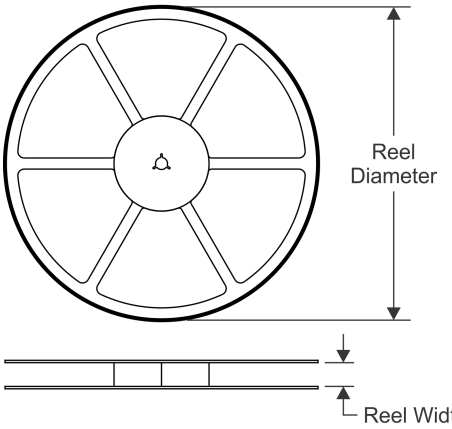
- Catalog: CD40107B
- Military: CD40107B-MIL

NOTE: Qualified Version Definitions:

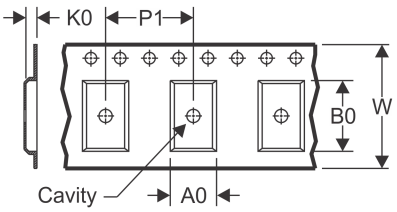
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

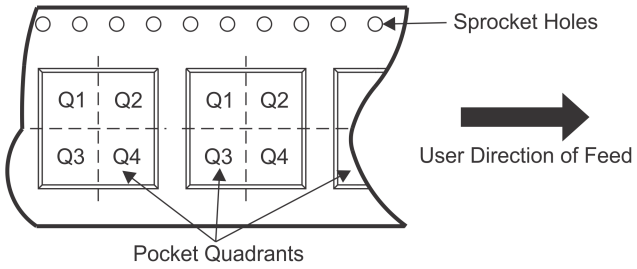



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

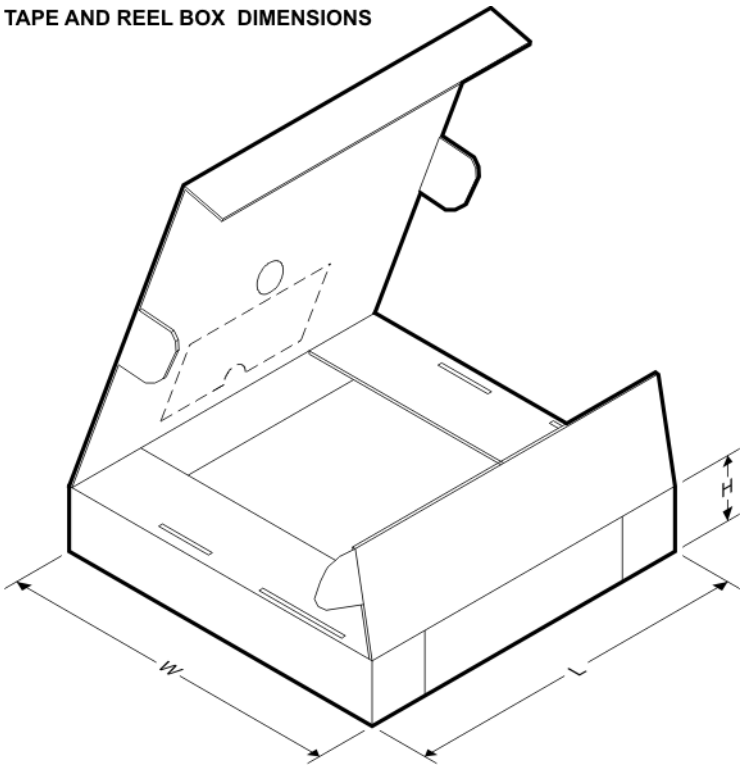
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD40107BM96 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| CD40107BM96 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| CD40107BMT | SOIC | D | 8 | 250 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| CD40107BPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| CD40107BPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



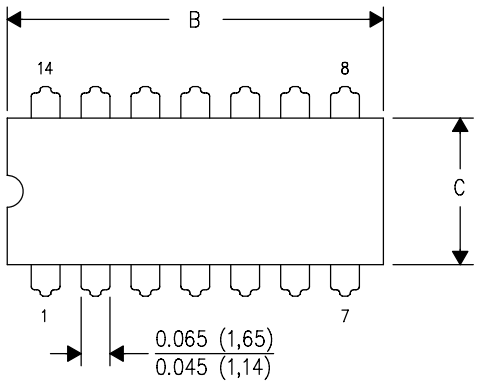

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD40107BM96 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| CD40107BM96 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| CD40107BMT | SOIC | D | 8 | 250 | 340.5 | 338.1 | 20.6 |
| CD40107BPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |
| CD40107BPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |

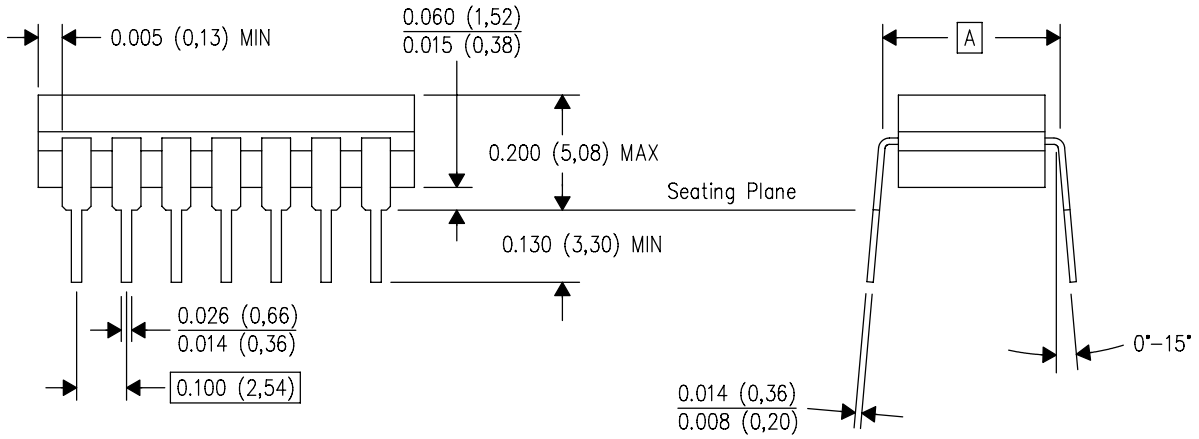
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



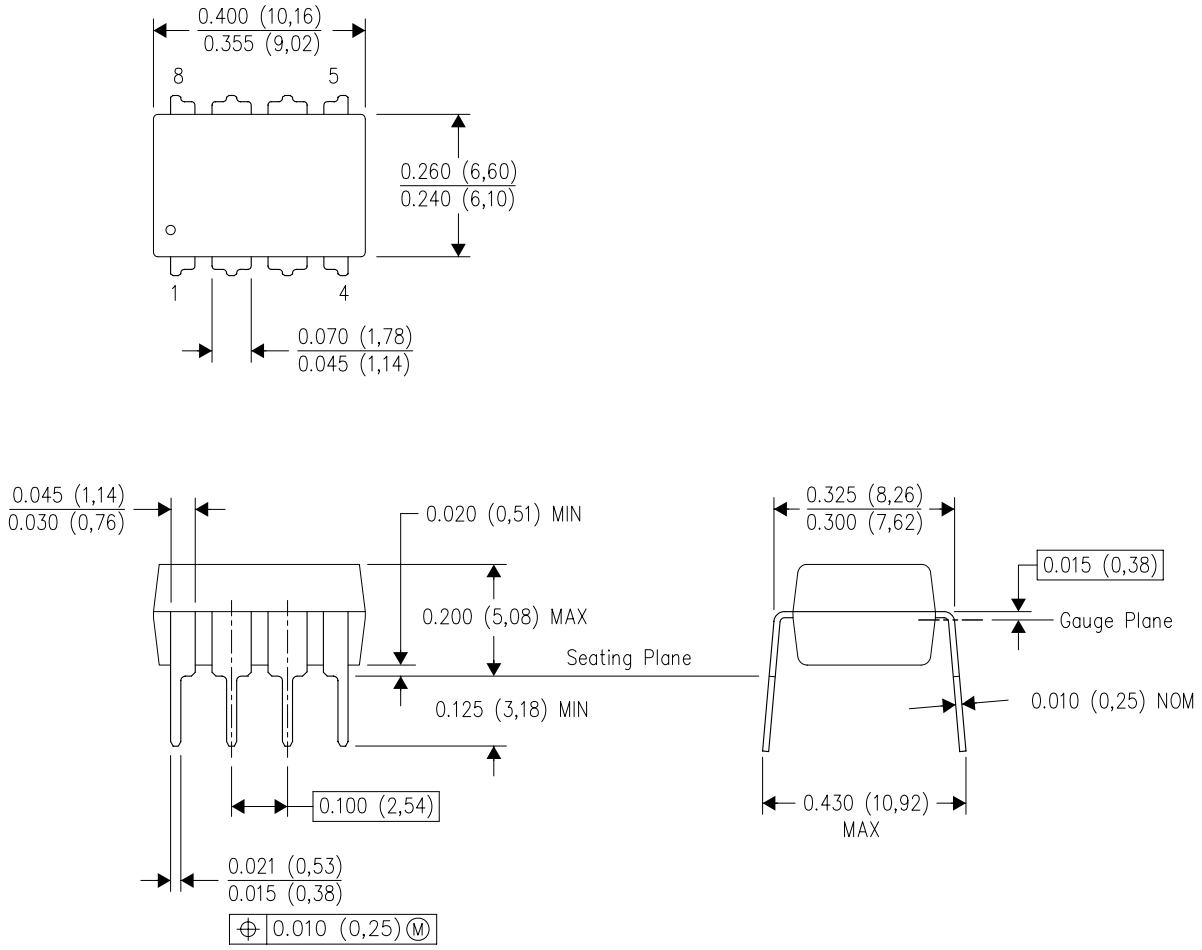

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

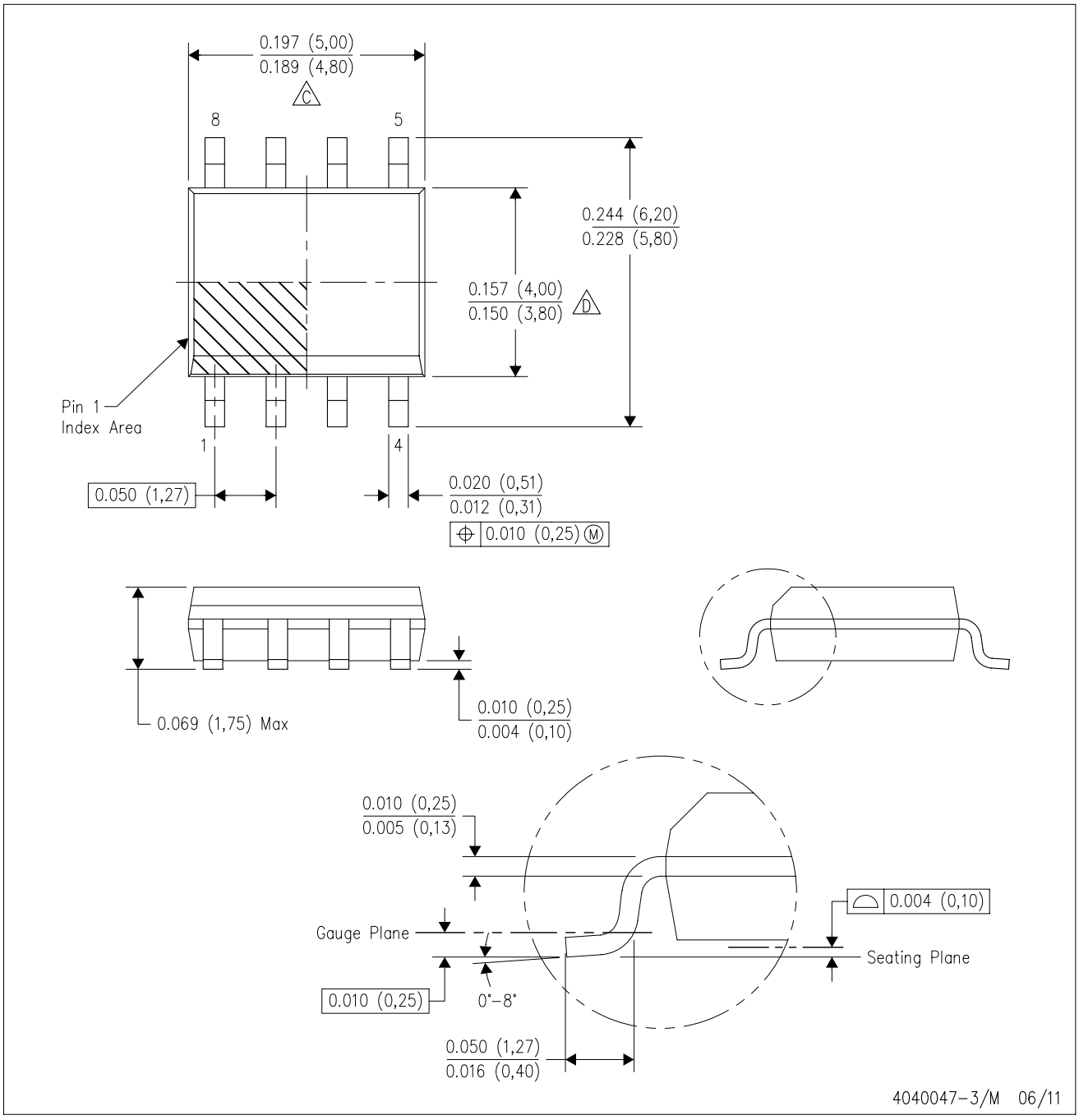
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



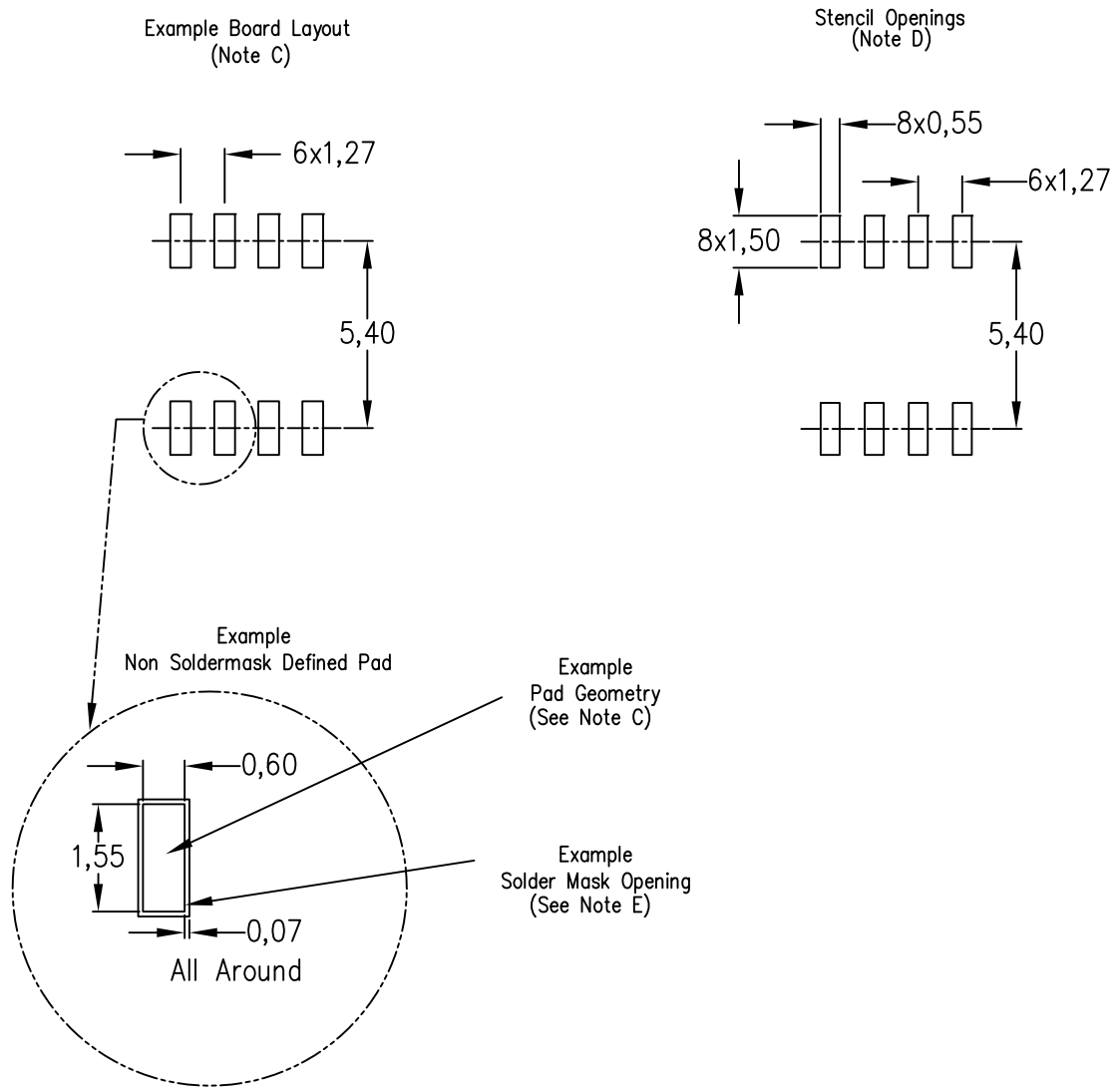

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

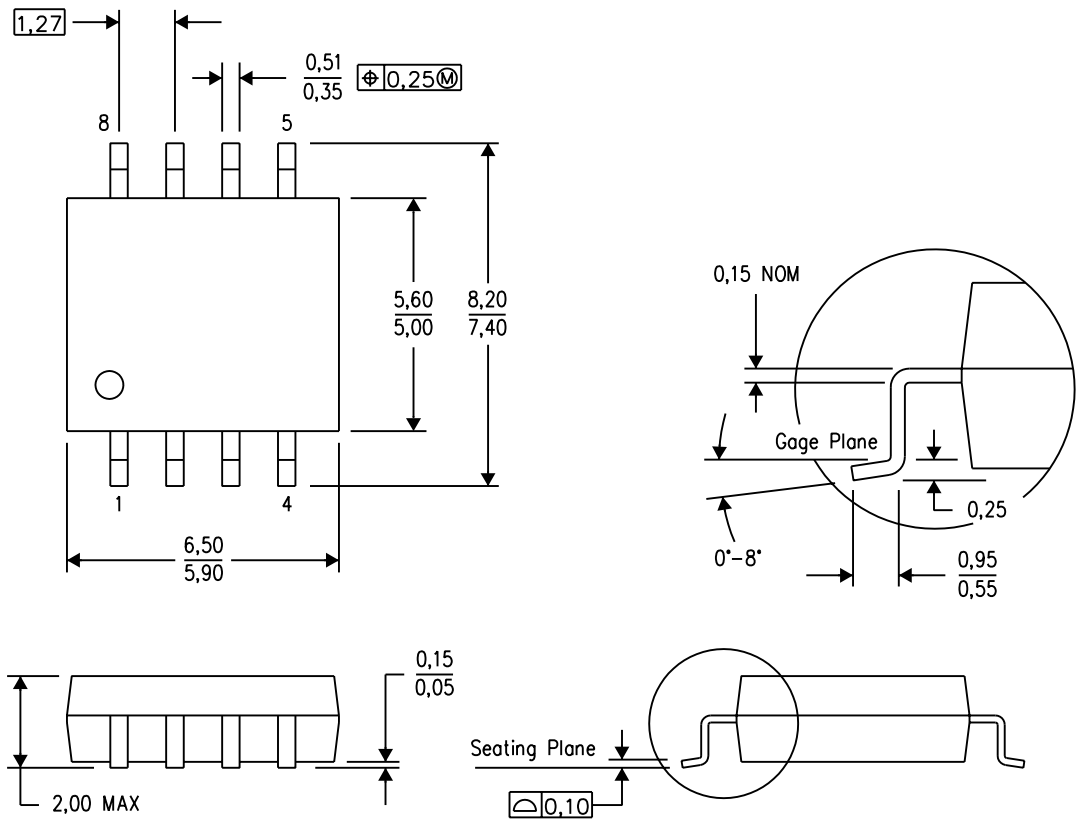
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

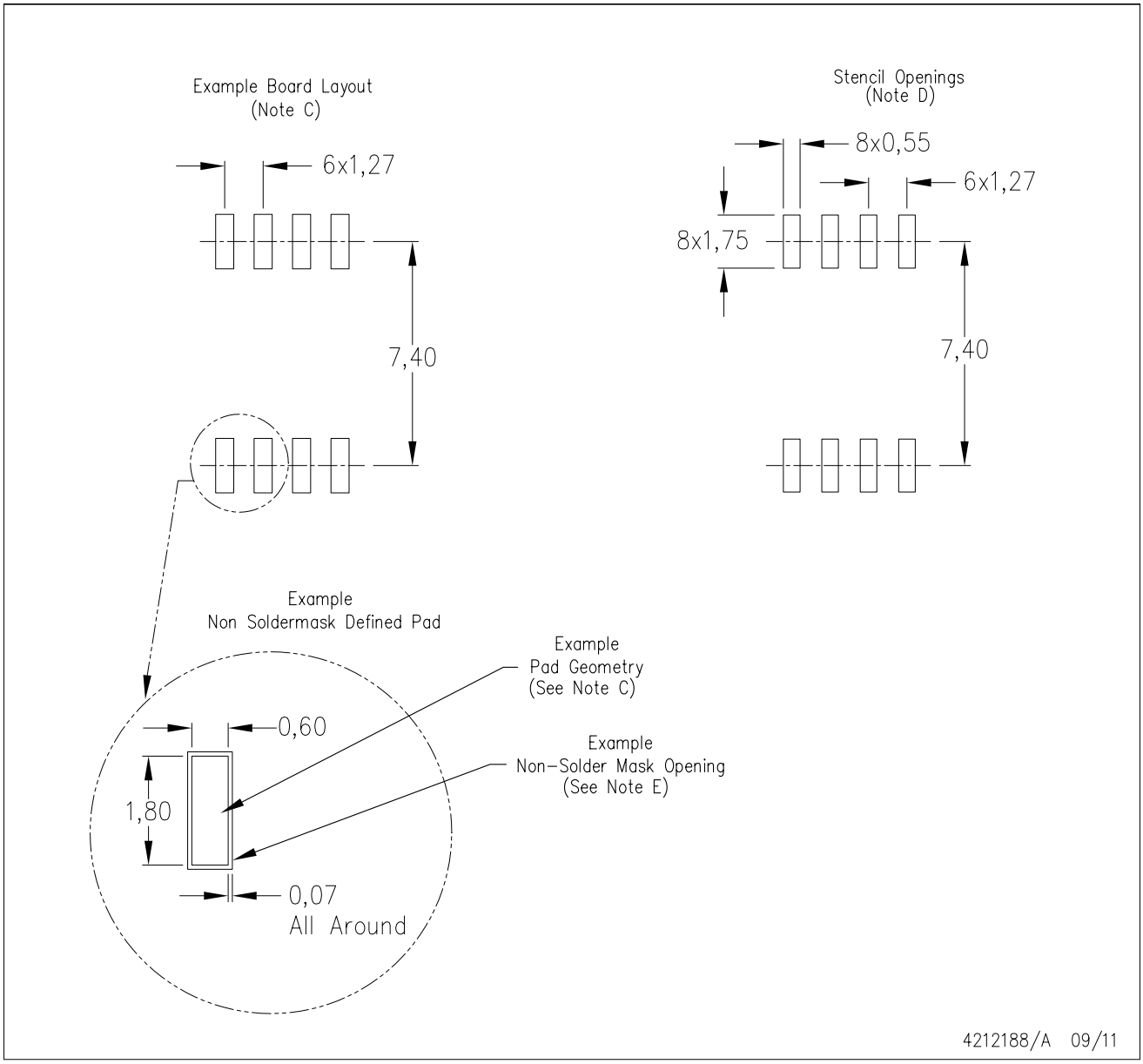
**PS (R-PDSO-G8)** **PLASTIC SMALL-OUTLINE PACKAGE**




4040063/C 03/03

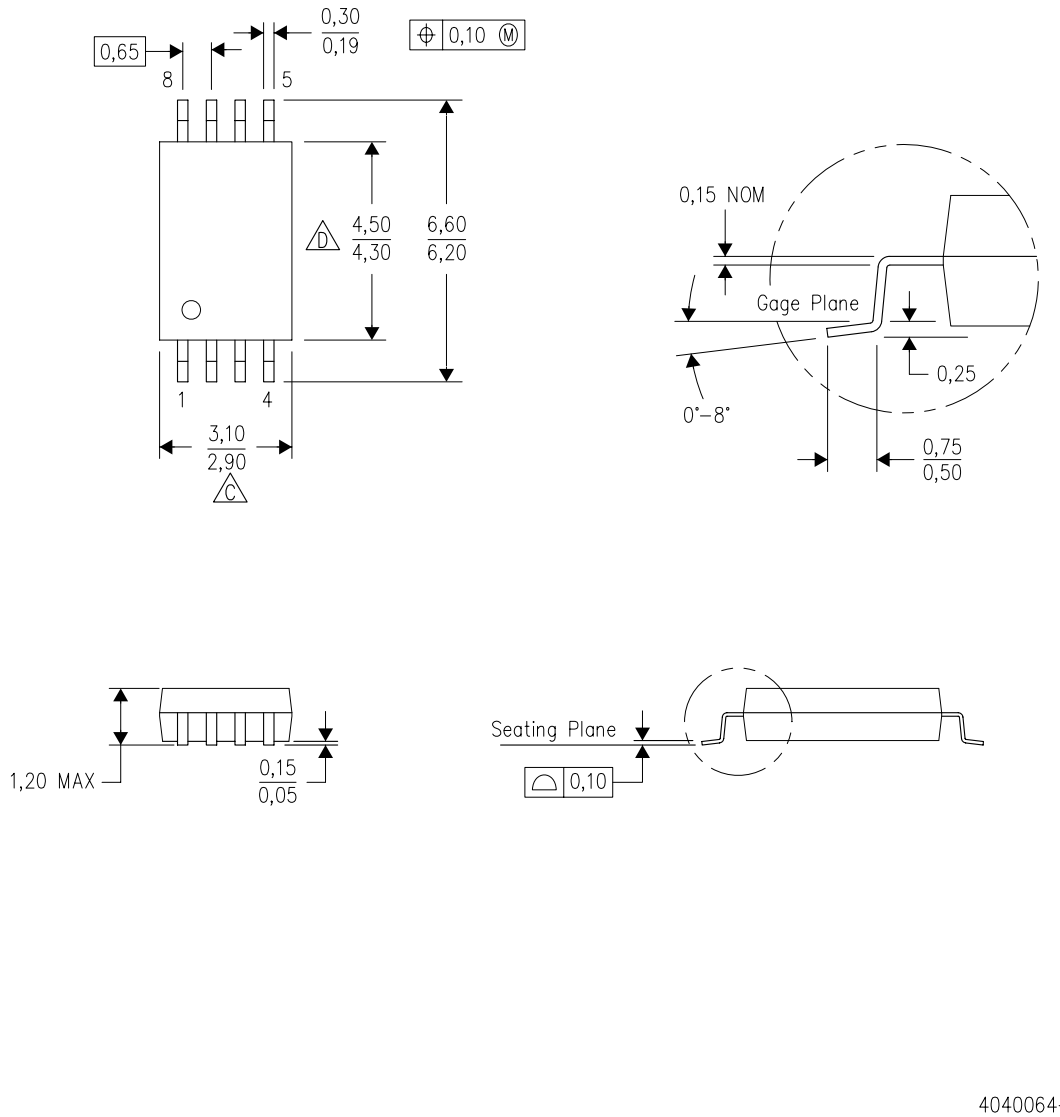
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE




4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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