

NOT RECOMMENDED FOR NEW DESIGNS

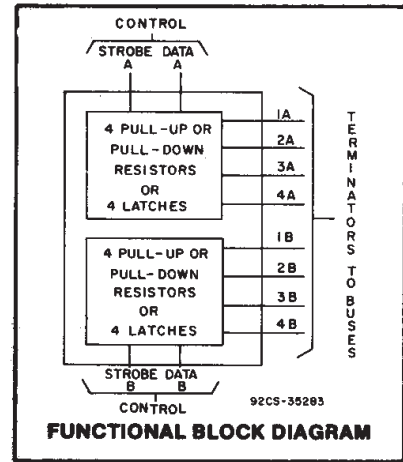
# CD40117B Types

## Programmable Dual 4-Bit Terminator

High-Voltage Types (20-Volt Rating)

**Features:**

- One standard "B" output will drive eight terminator circuits.
- Will terminate a CMOS data bus with up to 40 B-series inputs or 3-state outputs connected at VDD of 5 V.
- Input terminals protected by standard "B" series ESD protection network.
- Preserves final logic state.
- Output after switching is closer to VDD or VSS rail than with a resistor.
- Requires only one solder connection.
- Open circuited terminator not used will not affect performance.
- Can be connected to any CMOS I/O line.
- Draws current only when logic state is changing.
- Can be preset.



■ CD40117B is a dual 4-bit terminator that can be programmed by means of STROBE and DATA control bits to function as pull-up or pull-down resistors. The CD40117B can also be programmed to function as latches to terminate any open or unused CMOS logic when used with 3-state logic or during a power-down condition. Considerable savings in power and board space can be realized when this device is used to replace pull-up or pull-down resistors. When the STROBE is in the logic "1" state, the terminator functions as a pull-up resistor if the DATA input is a logic "1" or as a pull-down resistor if the DATA input is a logic "0".

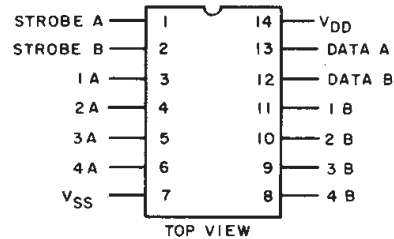
When the STROBE is in the logic "0" state, the terminator performs the latch function, i.e., it follows the changing states of the bus. If the bus goes into the high-Z state or into a power-down condition, the latched terminator retains the data ("1" or "0") that the bus carried before it switched to the high-Z or power-down state. If and when the bus changes from the high-Z state to the state opposite to that which the latch is storing, the bus will override the latch and the terminator will reflect the state on the bus. The small geometries chosen for the inverters in the latch allow this override mode. When checking the data bus whose last state is being preserved by the terminator, a resistor should be used in series with the probe whose input capacitance could trip the small latches. The resistance should be in excess of the output impedance of the latch, i.e., R should be > 30 KΩ at VDD = 10 V.

The STROBE and DATA inputs in each section can be paralleled allowing this device to be used as an 8-bit bus terminator.

The CD40117B types are supplied in 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

**Applications:**

- Error state identification.
- Replaces pull-up or pull-down resistors
- Avoids floating inputs in modular systems
- Sharpens transistors (hysteresis)
- Anti-bounce circuit



**TERMINAL DIAGRAM**

**TRUTH TABLE**

STROBE	DATA	1A(B)	2A(B)	3A(B)	4A(B)
1	0	0 $\Delta$	0 $\Delta$	0 $\Delta$	0 $\Delta$
1	1	1 $+$	1 $+$	1 $+$	1 $+$
0	X	*	*	*	*

1 = High, 0 = Low, X = Don't Care

$\Delta$  Equivalent to pull-down resistor.

$+$  Equivalent to pull-up resistor.

\*Equivalent to a latch.

# CD40117B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ ) Voltages referenced to $V_{SS}$ Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10mA$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ C$ to $+100^\circ C$	500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79mm$ ) from case for 10s max	$+265^\circ C$

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For $T_A$ =Full Package-Temperature Range)	—	3	18	V

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

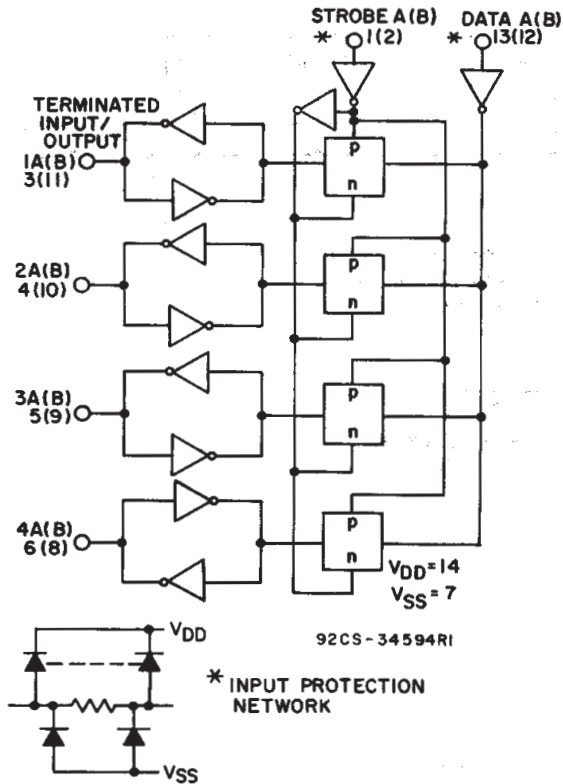
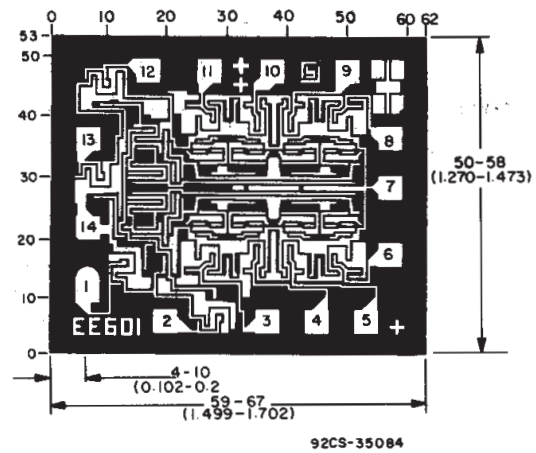


Fig. 1 - Logic diagram (1/2 of CD40117B)

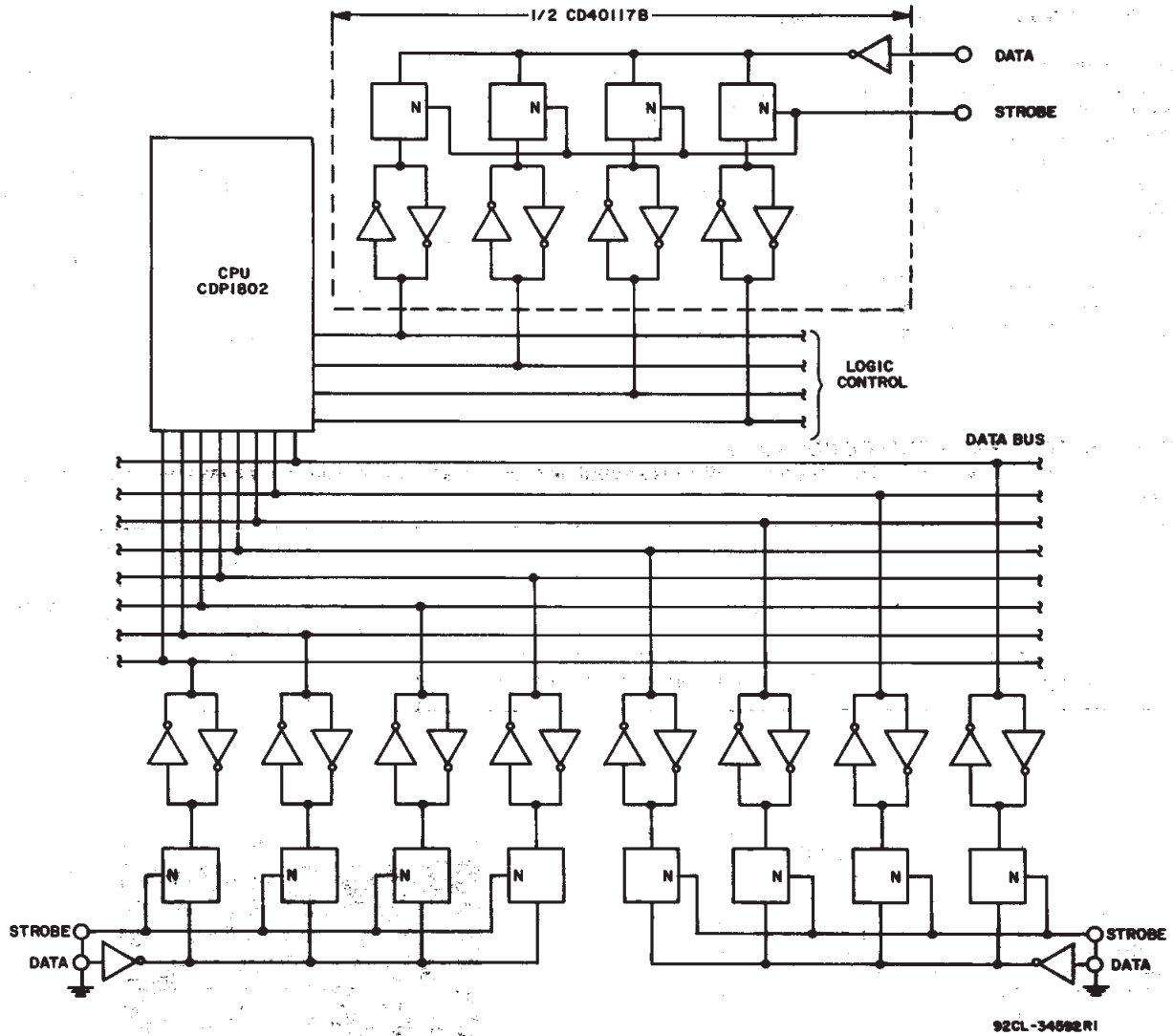


Dimensions and pad layout for CD40117B.

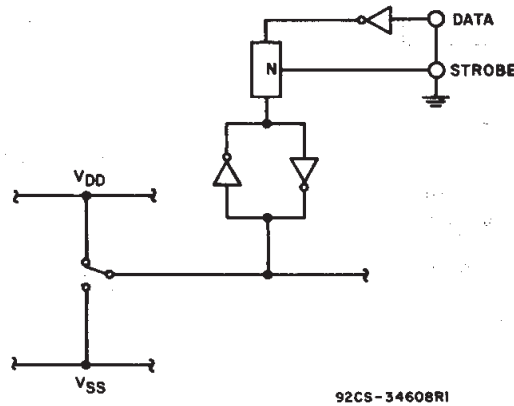
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## CD40117B Types

### TYPICAL APPLICATIONS



**Fig. 2 - Schematic of CD40117B interfacing with microprocessor terminating an 8-bit bus line and 1/2 of CD40117B as a programmable pull-up/pull down logic controller.**



**Fig. 3 - Schematic of CD40117B in anti-bounce circuit application.**

## CD40117B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current Max. I <sub>DD</sub>	—	0, 5	5	0.25	0.25	7.5	7.5	—	—	0.25	μA
	—	0, 10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0, 15	15	1	1	30	30	—	0.01	1	
	—	0, 20	20	5	5	150	150	—	0.02	5	
Output Low Sink Current Min. I <sub>OL</sub>	0.4	0, 5	5	—	—	—	—	—	25	—	μA
	0.5	0, 10	10	—	—	—	—	—	60	—	
	1.5	0, 15	15	—	—	—	—	—	250	—	
Output High (Source) Current Min. I <sub>OH</sub>	4.6	0, 5	5	—	—	—	—	—	-25	—	μA
	2.5	0, 5	5	—	—	—	—	—	—	—	
	9.5	0, 10	10	—	—	—	—	—	-60	—	
	13.5	0, 15	15	—	—	—	—	—	-250	—	
Output Voltage: Low-Level Max. V <sub>OL</sub>	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min. V <sub>OH</sub>	—	0, 5	5	4.95				4.95	5	—	V
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max. V <sub>IL</sub>	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage Min. V <sub>IH</sub>	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current Max. I <sub>IN</sub>	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

### DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub>=25°C; Input t<sub>r</sub>, t<sub>f</sub>=20 ns, C<sub>L</sub>=50 pF, R<sub>L</sub>=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V <sub>DD</sub> (V)	LIMITS All Packages			UNITS
			MIN.	TYP.	MAX.	
Propagation Delay Time Strobe, Data to Outputs	t <sub>PHL</sub>	5	—	1.7	—	μs
		10	—	850	—	ns
		15	—	575	—	ns
	t <sub>PLH</sub>	5	—	1.5	—	μs
		10	—	625	—	ns
		15	—	500	—	ns
Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	5	—	3.3	—	μs
		10	—	1.6	—	μs
		15	—	1.1	—	μs
Minimum Strobe Pulse Width	t <sub>w</sub>	5	—	1.5	—	μs
		10	—	600	—	ns
		15	—	475	—	ns
Minimum Data Pulse Width	t <sub>WH</sub> , t <sub>WL</sub>	5	—	1.6	—	μs
		10	—	700	—	ns
		15	—	500	—	ns
Minimum Terminator Input/Output Pulse Width	t <sub>w</sub>	5	—	10	—	ns
Minimum Data Setup Time Data to Strobe	t <sub>SU</sub>	5	—	0	—	ns
		10	—	0	—	ns
		15	—	0	—	ns
Input Capacitance	C <sub>IN</sub>	Any Input	—	5	—	pF

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD40117BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
CD40117BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
CD40117BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD40117BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD40117BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

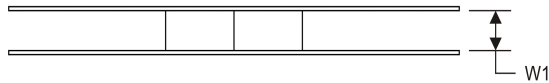
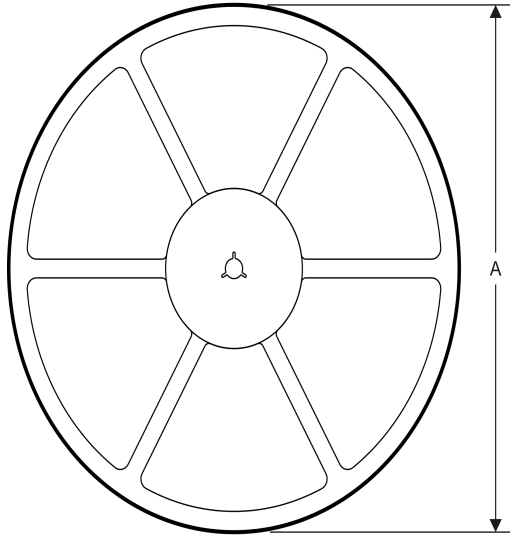
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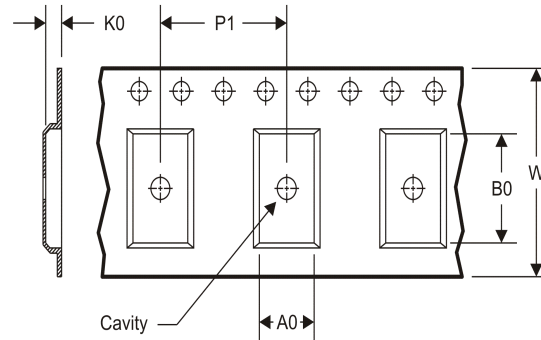


**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



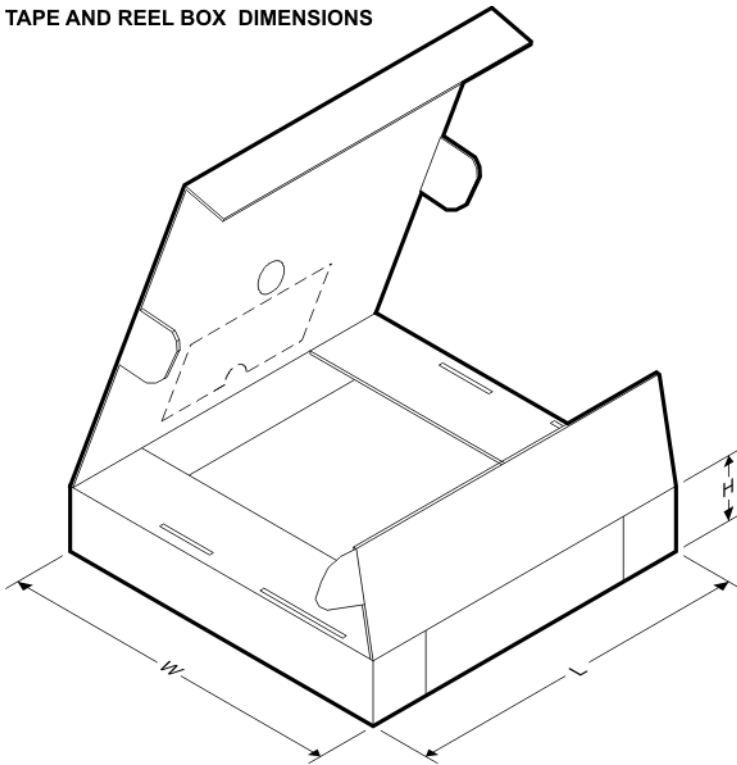
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40117BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40117BMT	SOIC	D	14	250	367.0	367.0	38.0



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

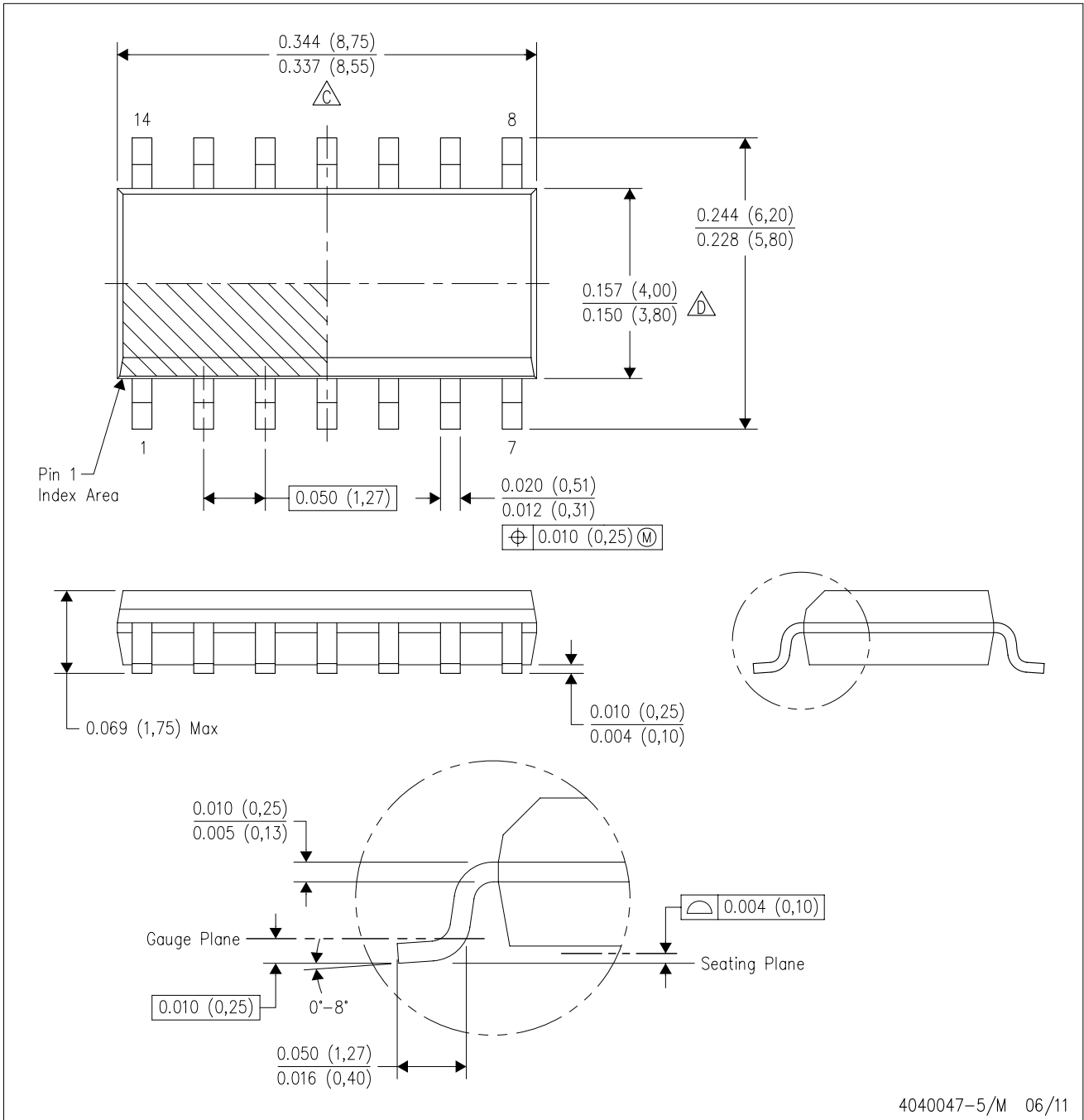
16 PINS SHOWN





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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