

CD40257B Types

CMOS Quad 2-Line-to-1-Line Data Selector/Multiplexer

High-Voltage Types (20-Volt Rating)

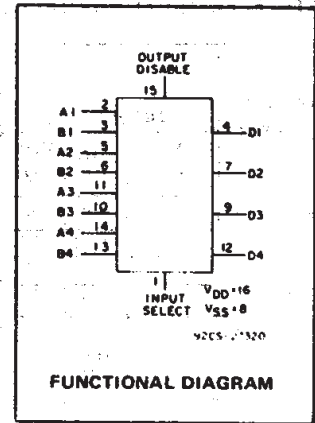
■ CD40257B is a Data Selector/Multiplexer featuring three-state outputs which can interface directly with and drive data lines of bus-oriented systems. The CD40257B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | |
| Voltages referenced to V _{SS} Terminal | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

Features:

- 3-state outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



Applications:

- Digital Multiplexing
- Shift-right/shift-left registers
- True/complement selection

RECOMMENDED OPERATING CONDITION

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|------|-------|
| | Min. | Max. | |
| Supply-Voltage Range (For T _A =Full Package-Temperature Range) | 3 | 18 | V |

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HIGH VOLTAGE ICs

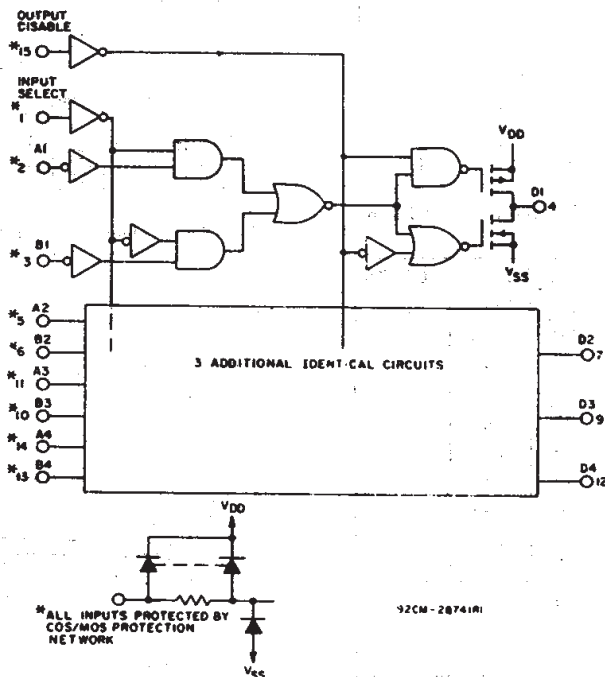


Fig. 1 - Logic diagram for CD40257B.

TRUTH TABLE

| 3-STATE OUTPUT DISABLE | INPUTS | | OUTPUT |
|------------------------|--------|-----|--------|
| | SELECT | A B | |
| 1 | X | X X | Z |
| 0 | 0 | 0 X | 0 |
| 0 | 0 | 1 X | 1 |
| 0 | 1 | X 0 | 0 |
| 0 | 1 | X 1 | 1 |

X = DON'T CARE LOGIC 1 = HIGH
LOGIC 0 = LOW Z = HIGH IMPEDANCE

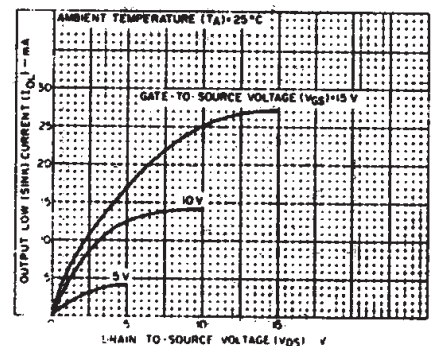


Fig. 2 - Typical output low (sink) current characteristics.

CD40257B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current I _{DD} Max. | - | 0.5 | 5 | 1 | 1 | 30 | 30 | - | 0.02 | 1 | μA |
| | - | 0.10 | 10 | 2 | 2 | 60 | 60 | - | 0.02 | 2 | |
| | - | 0.15 | 15 | 4 | 4 | 120 | 120 | - | 0.02 | 4 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0.5 | 5 | | | 0.05 | | | 0 | 0.05 | V |
| | - | 0.10 | 10 | | | 0.05 | | | 0 | 0.05 | |
| | - | 0.15 | 15 | | | 0.05 | | | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0.5 | 5 | | | 4.95 | | 4.95 | 5 | - | V |
| | - | 0.10 | 10 | | | 9.95 | | 9.95 | 10 | - | |
| | - | 0.15 | 15 | | | 14.95 | | 14.95 | 15 | - | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | | | 1.5 | | - | - | 1.5 | V |
| | 1.9 | - | 10 | | | 3 | | - | - | 3 | |
| | 1.5, 13.5 | - | 15 | | | 4 | | - | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | | | 3.5 | | 3.5 | - | - | V |
| | 1.9 | - | 10 | | | 7 | | 7 | - | - | |
| | 1.5, 13.5 | - | 15 | | | 11 | | 11 | - | - | |
| Input Current, I _{IN} Max. | - | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |
| 3-State Output Leakage Current I _{OUT} Max. | | 0.18 | 18 | ±0.4 | ±0.4 | ±12 | ±12 | - | ±10 ⁻⁴ | ±0.4 | μA |

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | UNITS | |
|---|-----------------|---------------------|------|-------|------|
| | | V _{DD} (V) | Typ. | | Max. |
| Propagation Delay Time: Data Input to Output, t _{PHL} , t _{PLH} | | 5 | 150 | 300 | ns |
| | | 10 | 70 | 140 | |
| | | 15 | 50 | 100 | |
| Select to Output, t _{PHL} , t _{PLH} | | 5 | 190 | 380 | ns |
| | | 10 | 85 | 170 | |
| | | 15 | 65 | 130 | |
| Output Disable to Output, t _{PHL} , t _{PLH} | | 5 | 95 | 190 | ns |
| | | 10 | 50 | 100 | |
| | | 15 | 40 | 80 | |
| Transition Time, t _{THL} , t _{TLH} | | 5 | 100 | 200 | ns |
| | | 10 | 50 | 100 | |
| | | 15 | 40 | 80 | |
| Input Capacitance, C _{IN} | Any Input | - | 5 | 7.5 | pF |

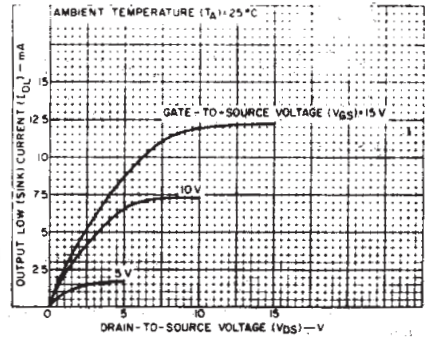


Fig.3 - Minimum output low (sink) current characteristics.

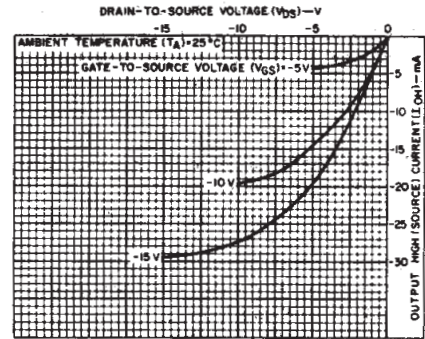


Fig.4 - Typical output high (source) current characteristics.

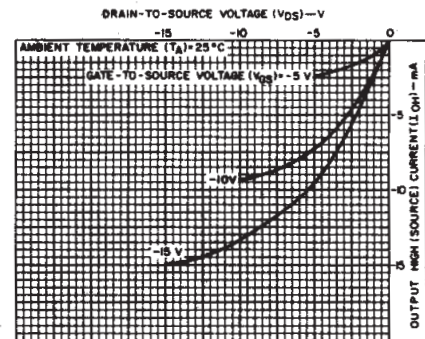


Fig.5 - Minimum output high (source) current characteristics.

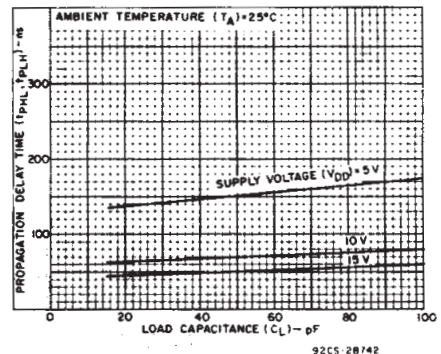


Fig.6 - Typical propagation delay time as a function of load capacitance (DATA INPUT to OUTPUT).

CD40257B Types

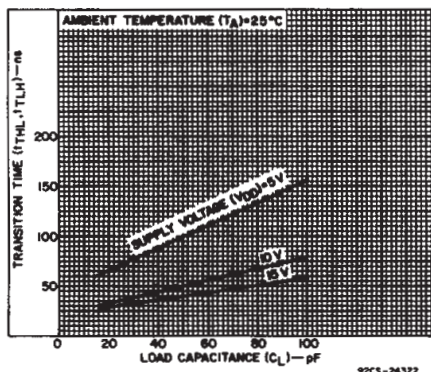


Fig.7 - Typical transition time as a function of load capacitance.

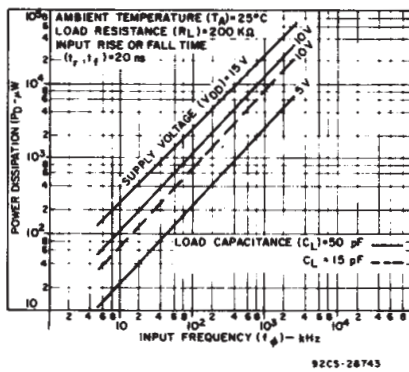


Fig.8 - Typical dynamic power dissipation as a function of input frequency (one INPUT to one OUTPUT).

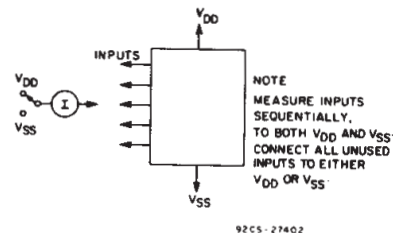


Fig.9 - Input current test circuit.

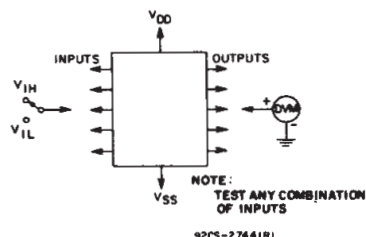


Fig.10 - Input voltage test circuit.

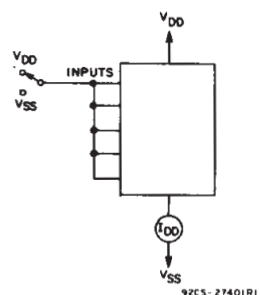
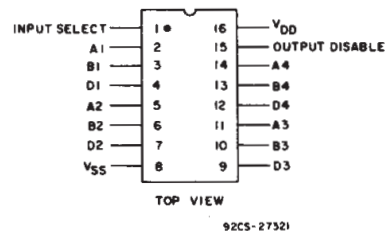
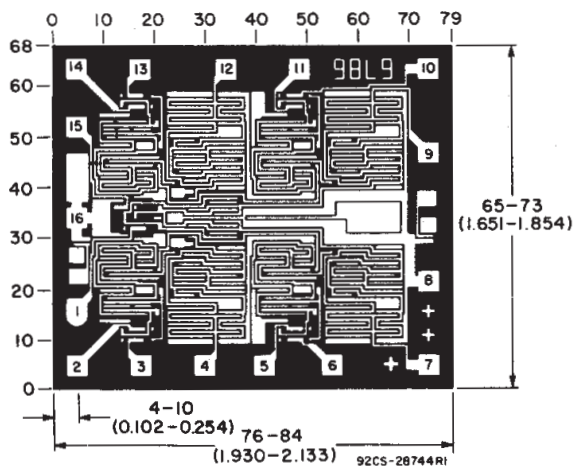


Fig.11 - Quiescent device current test circuit.



TERMINAL ASSIGNMENT

Dimensions and pad layout for CD40257BH.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|---|
| CD40257BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Contact TI Distributor or Sales Office |
| CD40257BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Contact TI Distributor or Sales Office |
| CD40257BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| CD40257BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD40257BME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD40257BMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD40257BMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD40257BMTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| CD40257BMTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD40257B, CD40257B-MIL :

- Catalog: [CD40257B](#)
- Military: [CD40257B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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