

**8-Line to 1-Line Data Selector/Multiplexer/Register  
With 3-State Outputs**

SCHS277D - November 1997 - Revised May 2003

**Features**

- HC/HCT354
  - Transparent Data and Select Latches
- Buffered Inputs
- Three-State Complementary Outputs
- Bus Line Driving Capability
- Typical Propagation Delay:  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^{\circ}C$ 
  - Data to Output = 18ns
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^{\circ}C$  to  $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

**Description**

The CD54HC354, CD74HC354, and CD74HCT354 are data selectors/multiplexers that select one of eight sources. In both types, the data select bits S0, S1 and S2 are stored in transparent latches that are enabled by a low latch enable input,  $\overline{LE}$ .

In the HC/HCT354 the data enable input,  $\overline{E}$ , controls transparent latches that pass data to the outputs when  $\overline{E}$  is high and latches in new data when  $\overline{E}$  is low.

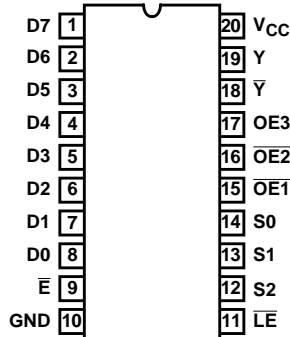
In both types the three-state outputs are controlled by three output-enable inputs OE1, OE2, and OE3.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC354F3A	-55 TO 125	20 Ld CERDIP
CD74HC354E	-55 to 125	20 Ld PDIP
CD74HCT354E	-55 to 125	20 Ld PDIP

**Pinout**

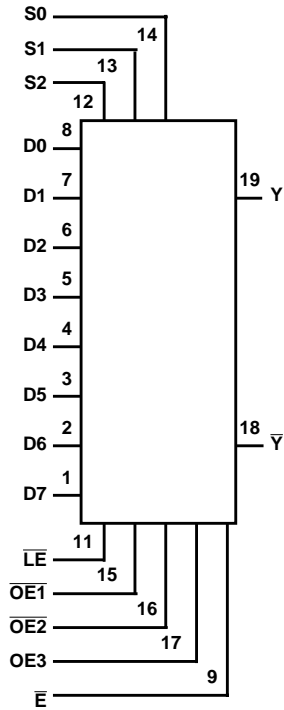
CD54HC354 (CERDIP)  
CD74HC354, CD74HCT354 (PDIP)  
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

CD54HC354, CD74HC354, CD74HCT354

Functional Diagram



TRUTH TABLE

INPUTS							OUTPUTS	
SELECT (NOTE 1)			ENABLE DATA	OUTPUT ENABLES				
S2	S1	S0	$\bar{E}$	$\bar{OE1}$	$\bar{OE2}$	OE3	$\bar{Y}$	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\bar{D0}$	D0
L	L	L	H	L	L	H	$\bar{D0}_n$	D0 <sub>n</sub>
L	L	H	L	L	L	H	$\bar{D1}$	D1
L	L	H	H	L	L	H	$\bar{D1}_n$	D1 <sub>n</sub>
L	H	L	L	L	L	H	$\bar{D2}$	D2
L	H	L	H	L	L	H	$\bar{D2}_n$	D2 <sub>n</sub>
L	H	H	L	L	L	H	$\bar{D3}$	D3
L	H	H	H	L	L	H	$\bar{D3}_n$	D3 <sub>n</sub>
H	L	L	L	L	L	H	$\bar{D4}$	D4
H	L	L	H	L	L	H	$\bar{D4}_n$	D4 <sub>n</sub>
H	L	H	L	L	L	H	$\bar{D5}$	D5
H	L	H	H	L	L	H	$\bar{D5}_n$	D5 <sub>n</sub>
H	H	L	L	L	L	H	$\bar{D6}$	D6
H	H	L	H	L	L	H	$\bar{D6}_n$	D6 <sub>n</sub>

**CD54HC354, CD74HC354, CD74HCT354**

TRUTH TABLE (Continued)

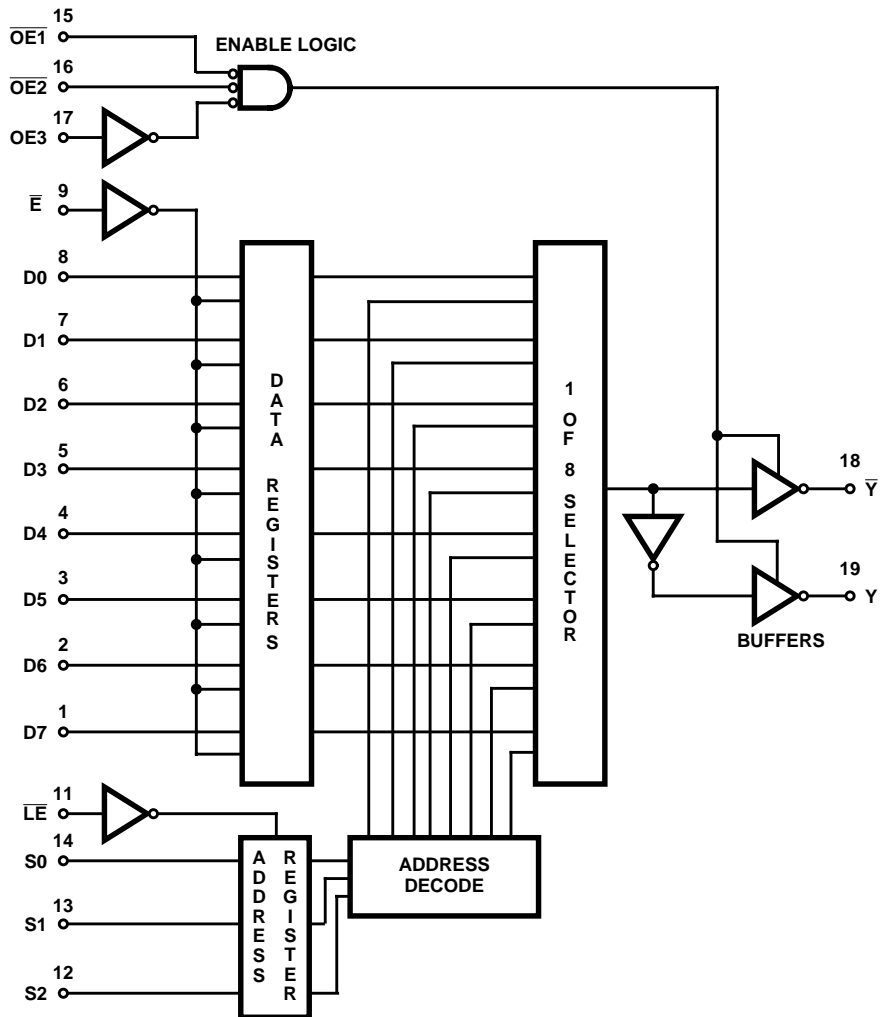
INPUTS							OUTPUTS	
SELECT (NOTE 1)			ENABLE DATA	OUTPUT ENABLES				
S2	S1	S0	$\bar{E}$	$\bar{OE1}$	$\bar{OE2}$	OE3	$\bar{Y}$	Y
H	H	H	L	L	L	H	$\bar{D7}$	D7
H	H	H	H	L	L	H	$\bar{D7}_n$	D7 <sub>n</sub>

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); X = Don't Care; Z = High Impedance State (Off State); D0<sub>n</sub>...D7<sub>n</sub> = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

NOTE:

1. This column shows the input address setup with  $\bar{LE}$  low.

**Block Diagram**



CD54HC354, CD74HC354, CD74HCT354

Logic Diagram

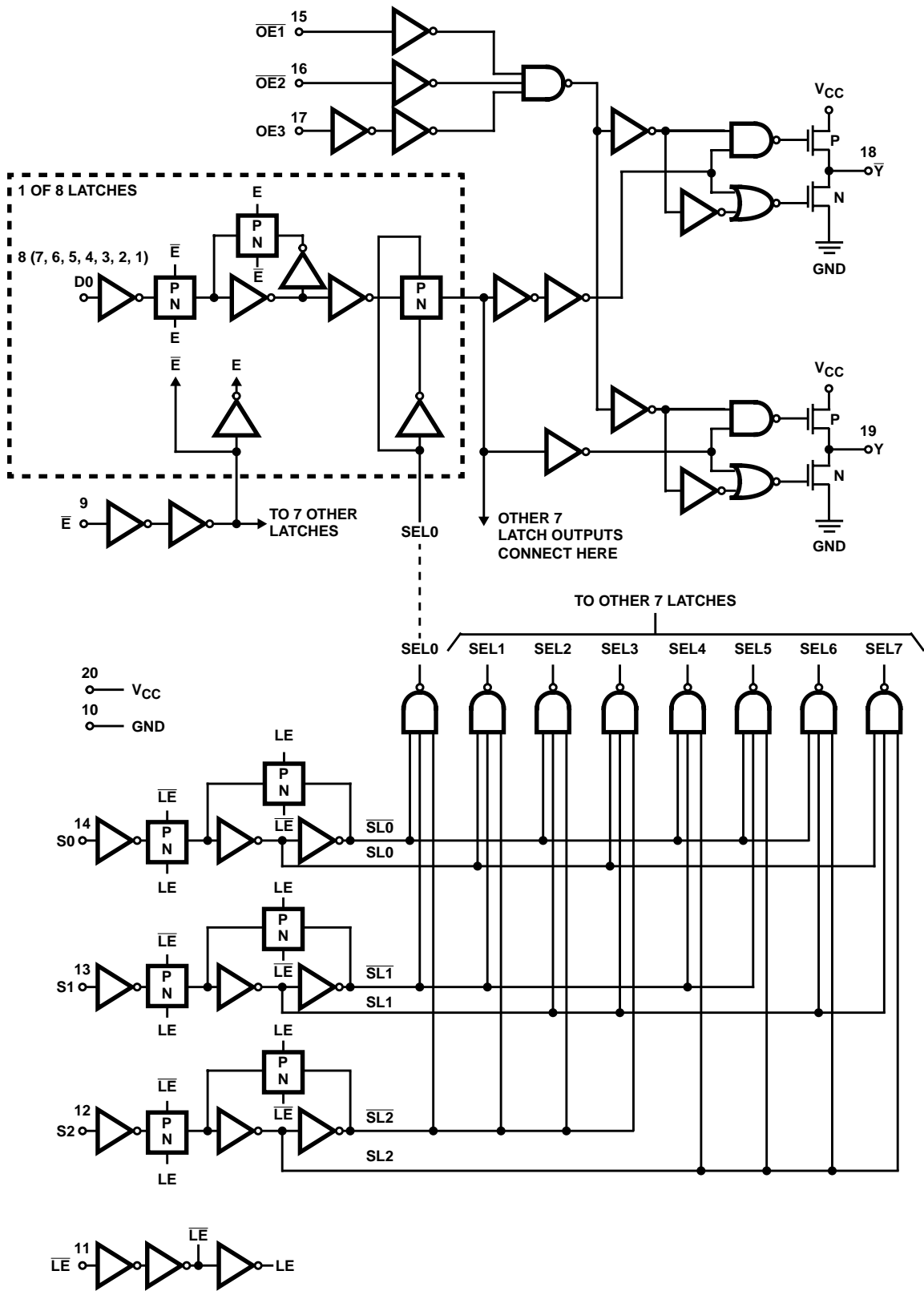


FIGURE 1. HC/HCT354 LOGIC DIAGRAM

# CD54HC354, CD74HC354, CD74HCT354

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ (°C/W)
E (PDIP) Package .....	69
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C
(SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range, $T_A$ .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads (Bus Driver)	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads (Bus Driver)	$V_{OL}$	$V_{IH}$ or $V_{IL}$	6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

## CD54HC354, CD74HC354, CD74HCT354

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5.0	-	±10	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 3)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	-	-	±0.5	-	±5.0	-	±10	μA

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
D0-D7	0.50
S0, S1, S3	0.70
OE1, OE2	0.80
OE3	0.25
LE	0.25
E	0.60

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

**CD54HC354, CD74HC354, CD74HCT354**

**Prerequisite For Switching Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
$\bar{E}$ Pulse Width	$t_{PLH}, t_{PHL}$	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
$\bar{LE}$ Pulse Width	$t_{PLH}, t_{PHL}$	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Set-up Times Dn $\rightarrow \bar{E}$	$t_{SU}$	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Set-up Times Sn $\rightarrow \bar{LE}$	$t_{SU}$	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Hold Times Dn $\rightarrow \bar{E}$	$t_H$	-	2	45	-	-	55	-	70	-	ns
			4.5	9	-	-	11	-	14	-	ns
			6	8	-	-	9	-	12	-	ns
Hold Times Sn $\rightarrow \bar{LE}$	$t_H$	-	2	45	-	-	55	-	70	-	ns
			4.5	9	-	-	11	-	14	-	ns
			6	8	-	-	9	-	12	-	ns
<b>HCT TYPES</b>											
$\bar{E}$ Pulse Width	$t_{PLH}, t_{PHL}$	-	4.5	16	-	-	20	-	24	-	ns
$\bar{LE}$ Pulse Width	$t_{PLH}, t_{PHL}$	-	4.5	16	-	-	20	-	24	-	ns
Set-up Times Dn $\rightarrow \bar{E}$	$t_{SU}$	-	4.5	10	-	-	13	-	15	-	ns
Set-up Times Sn $\rightarrow \bar{LE}$	$t_{SU}$	-	4.5	10	-	-	13	-	15	-	ns
Hold Times Dn $\rightarrow \bar{E}$	$t_H$	-	4.5	9	-	-	11	-	14	-	ns
Hold Times Sn $\rightarrow \bar{LE}$	$t_H$	-	4.5	9	-	-	11	-	14	-	ns

**Switching Specifications** Input  $t_r, t_f = 6ns$

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, Dn $\rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	C <sub>L</sub> = 50pF	2	-	210	265	315	ns
			4.5	-	42	53	63	ns
			6	-	36	45	54	ns
		C <sub>L</sub> = 15pF	5	18	-	-	-	ns
Propagation Delay, $\bar{E} \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	C <sub>L</sub> = 50pF	2	-	250	315	375	ns
			4.5	-	50	63	75	ns
			6	-	43	54	64	ns
		C <sub>L</sub> = 15pF	5	21	-	-	-	ns

**CD54HC354, CD74HC354, CD74HCT354**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, $S_n \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	260	325	390	ns
			4.5	-	52	65	78	ns
			6	-	44	55	66	ns
		$C_L = 15\text{pF}$	5	22	-	-	-	ns
Propagation Delay, $\bar{L}\bar{E} \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	290	365	435	ns
			4.5	-	58	73	87	ns
			6	-	49	62	74	ns
		$C_L = 15\text{pF}$	5	24	-	-	-	ns
Output Disabling Time, $\bar{O}\bar{E}_n$ to $Y, \bar{Y}$	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	2	-	155	195	235	ns
			4.5	-	31	39	47	ns
			6	-	26	33	40	ns
		$C_L = 15\text{pF}$	5	13	-	-	-	ns
Output Disabling Time, $O\bar{E}_3$ to $Y, \bar{Y}$	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	2	-	155	195	235	ns
			4.5	-	31	39	47	ns
			6	-	26	33	40	ns
		$C_L = 15\text{pF}$	5	13	-	-	-	ns
Output Enabling Time, $\bar{O}\bar{E}_n$ to $Y, \bar{Y}$	$t_{PZL}, t_{PZH}$	$C_L = 50\text{pF}$	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		$C_L = 15\text{pF}$	5	12, 13	-	-	-	ns
Output Enabling Time, $O\bar{E}_3$ to $Y, \bar{Y}$	$t_{PZL}, t_{PZH}$	$C_L = 50\text{pF}$	2	-	160	200	240	ns
			4.5	-	32	40	48	ns
			6	-	27	34	41	ns
		$C_L = 15\text{pF}$	5	12, 13	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	$C_I$	-	-	-	10	10	10	pF
Three-State Capacitance	$C_O$	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 4, 5)	$C_{PD}$	-	5	90	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay, $D_n \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	47	59	71	ns
		$C_L = 15\text{pF}$	5	20	-	-	-	ns
Propagation Delay, $\bar{E} \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	54	68	81	ns
		$C_L = 15\text{pF}$	5	23	-	-	-	ns



## CD54HC354, CD74HC354, CD74HCT354

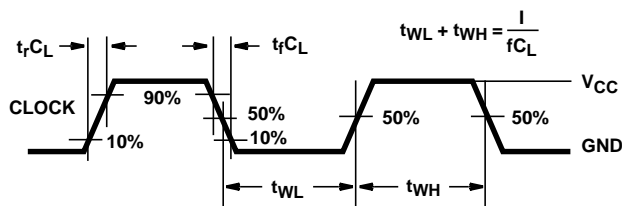
### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, $S_n \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	59	74	89	ns
		$C_L = 15\text{pF}$	5	25	-	-	-	ns
Propagation Delay, $\bar{LE} \rightarrow Y, \bar{Y}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	63	79	94	ns
		$C_L = 15\text{pF}$	5	25	-	-	-	ns
Output Disabling Time, $\bar{OE}_n \rightarrow Y, \bar{Y}$	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	33	41	50	ns
		$C_L = 15\text{pF}$	5	13, 16	-	-	-	ns
Output Disabling Time, $OE_3 \rightarrow Y, \bar{Y}$	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	39	49	59	ns
		$C_L = 15\text{pF}$	5	13, 16	-	-	-	ns
Output Enabling Time, $\bar{OE}_n \rightarrow Y, \bar{Y}$	$t_{PZL}, t_{PZH}$	$C_L = 50\text{pF}$	4.5	-	34	43	51	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Output Enabling Time, $OE_3 \rightarrow Y, \bar{Y}$	$t_{PZL}, t_{PZH}$	$C_L = 50\text{pF}$	4.5	-	34	43	51	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	12	15	18	ns
Input Capacitance	$C_{IN}$	-	-	-	10	10	10	pF
Three-State Capacitance	$C_O$	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 4, 5)	$C_{PD}$	-	5	92	-	-	-	pF

**NOTES:**

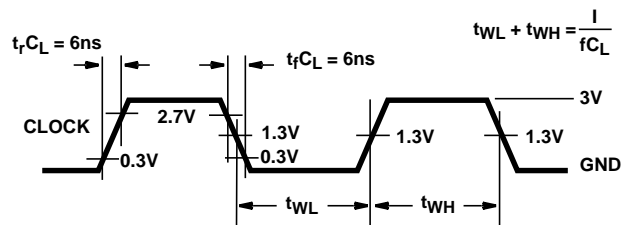
4.  $C_{PD}$  is used to determine the dynamic power consumption, per device.
5.  $P_D = V_{CC}^2 (C_{PD} + C_L) f_i$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

Test Circuits and Waveforms (Continued)

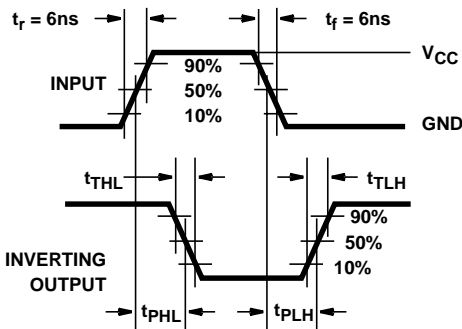


FIGURE 4. HC AND HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

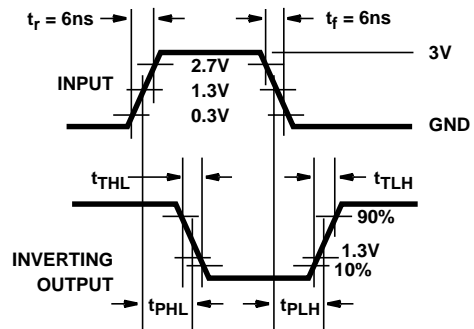


FIGURE 5. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

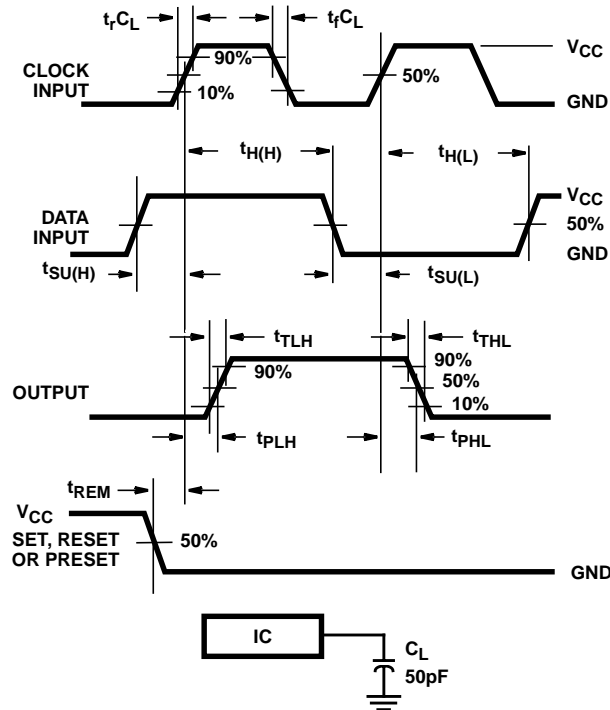


FIGURE 6. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

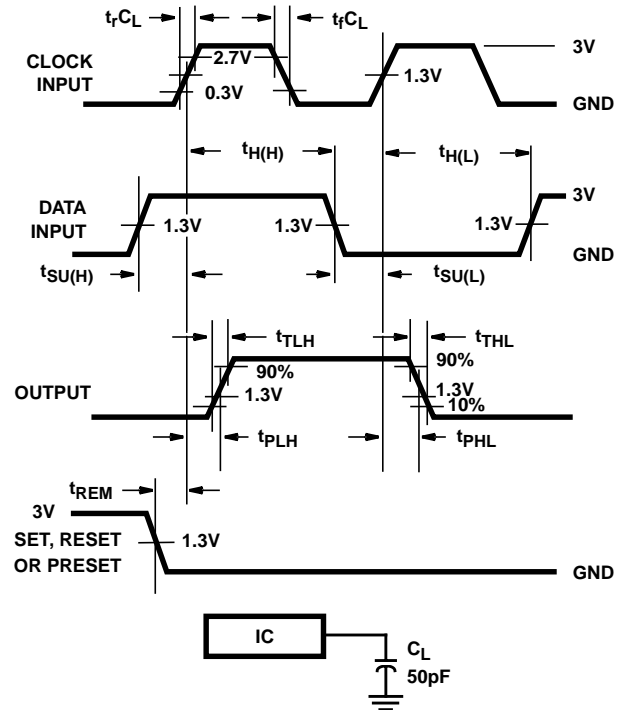


FIGURE 7. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**Test Circuits and Waveforms** (Continued)

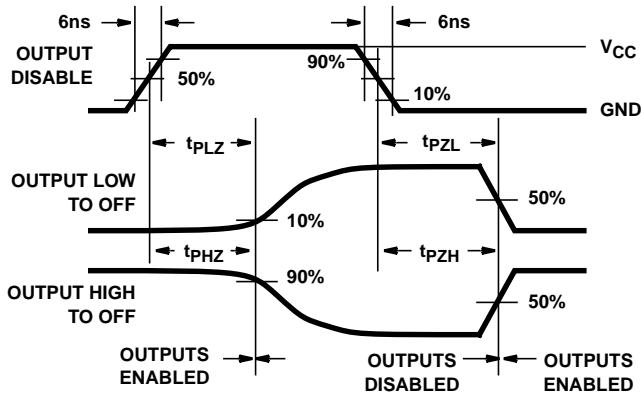


FIGURE 8. HC THREE-STATE PROPAGATION DELAY WAVEFORM

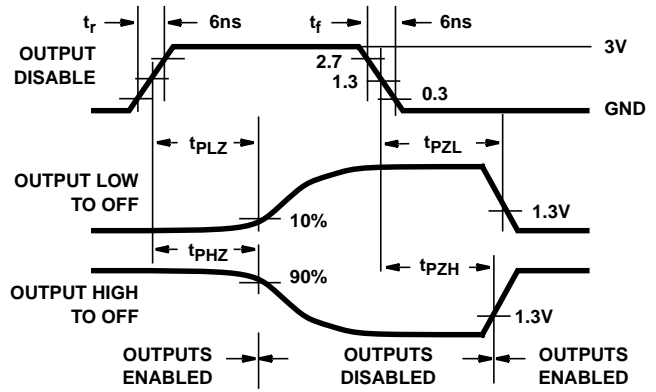
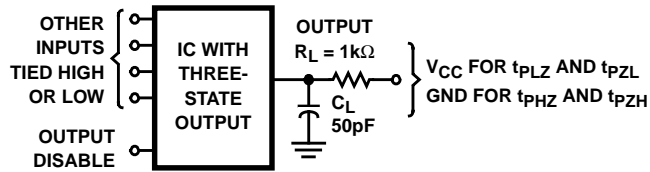


FIGURE 9. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 10. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54HC354F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD74HC354E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC354EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT354E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT354EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated