

CMOS HEX BUFFER/CONVERTER

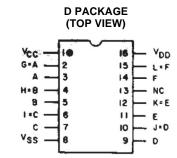
Check for Samples: CD4010B-Q1

FEATURES

- Qualified for Automotive Applications
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 µA at 18 V Over Full Package-Temperature Range: 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V Parametric Ratings
- Latch-Up Performance Meets 100 mA per JESD 78, Class I

APPLICATIONS

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- · CMOS High-to-Low Logic-Level Converter
- Multiplexer: 1-to-6 or 6-to-1



DESCRIPTION

CD4010B hex buffer/converter may be used as CMOS to TTL or DTL logic-level converters or CMOS high-sink-current drivers.

The CD4050B is the preferred hex buffer replacement for the CD4010B in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB hex inverter is recommended.

The CD4010B is supplied in 16-lead hermetic dual-in-line ceramic (D) packages.

ORDERING INFORMATION⁽¹⁾

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 125°C	SOIC - D	Reel of 2500	CD4010BQDRQ1	CD4010BQ	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

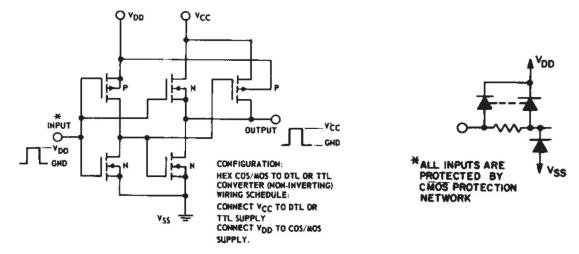
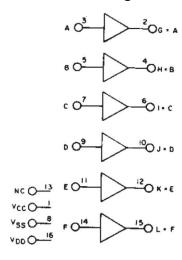


Figure 1. Schematic Diagram – One of Six Identical Stages

Functional Diagram





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{DD}	DC supply voltage range, voltage	s referenced to V _{SS} terminal	-0.5 to +20	V
	Input voltage range, all inputs		–0.5 to V _{DD} +0.5	V
	DC input current, any one input		±10	mA
		$T_A = -40^{\circ}\text{C to } +100^{\circ}\text{C}$	500	
P_D	Power dissipation per package	$T_A = +100^{\circ}C \text{ to } +125^{\circ}C$	Derate linearly at 12 mW/°C to 200 mW	mW
	Device dissipation per output transistor	T _A = full package-temperature range (all packages types)	100	mW
T _A	Operating temperature range	•	-40 to +125	°C
T _{stg}	Storage temperature range		-65 to +150	°C
	Latch-up performance per JESD 7	78, Class I	100	mA
		Human-body model (HBM)	500	
ESD	Electrostatic discharge rating (2)	Machine model (MM)	100	V
		Charged-Device Model (CDM)	1000	

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT	
V_{DD}	Supply voltage range ⁽¹⁾	3	18	. V	
V _{CC}	Supply voltage range **	3	V_{DD}	V	
V_{I}	Input voltage range	V_{CC}	V_{DD}	V	

(1) The CD4010B has high-to-low level voltage conversion capability, but not low-to-high level; therefore, it is recommended that V_{DD} > V_I > V_{CC}.

⁽²⁾ Tested in accordance with AEC-Q100.



STATIC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

		TEST	CONDIT	IONS	LIMIT	S AT IN	DICATED	TEMPER	ATURES	(°C)		
	PARAMETER		.,	v	40	0.5	405	+25			UNIT	
		v _o	V _{IN}	V_{DD}	-40	+85	+125	MIN	TYP	MAX		
			0, 5	5	1	30	30		0.02	1		
	Ouissant device current		0, 10	10	2	60	60		0.02	2		
I _{DD Max}	Quiescent device current		0, 15	15	4	120	120		0.02	4	μΑ	
			0,20	20	20	600	600		0.04	20		
		0.4	0, 5	4.5	3.1	2.1	1.8	2.6	3.4			
I Min	Output law (sink) surrent	0.4	0, 5	5	3.6	2.4	2.1	3	4		m 1	
I _{OL} Min	Output low (sink) current	0.5	0, 10	10	9.6	6.4	5.6	8	10		mA	
		1.5	0, 15	15	40	19	16	24	36			
	Output high (source) current	4.6	0, 5	5	-0.23	-0.18	-0.15	-0.2	-0.4		mA	
I Min		2.5	0, 5	5	-0.9	-0.65	-0.58	-0.8	-1.6			
I _{OH} Min		9.5	0, 10	10	-0.5	-0.38	-0.33	-0.45	-0.9			
		13.5	0, 15	15	-1.6	-1.25	-1.1	-1.5	-3			
	Output voltage: Low-level		0, 5	5		0.05			0	0.05	5 V	
V _{OL} Max			0, 10	10		0.05			0	0.05		
			0, 15	15		0.05			0	0.05		
			0, 5	5		4.95		4.95	5			
V _{OH} Min	Output voltage: High-level		0, 10	10		9.95		9.95	10		V	
			0, 15	15		14.95		14.95	15		1	
		0.5		5		1.5				1.5	-	
V _{IL} Max	Input low voltage	1		10		3				3		
		1.5		15		4				4	1	
		4.5		5		3.5		3.5				
V _{IH} Min	Input high voltage	9		10		7		7			V	
		13.5		15		11		11				
I _{IN} Max	Input current		0, 18	18	±0.1	±1	±1		±10 ⁻⁵	±0.1	μA	



DYNAMIC ELECTRICAL CHARACTERISTICS

 $T_A = 25^{\circ}C$, Input $t_r/t_f = 20$ ns, $C_L = 50$ pf, $R_L = 200$ k Ω

		TES	T CONDIT	IONS	LIMITS ALL		
	PARAMETER	V _{DD} (V)	V _I (V)	V _{CC} (V)	TYP	MAX	UNIT
		5	5	5	100	200	
		10	10	10	50	100	
t _{PLH}	Propagation delay time: low-to-high	10	10	5	50	100	ns
		15	15	15	35	70	
		15	15	5	35	70	
		5	5	5	65	130	ns
		10	10	10	35	70	
t _{PHL}	Propagation time: high-to-low	10	10	5	30	70	
		15	15	15	25	50	
		15	15	5	20	40	
		5	5	5	150	350	
t _{TLH}	Transition time: low-to-high	10	10	10	75	150	ns
		15	15	15	55	110	
		5	5	5	35	90	ns
t _{THL}	Transition time: high-to-low	10	10	10	20	45	
		15	15	15	15	40	
C _{IN}	Input capacitance				5	7.5	pF



TYPICAL CHARACTERISTICS

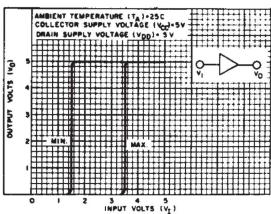


Figure 2. Minimum and Maximum Voltage Transfer Characteristics (V_{DD} = 5 V)

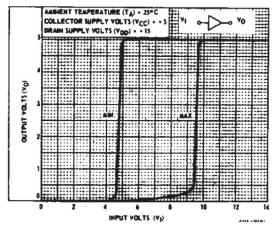


Figure 4. Minimum and Maximum Voltage Transfer Characteristics (V_{DD} = 15 V)

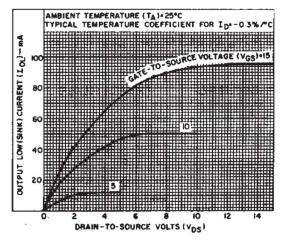


Figure 6. Typical Output Low (Sink) Current Characteristics

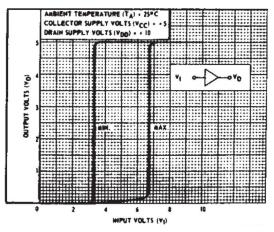


Figure 3. Minimum and Maximum Voltage Transfer Characteristics ($V_{DD} = 10 \text{ V}$)

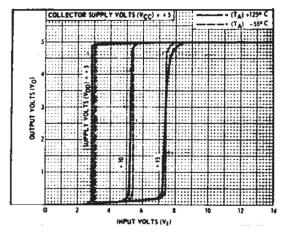


Figure 5. Typical Voltage Transfer Characteristics as a Function of Temperature

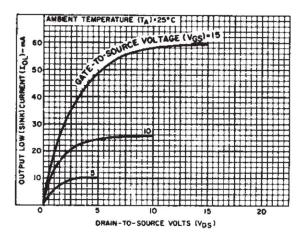


Figure 7. Minimum Output Low (Sink) Current Characteristics



TYPICAL CHARACTERISTICS (continued)

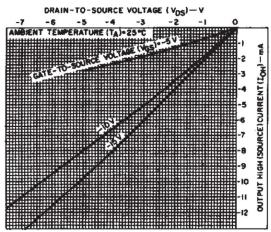


Figure 8. Typical Output High (Source) Current Characteristics

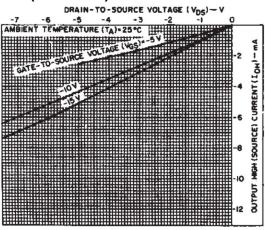


Figure 9. Minimum Output High (Source) Current Characteristics

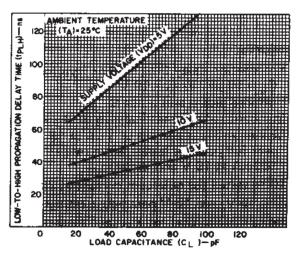


Figure 10. Typical Low-to-High Propagation Delay Time vs Load Capacitance

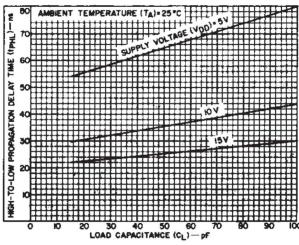


Figure 11. Typical High-to-Low Propagation Delay Time vs Load Capacitance

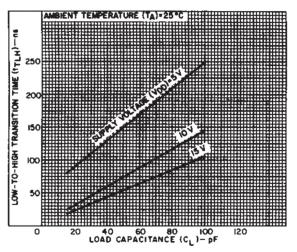


Figure 12. Typical Low-to-High Transition Time vs Load Capacitance

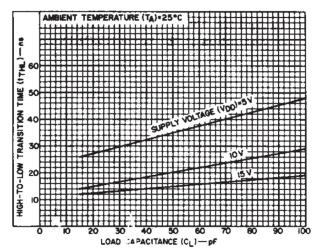
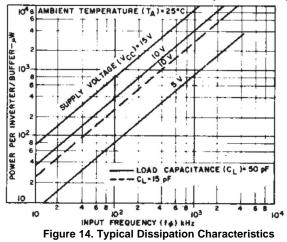


Figure 13. Typical High-to-Low Transition Time vs Load Capacitance



TYPICAL CHARACTERISTICS (continued)





PARAMETER MEASUREMENT INFORMATION

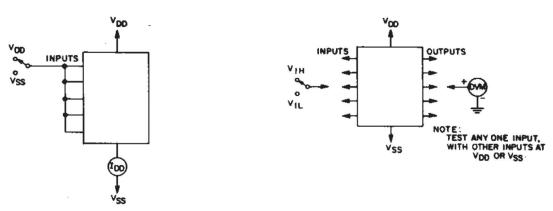


Figure 15. Quiescent Device Current Test Circuit

Figure 16. Noise Immunity Test Circuit

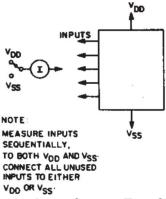
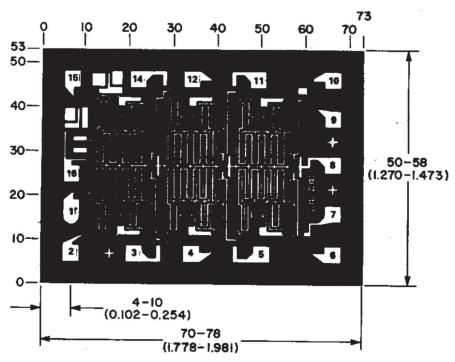


Figure 17. Input Current Test Circuit



Note: Dimensions in parentheses are in millimeters and are dereived from the basic inch dimensions as indicated. Grid graduation are in mils (10^{-3} inch) .

Figure 18. Dimensions and Layout



REVISION HISTORY

Cł	hanges from Original (March 2010) to Revision A	Page
•	Changed STATIC ELECTRICAL CHARACTERISTICS table to correct typos and misplaced data	

PACKAGE OPTION ADDENDUM

www.ti.com 16-Apr-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Pa	ckage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4010BQDRQ1	ACTIVE	SOIC	D	16 2	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD4010B-Q1:

Catalog: CD4010B

Military: CD4010B-MIL

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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