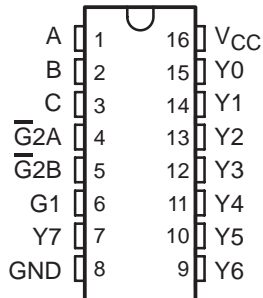


SN54HCT138, SN74HCT138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

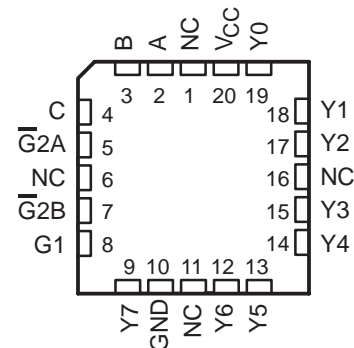
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- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 17$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception

SN54HCT138 . . . J OR W PACKAGE
SN74HCT138 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HCT138 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HCT138N | SN74HCT138N |
| | SOIC – D | Tube of 40 | SN74HCT138D | HCT138 |
| | | Reel of 2500 | SN74HCT138DR | |
| | | Reel of 250 | SN74HCT138DT | |
| | SOP – NS | Reel of 2000 | SN74HCT138NSR | HCT138 |
| | TSSOP – PW | Tube of 90 | SN74HCT138PW | HT138 |
| Reel of 2000 | | SN74HCT138PWR | | |
| Reel of 250 | | SN74HCT138PWT | | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HCT138J | SNJ54HCT138J |
| | CFP – W | Tube of 150 | SNJ54HCT138W | SNJ54HCT138W |
| | LCCC – FK | Tube of 55 | SNJ54HCT138FK | SNJ54HCT138FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HCT138, SN74HCT138 3-LINE TO 8-LINE DECODERS/DEMULPLEXERS

SCLS171E – MARCH 1984 – REVISED SEPTEMBER 2003

description/ordering information (continued)

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low (\overline{G}) and one active-high (G) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|--------|------------------|------------------|--------|---|---|---------|----|----|----|----|----|----|----|
| ENABLE | | | SELECT | | | | | | | | | | |
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | H | L | H | H | H | H | H | L | H | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

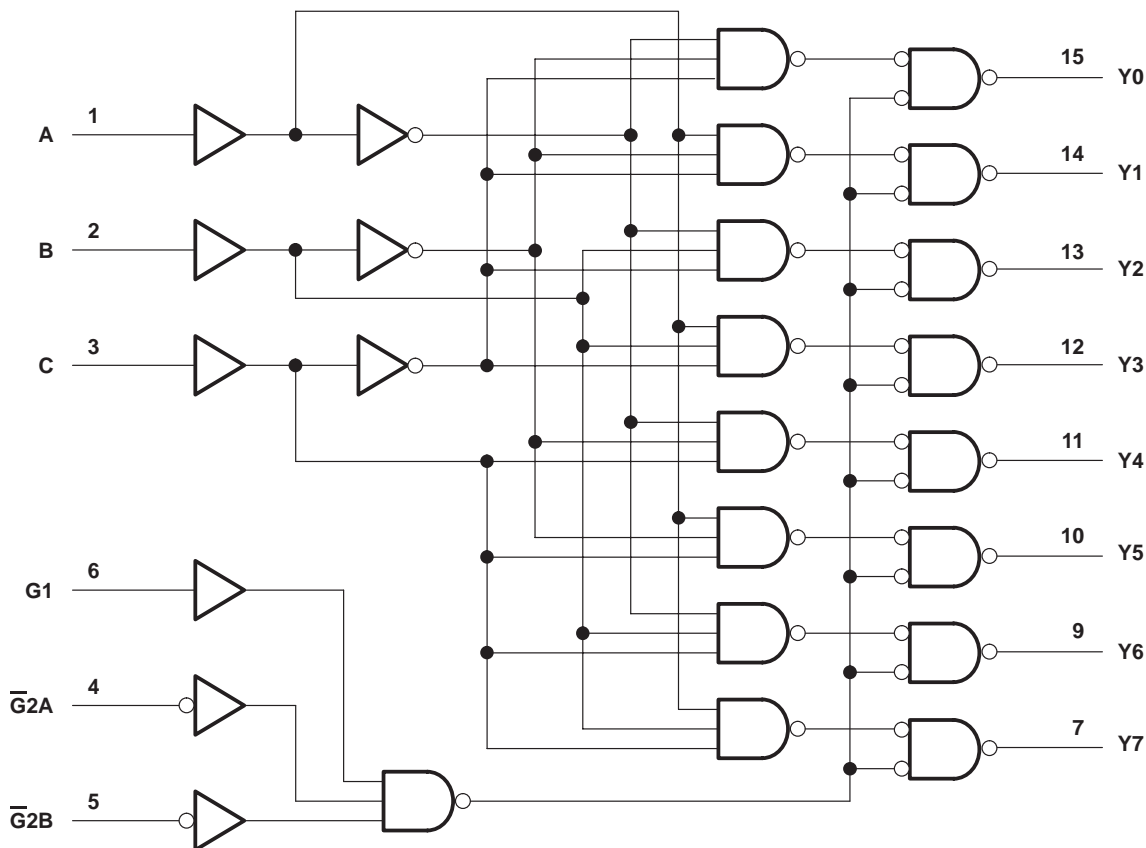


SN54HCT138, SN74HCT138

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCLS171E – MARCH 1984 – REVISED SEPTEMBER 2003

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.



SN54HCT138, SN74HCT138

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCLS171E – MARCH 1984 – REVISED SEPTEMBER 2003

recommended operating conditions (see Note 3)

| | | SN54HCT138 | | | SN74HCT138 | | | UNIT |
|---------------------|---------------------------------|---|-----|-----|------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | 2 | | | V |
| V_{IL} | Low-level input voltage | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | 0.8 | | | V |
| V_I | Input voltage | 0 | | | V_{CC} | | | V |
| V_O | Output voltage | 0 | | | V_{CC} | | | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | 500 | | | 500 | | | ns |
| T_A | Operating free-air temperature | -55 | | | 125 | | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT138 | | SN74HCT138 | | UNIT |
|-------------------------|--|----------------|-----------------------------|-----------|------------|------------|---------------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V_{OH} | $V_I = V_{IH}$ or V_{IL} | 4.5 V | $I_{OH} = -20\ \mu\text{A}$ | 4.4 | 4.499 | 4.4 | 4.4 | V | | |
| | | | $I_{OH} = -4\ \text{mA}$ | 3.98 | 4.3 | 3.7 | 3.84 | | | |
| V_{OL} | $V_I = V_{IH}$ or V_{IL} | 4.5 V | $I_{OL} = 20\ \mu\text{A}$ | 0.001 | 0.1 | 0.1 | 0.1 | V | | |
| | | | $I_{OL} = 4\ \text{mA}$ | 0.17 | 0.26 | 0.4 | 0.33 | | | |
| I_I | $V_I = V_{CC}$ or 0 | 5.5 V | ± 0.1 | ± 100 | ± 1000 | ± 1000 | nA | | | |
| I_{CC} | $V_I = V_{CC}$ or 0, $I_O = 0$ | 5.5 V | 8 | | 160 | 80 | μA | | | |
| ΔI_{CC}^\dagger | One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC} | 5.5 V | 1.4 | 2.4 | 3 | 2.9 | mA | | | |
| C_i | | 4.5 V to 5.5 V | 3 | 10 | 10 | 10 | pF | | | |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

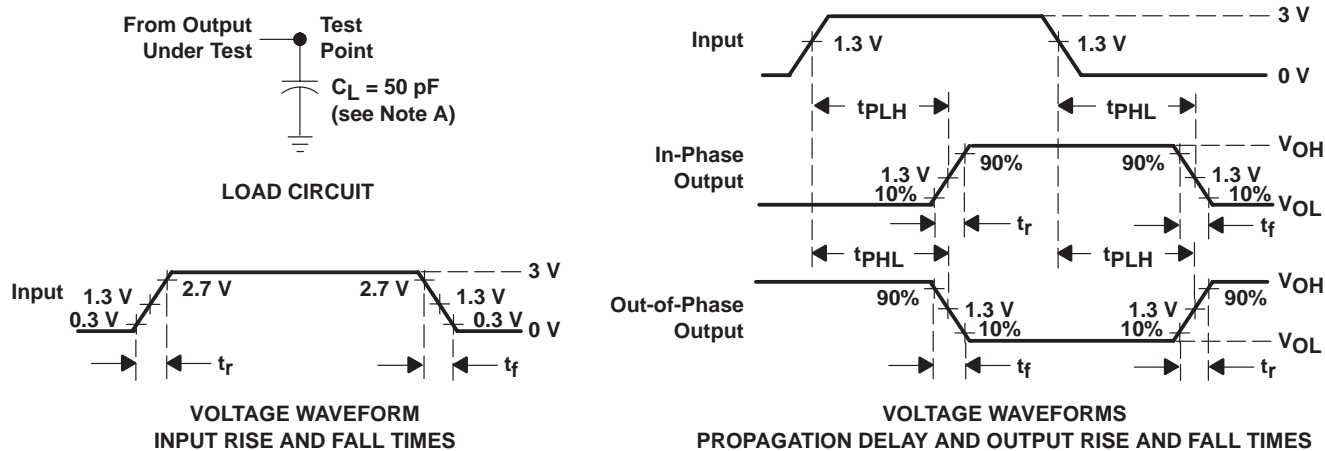
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT138 | | SN74HCT138 | | UNIT |
|-----------|--------------|-------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A, B, or C | Any Y | 4.5 V | 23 | 36 | 54 | 45 | ns | | | |
| | | | 5.5 V | 17 | 32 | 49 | 34 | | | | |
| | Enable | Any Y | 4.5 V | 22 | 33 | 50 | 42 | | | | |
| | | | 5.5 V | 18 | 30 | 45 | 38 | | | | |
| t_t | | Y | 4.5 V | 12 | 15 | 22 | 19 | ns | | | |
| | | | 5.5 V | 11 | 14 | 20 | 17 | | | | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | 85 | pF |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------------|-------------------------|
| 85504012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | -55 to 125 | 85504012A SNJ54HCT 138FK | Samples |
| 8550401EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | -55 to 125 | 8550401EA SNJ54HCT138J | Samples |
| 8550401FA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8550401FA SNJ54HCT138W | Samples |
| JM38510/65852BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65852BEA | Samples |
| M38510/65852BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65852BEA | Samples |
| SN54HCT138J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54HCT138J | Samples |
| SN74HCT138D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT138N | Samples |
| SN74HCT138N3 | OBsolete | PDIP | N | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------------|-------------------------|
| SN74HCT138NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT138N | Samples |
| SN74HCT138NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT138 | Samples |
| SN74HCT138PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWLE | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HCT138PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SN74HCT138PWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT138 | Samples |
| SNJ54HCT138FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 85504012A SNJ54HCT 138FK | Samples |
| SNJ54HCT138J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8550401EA SNJ54HCT138J | Samples |
| SNJ54HCT138W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54HCT138, SN74HCT138 :

● Catalog: [SN74HCT138](#)

● Military: [SN54HCT138](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT138DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT138PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT138PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT138DRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HCT138PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HCT138PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

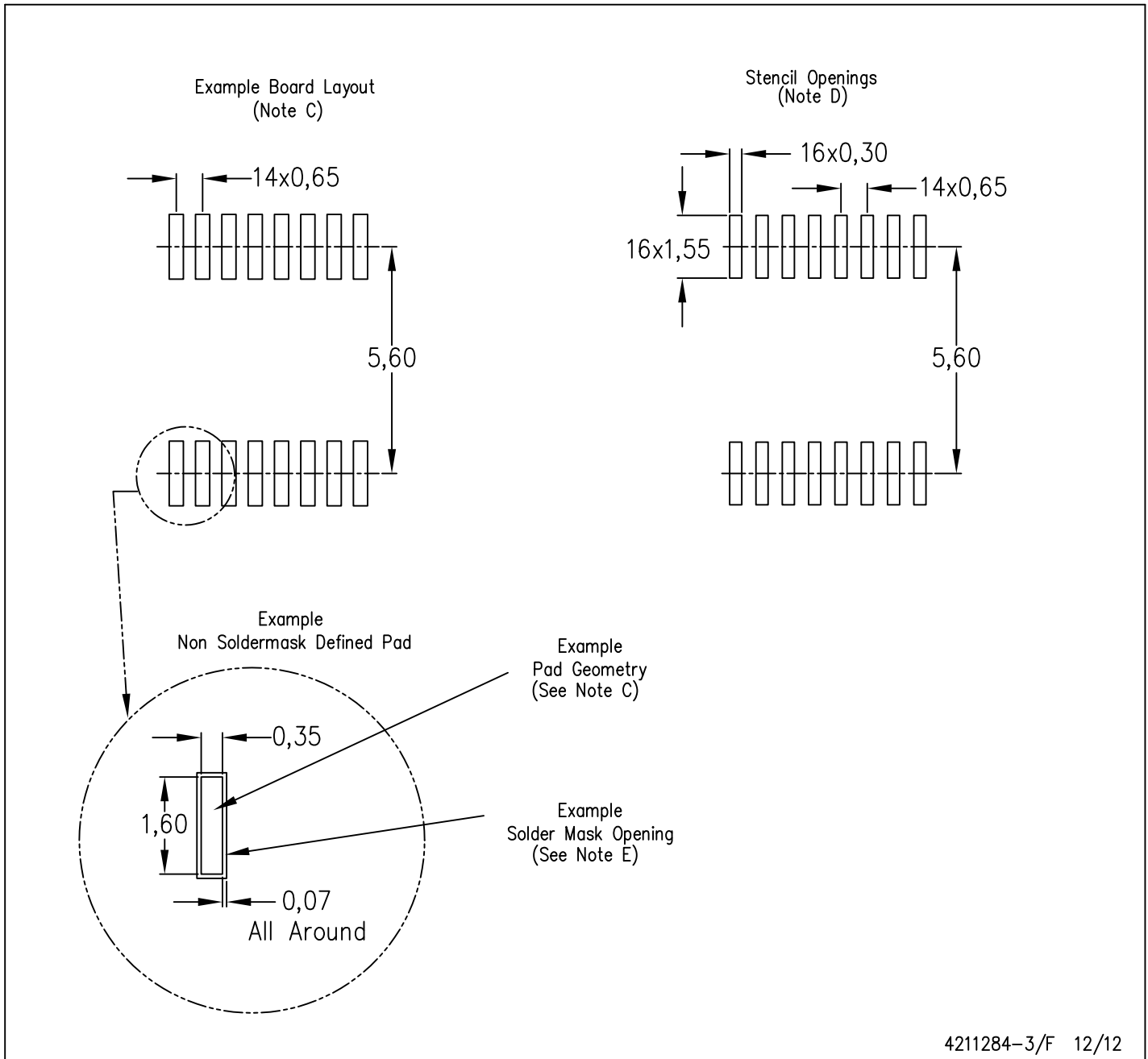


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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