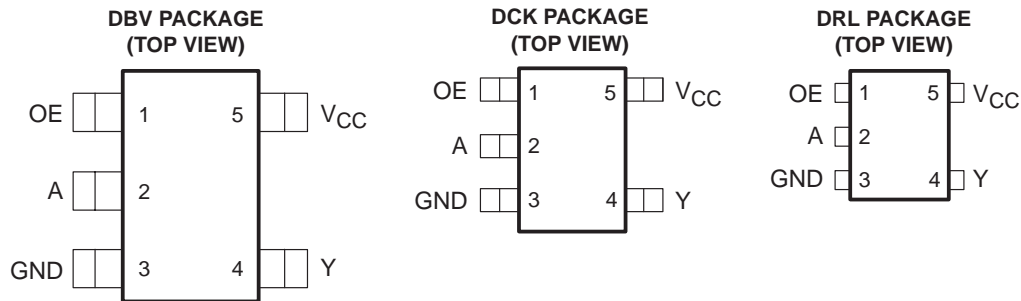


# SN74AHC1G126 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

SCLS379J – AUGUST 1997 – REVISED JUNE 2005

- Operating Range of 2 V to 5.5 V
- Max  $t_{pd}$  of 6 ns at 5 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17



See mechanical drawings for dimensions.

## description/ordering information

The SN74AHC1G126 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G126DBVR	A26_
		Reel of 250	SN74AHC1G126DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AHC1G126DCKR	AN_
		Reel of 250	SN74AHC1G126DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74AHC1G126DRLR	AN_

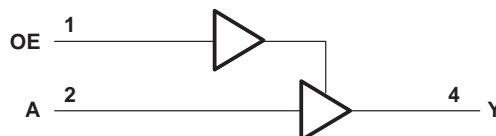
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ The actual top-side marking has one additional character that designates the assembly/test site.

## FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74AHC1G126

## SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package .....	206°C/W
..... DCK package .....	252°C/W
..... DRL package .....	142°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	-50	µA
		$V_{CC} = 3.3$ V ± 0.3 V	-4	mA
		$V_{CC} = 5$ V ± 0.5 V	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	µA
		$V_{CC} = 3.3$ V ± 0.3 V	4	mA
		$V_{CC} = 5$ V ± 0.5 V	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**SINGLE BUS BUFFER GATE**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25	±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			1	10	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10	10	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		10			pF	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		5.6	8	1	9.5	ns
t <sub>PHL</sub>					5.6	8	1	9.5	
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 15 pF		5.4	8	1	9.5	ns
t <sub>PZL</sub>					5.4	8	1	9.5	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 15 pF		7	9.7	1	11.5	ns
t <sub>PLZ</sub>					7	9.7	1	11.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		8.1	11.5	1	13	ns
t <sub>PHL</sub>					8.1	11.5	1	13	
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 50 pF		7.9	11.5	1	13	ns
t <sub>PZL</sub>					7.9	11.5	1	13	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50 pF		9.5	13.2	1	15	ns
t <sub>PLZ</sub>					9.5	13.2	1	15	



**SN74AHC1G126**  
**SINGLE BUS BUFFER GATE**  
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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

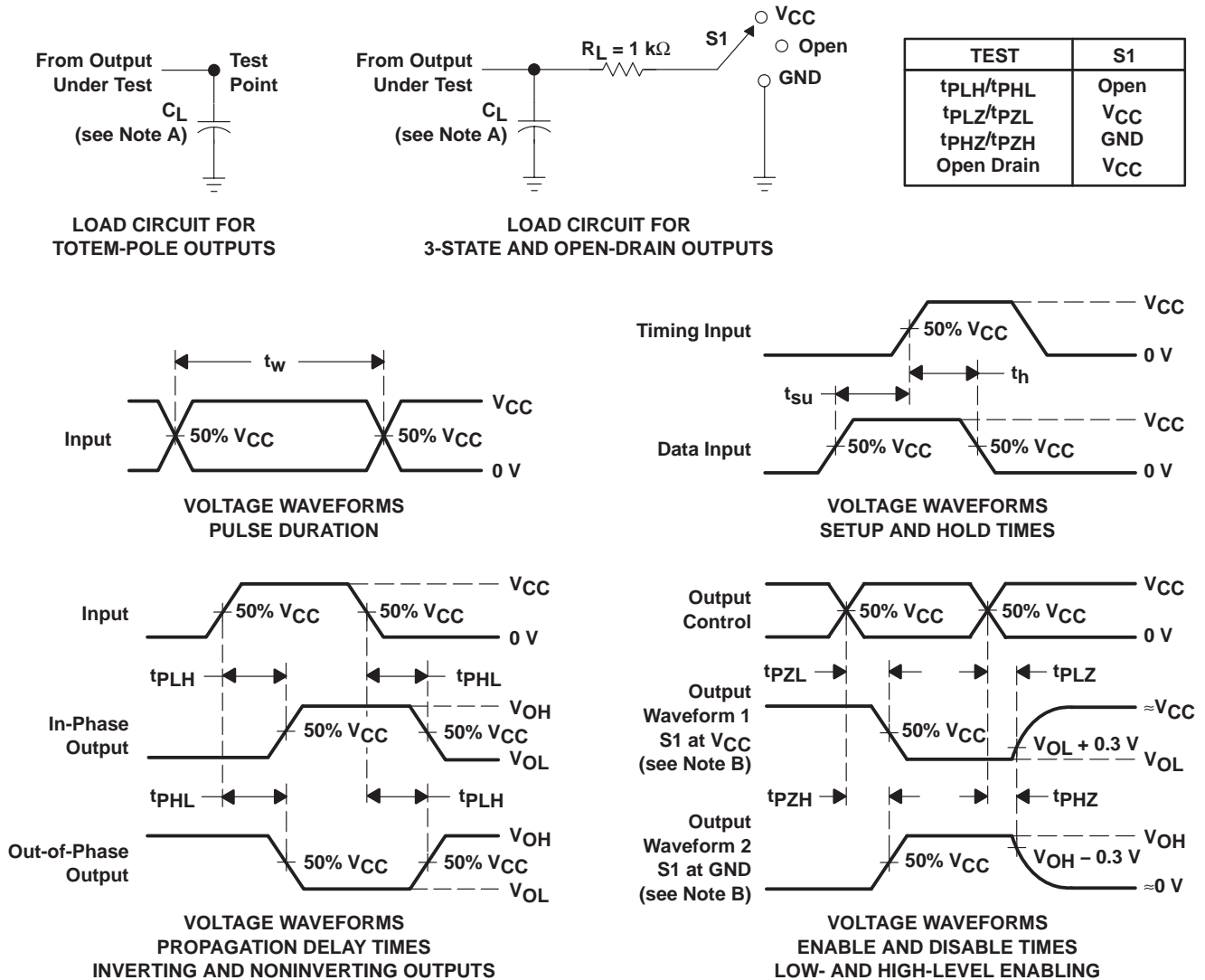
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	3.8	5.5	1	6.5	ns	
$t_{PHL}$				3.8	5.5	1	6.5		
$t_{PZH}$	OE	Y	$C_L = 15\text{ pF}$	3.6	5.1	1	6	ns	
$t_{PZL}$				3.6	5.1	1	6		
$t_{PHZ}$	OE	Y	$C_L = 15\text{ pF}$	4.6	6.8	1	8	ns	
$t_{PLZ}$				4.6	6.8	1	8		
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	ns	
$t_{PHL}$				5.3	7.5	1	8.5		
$t_{PZH}$	OE	Y	$C_L = 50\text{ pF}$	5.1	7.1	1	8	ns	
$t_{PZL}$				5.1	7.1	1	8		
$t_{PHZ}$	OE	Y	$C_L = 50\text{ pF}$	6.1	8.8	1	10	ns	
$t_{PLZ}$				6.1	8.8	1	10		

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF



**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time, with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74AHC1G126DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A263 ~ A26G ~ A26J ~ A26S)	<a href="#">Samples</a>
74AHC1G126DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A263 ~ A26G ~ A26J ~ A26S)	<a href="#">Samples</a>
74AHC1G126DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A263 ~ A26G ~ A26S)	<a href="#">Samples</a>
74AHC1G126DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A263 ~ A26G ~ A26S)	<a href="#">Samples</a>
74AHC1G126DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AN3 ~ ANG ~ ANJ ~ ANS)	<a href="#">Samples</a>
74AHC1G126DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AN3 ~ ANG ~ ANJ ~ ANS)	<a href="#">Samples</a>
74AHC1G126DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AN3 ~ ANG ~ ANS)	<a href="#">Samples</a>
74AHC1G126DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AN3 ~ ANG ~ ANS)	<a href="#">Samples</a>
74AHC1G126DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ANS	<a href="#">Samples</a>
SN74AHC1G126DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A263 ~ A26G ~ A26J ~ A26S)	<a href="#">Samples</a>
SN74AHC1G126DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A263 ~ A26G ~ A26S)	<a href="#">Samples</a>
SN74AHC1G126DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AN3 ~ ANG ~ ANJ ~ ANS)	<a href="#">Samples</a>
SN74AHC1G126DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AN3 ~ ANG ~ ANS)	<a href="#">Samples</a>
SN74AHC1G126DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ANS	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G126DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74AHC1G126DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G126DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G126DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74AHC1G126DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G126DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G126DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G126DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G126DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G126DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G126DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G126DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G126DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G126DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G126DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G126DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G126DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G126DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

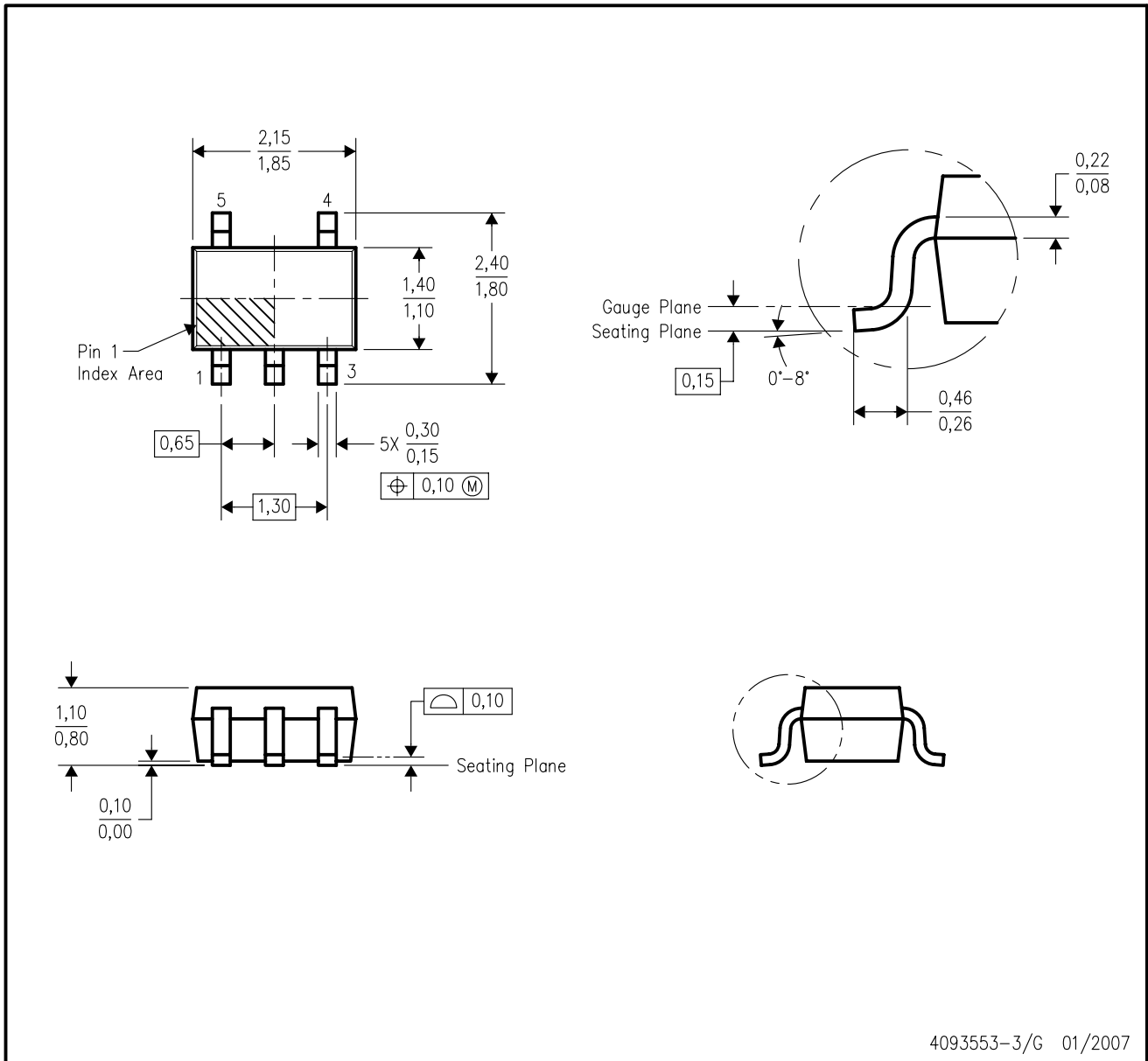
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



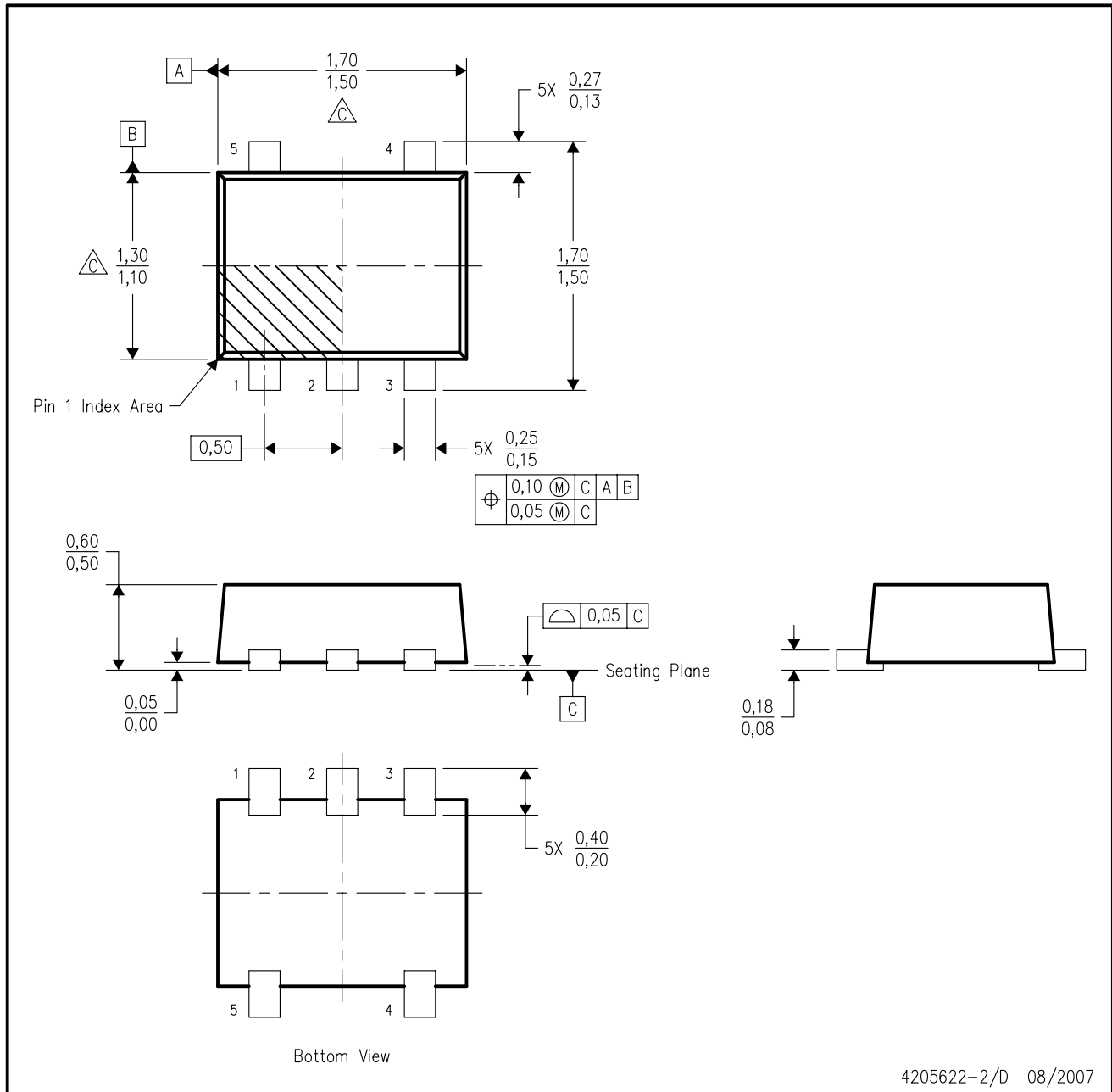
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

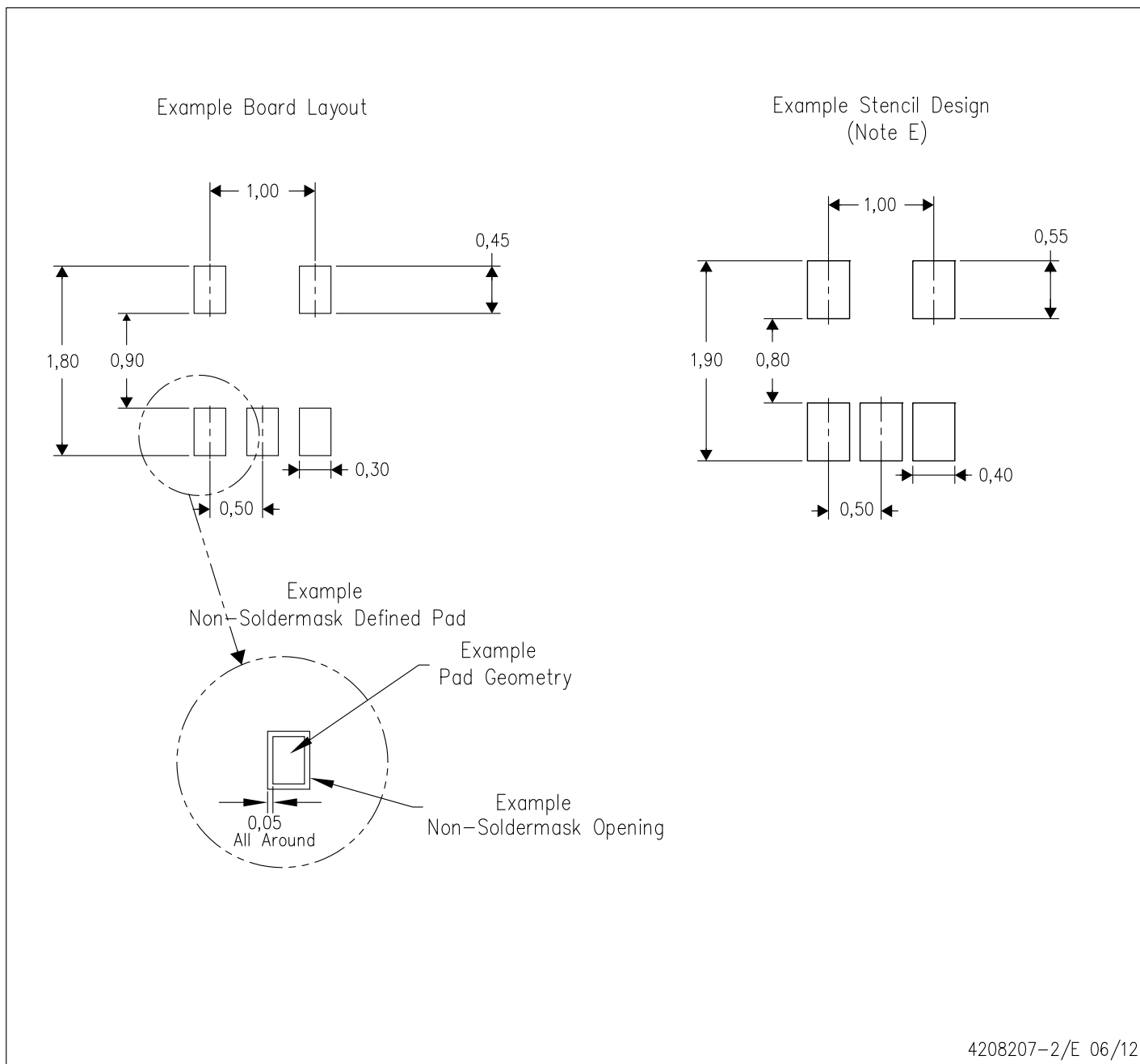
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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