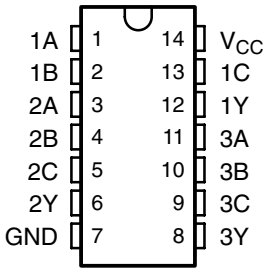
- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **2-V to 6-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 6 V**
- **Max $t_{pd}$ of 7.5 ns at 5 V**

**D PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ’AC11 device contains three independent 3-input AND gates. This device performs the Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

**ORDERING INFORMATION†**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SOIC – D | Tape and reel | SN74AC11IDRQ1 | AC11IQ1 |
| | TSSOP – PW | Tape and reel | SN74AC11IPWRQ1 | AC11IQ1 |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

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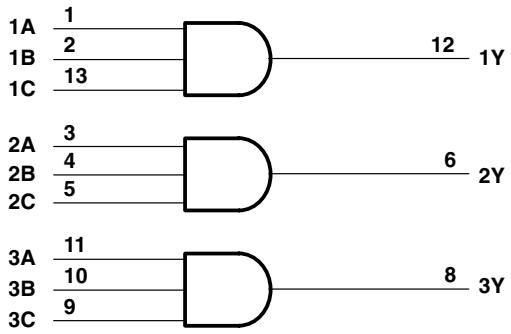
## logic diagram, each gate (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 86°C/W
PW package . . . . . 113°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | –12 | mA |
| | | $V_{CC}$ = 4.5 V | | –24 | |
| | | $V_{CC}$ = 5.5 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | 24 | |
| | | $V_{CC}$ = 5.5 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 8 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 3 V | 2.9 | 2.99 | | 2.9 | | V |
| | | 4.5 V | 4.4 | 4.49 | | 4.4 | | |
| | | 5.5 V | 5.4 | 5.49 | | 5.4 | | |
| | $I_{OH}$ = –12 mA | 3 V | 2.56 | | | 2.46 | | |
| | $I_{OH}$ = –24 mA | 4.5 V | 3.86 | | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.76 | | |
| | $I_{OH}$ = –50 mA† | 5.5 V | | | | | | |
| | $I_{OH}$ = –75 mA† | 5.5 V | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 3 V | | 0.002 | 0.1 | | 0.1 | V |
| | | 4.5 V | | 0.001 | 0.1 | | 0.1 | |
| | | 5.5 V | | 0.001 | 0.1 | | 0.1 | |
| | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 50 mA† | 5.5 V | | | | | | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | μA |
| $C_i$ | VI = $V_{CC}$ or GND | 5 V | | 2.6 | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | 1.5 | 5.5 | 9.5 | 1 | 10 | ns |
| $t_{PHL}$ | | | 1.5 | 5.5 | 8.5 | 1 | 9.5 | |

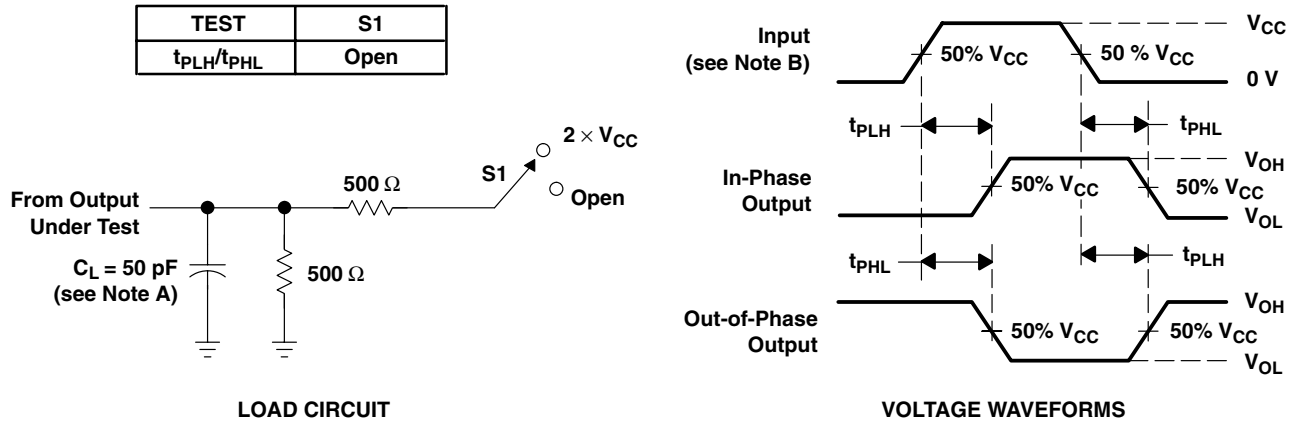
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A, B, or C | Y | 1.5 | 4 | 8 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | 1.5 | 4 | 7 | 1 | 7.5 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50pF, | f = 1 MHz | 20 | pF |

## PARAMETER MEASUREMENT INFORMATION




**LOAD CIRCUIT** **VOLTAGE WAVEFORMS**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AC11IDRG4Q1 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC11IQ1 | Samples |
| SN74AC11IDRQ1 | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 85 | AC11IQ1 | |
| SN74AC11IPWRG4Q1 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC11IQ1 | Samples |
| SN74AC11IPWRQ1 | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | AC11IQ1 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**OTHER QUALIFIED VERSIONS OF SN74AC11-Q1 :**

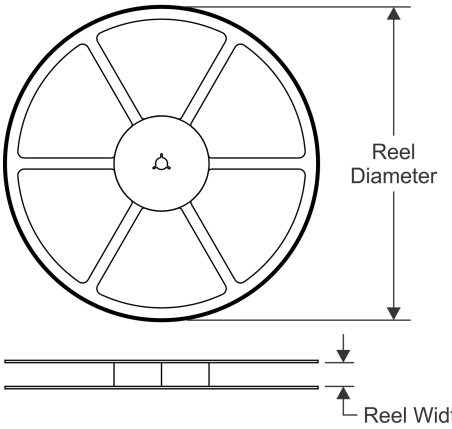
- Catalog: SN74AC11
- Enhanced Product: SN74AC11-EP
- Military: SN54AC11

NOTE: Qualified Version Definitions:

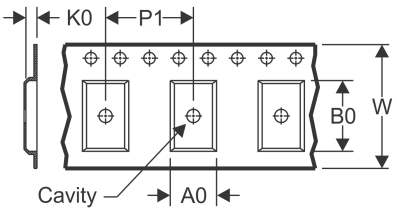
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

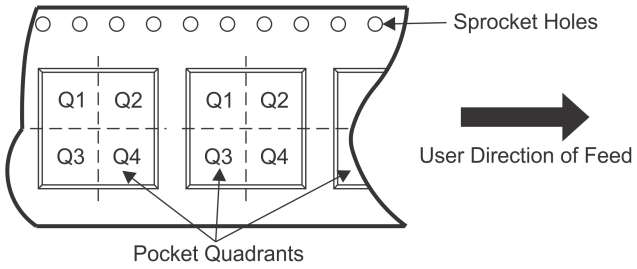



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

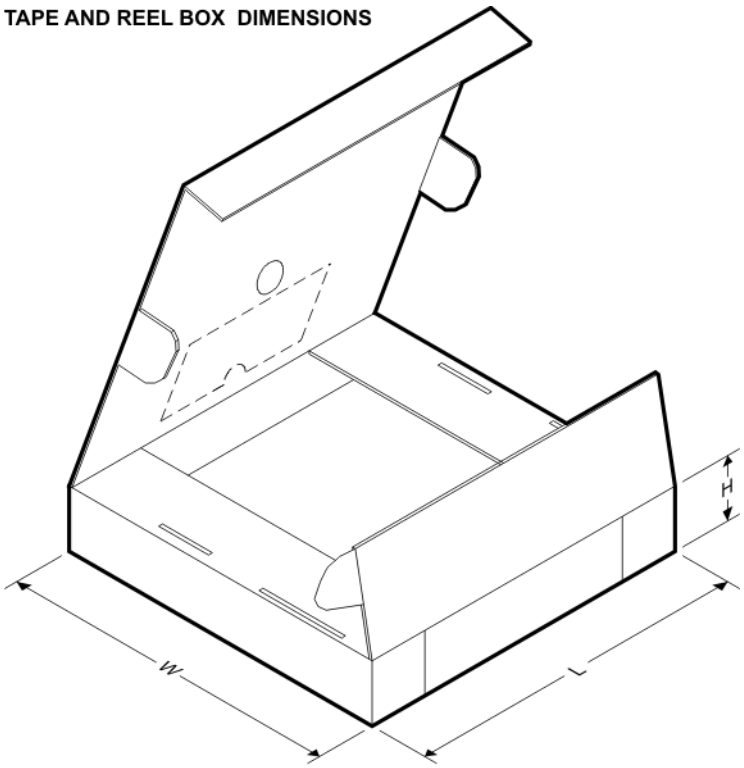
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AC11IPWRG4Q1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

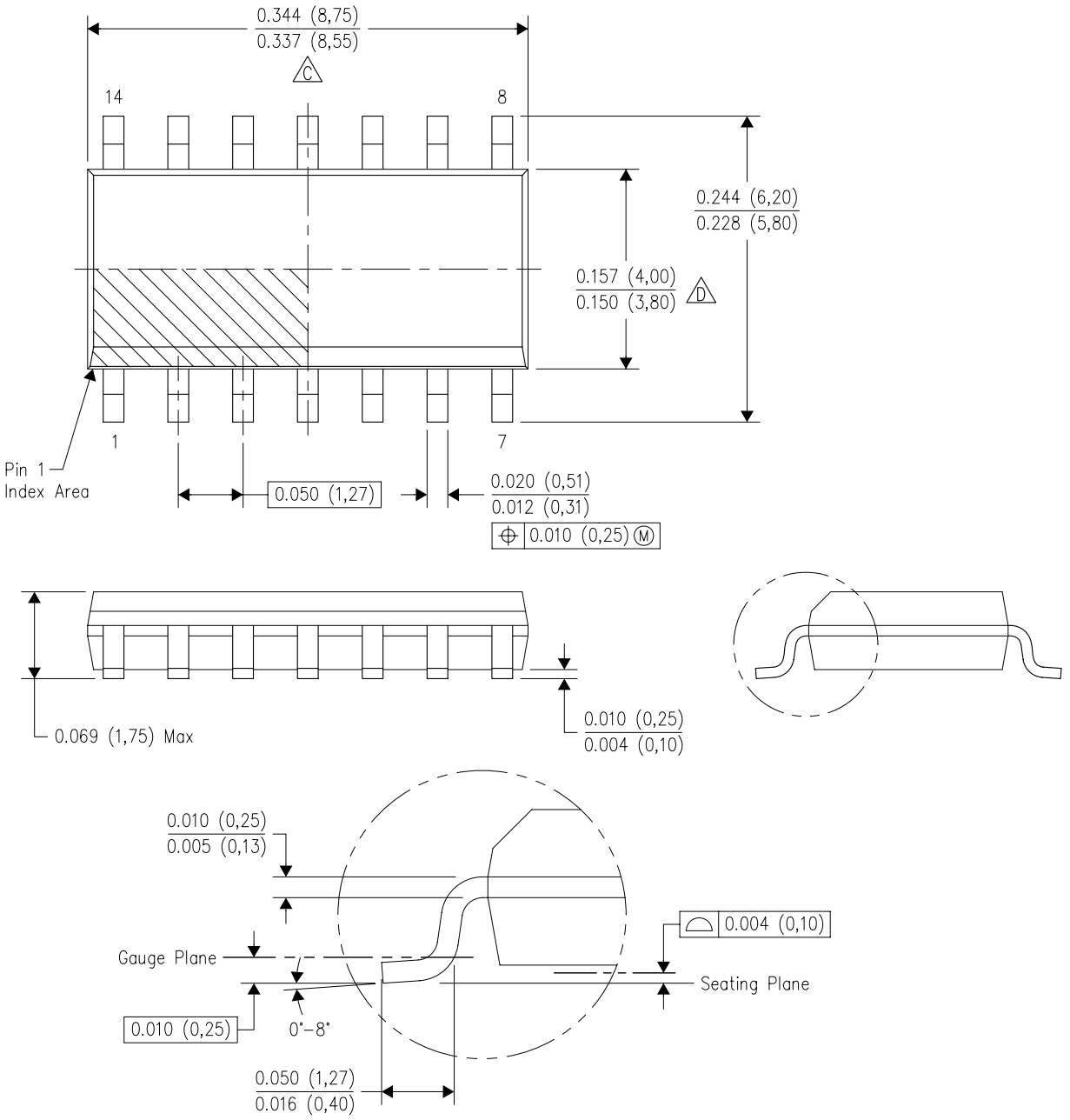
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AC11IPWRG4Q1 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

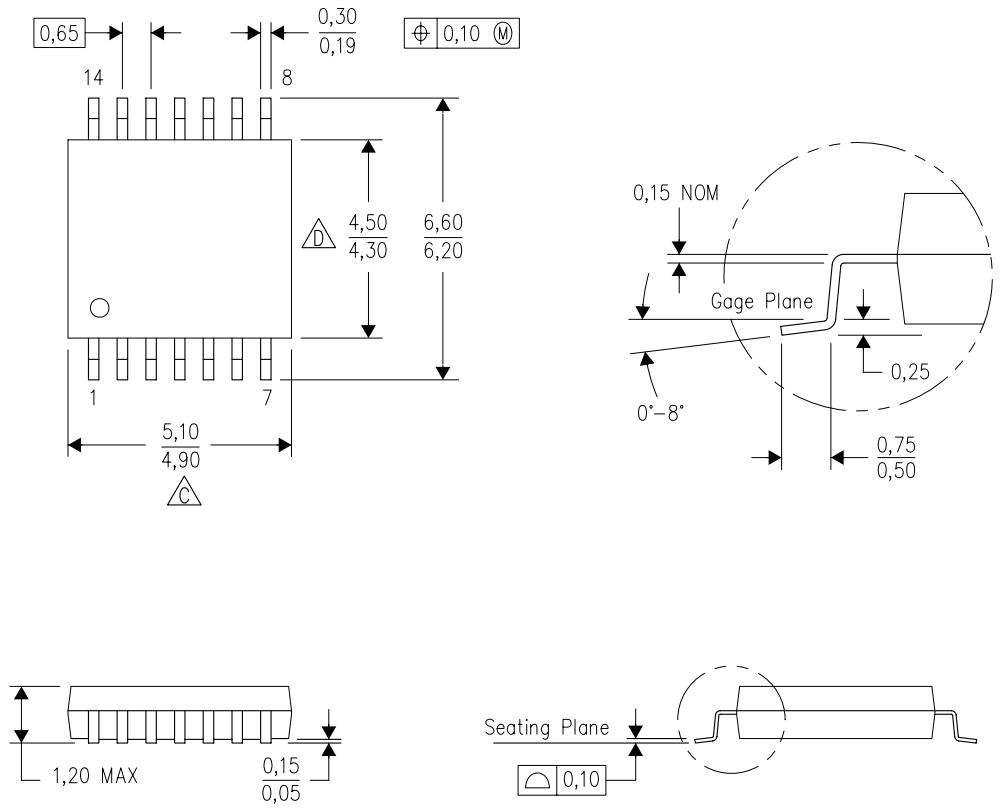
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

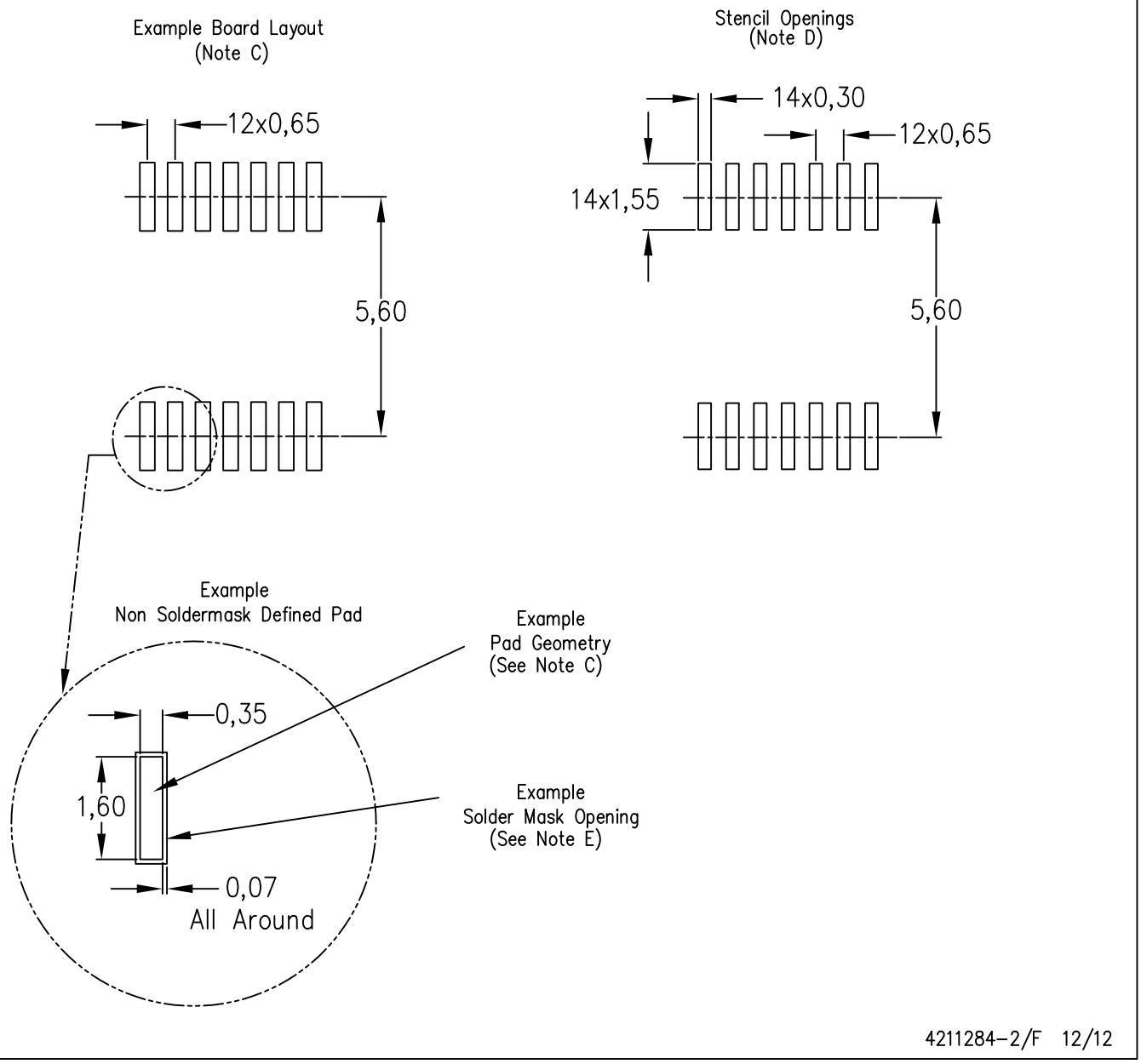
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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