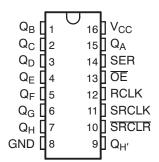


8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

Check for Samples: SN74LV595A-Q1

FEATURES

- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift
- I_{off} Supports Partial-Power-Down Mode Operation
- · Shift Register Has Direct Clear



DESCRIPTION

The SN74LV595A is an 8-bit shift register designed for 2-V to 5.5-V V_{CC} operation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (\overline{SRCLR}) input, serial (\overline{SER}) input, and a serial output for cascading. When the output-enable (\overline{OE}) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP - PW	Reel of 2000	SN74LV595AIPWRQ1	LV595AI
-40°C to 125°C	TSSOP - PW	Reel of 2000	SN74LV595AQPWRQ1	LV595AQ

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

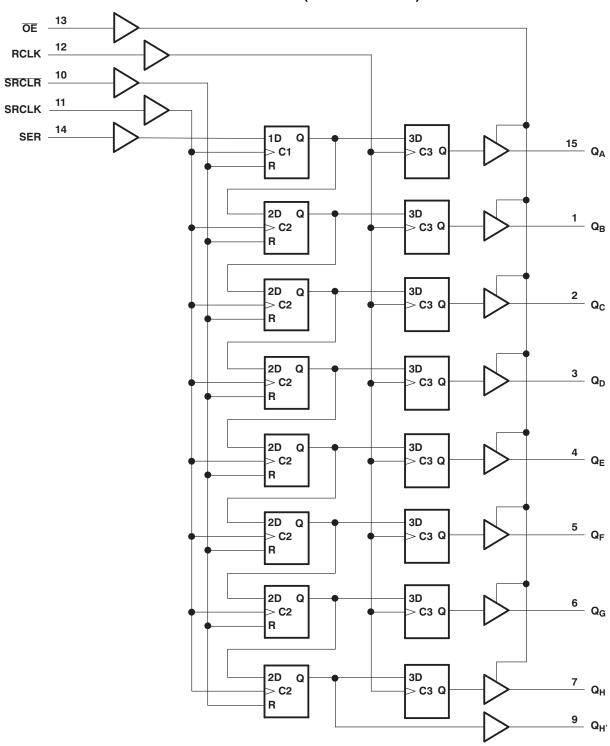


Table 1. FUNCTION TABLE

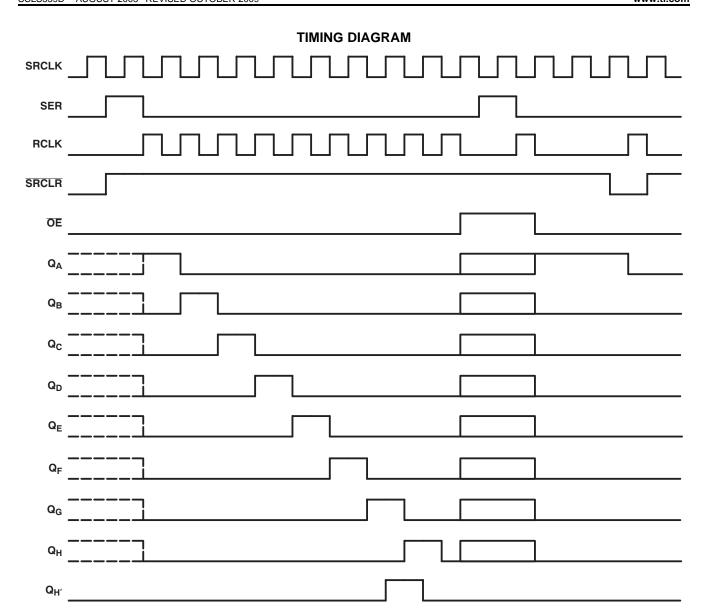
		INPUTS			FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	FUNCTION
Х	Х	Х	Х	Н	Outputs Q _A -Q _H are disabled.
X	X	Χ	Χ	L	Outputs Q _A -Q _H are enabled.
X	Χ	L	Χ	Χ	Shift register is cleared.
L	↑	Н	X	Х	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
Н	↑	Н	Х	Х	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
Х	Χ	Х	↑	Х	Shift-register data is stored in the storage register.



LOGIC DIAGRAM (POSITIVE LOGIC)









ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

JVCIO	perating nee an temperature range (anicss o	therwise noted)	
V_{CC}	Supply voltage range		−0.5 V to 7 V
V _I	Input voltage range (2)		-0.5 V to 7 V
Vo	Voltage range applied to any output in the high-in	mpedance or power-off state ⁽²⁾	-0.5 V to 7 V
Vo	Output voltage range applied in the high or low s	state ⁽²⁾ (3)	-0.5 V to V _{CC} + 0.5 V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0	–20 mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0	–50 mA
l _o	Continuous output current	$V_O = 0$ to V_{CC}	±35 mA
	Continuous current through V _{CC} or GND		±70 mA
θ_{JA}	Package thermal impedance (4)		108°C/W
T _{stg}	Storage temperature range		-65°C to 150°C
		Human-body model (HBM)	2000 V
ESD	Electrostatic discharge rating	Machine model (MM)	200 V
		Charged-device model (CDM)	1000 V

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V	Lligh level input veltage	V _{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		V
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V
		V _{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
		V _{CC} = 2 V		0.5	
\/	Low level input valtage	V _{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	V
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	V
		V _{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
VI	Input voltage		0	5.5	V
.,	Output valtage	High or low state	0	V _{CC}	V
Vo	Output voltage	3-state	0	5.5	V
		V _{CC} = 2 V		-50	μA
	High lavel autout average	V _{CC} = 2.3 V to 2.7 V		-2	
I _{OH}	High level output current	V _{CC} = 3 V to 3.6 V		-8	mA
		V _{CC} = 4.5 V to 5.5 V		-16	
		V _{CC} = 2 V		50	μA
	Low lovel output ourrent	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2	
l _{OL}	Low level output current	V _{CC} = 3 V to 3.6 V		8	mA
		V _{CC} = 4.5 V to 5.5 V		16	
		V _{CC} = 2.3 V to 2.7 V		200	
Δt/Δν	Input transition rise/fall time	V _{CC} = 3 V to 3.6 V		100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20	
_	On another fine a sin to make a section.	SN74LV595AIPWRQ1	-40	85	°C
T_A	Operating free-air temperature	SN74LV595AQPWRQ1	-40	125	-0

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ This value is limited to 5.5 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

Б.	DAMETED	TEST CONDITIONS	V	T _A = -40°	°C TO 85	°C	T _A = -40°	C TO 12	5°C	LINUT
PA	RAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			
		$I_{OH} = -2 \text{ mA}$	2.3 V	2			2			
\/	$Q_{H'}$	$I_{OH} = -6 \text{ mA}$	3 V	2.48			2.45			V
V_{OH}	Q _A -Q _H	I _{OH} = −8 mA	3 V	2.48			2.45			V
	Q _H ′	I _{OH} = −12 mA	4.5 V	3.8			3.7			
	Q _A -Q _H	I _{OH} = −16 mA	4.5 V	3.8			3.7			
		I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	
		$I_{OH} = 2 \text{ mA}$	2.3 V			0.4			0.45	
\/	Q _H ′	I _{OH} = 6 mA	3 V			0.44			0.5	V
V_{OL}	Q _A -Q _H	I _{OH} = 8 mA	3 V			0.44			0.5	V
	$Q_{H'}$	I _{OH} = 12 mA	4.5 V			0.55			0.65	
	Q_A – Q_H	I _{OH} = 16 mA	4.5 V			0.55			0.65	
I _I		$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V			±1			±1	nΑ
l _{OZ}	Q _A -Q _H	$V_O = V_{CC}$ or GND	5.5 V			±5			±10	μA
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			40	μΑ
I _{off}		V_I or $V_O = 0$ to 5.5 V	0			5 ⁽¹⁾			10	μA
Ci		$V_I = V_{CC}$ or GND	3.3 V		3.5			3.5		pF

⁽¹⁾ I_{off} does not apply to pin 9.



TIMING REQUIREMENTS

over operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

		-	T _A = 2	25°C	T _A = - TO 8		T _A = - TO 12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
		SRCLK high or low	7		7.5		8.5		
t _w	Pulse duration	RCLK high or low	7		7.5		8.5		ns
		SRCLR low	6		6.5		7.5		
		SER before SRCLK↑	5.5		5.5		6.5		
	Setup time	SRCLK↑ before RCLK↑ ⁽¹⁾	8		9		10		no
t _{su}	Setup time	SRCLR low before RCLK↑	8.5		9.5		10.5		ns
		SRCLR high (inactive) before SRCLK↑	4		4		5		
t _h	Hold time	SER after SRCLK↑	1.5		1.5		2.5		ns

⁽¹⁾ This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

TIMING REQUIREMENTS

over operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

			T _A = 2	25°C	T _A = - TO 8		T _A = - TO 12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
		SRCLK high or low	5.5		5.5		6.5		
t _w	Pulse duration	RCLK high or low	5.5		5.5		6.5		ns
		SRCLR low	5		5		6		
		SER before SRCLK↑	3.5		3.5		4.5		
	Catua tima	SRCLK↑ before RCLK↑ ⁽¹⁾	8		8.5		9.5		
t _{su}	Setup time	SRCLR low before RCLK↑	8		9		10		ns
		SRCLR high (inactive) before SRCLK↑	3		3		4		
t _h	Hold time	SER after SRCLK↑	1.5		1.5		2.5		ns

⁽¹⁾ This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

TIMING REQUIREMENTS

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T _A = 2	25°C	T _A = - TO 8		T _A = - TO 12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
		SRCLK high or low	5		5		6		
t _w	Pulse duration	RCLK high or low	5		5		6		ns
		SRCLR low	5.2		5.2		6.2		
		SER before SRCLK↑	3		3		4		
	Catur time	SRCLK↑ before RCLK↑ ⁽¹⁾	5		5		6		20
t _{su}	Setup time	SRCLR low before RCLK↑	5		5		6		ns
		SRCLR high (inactive) before SRCLK↑	2.5		2.5		3.5		
t _h	Hold time	SER after SRCLK↑	2		2		3		ns

⁽¹⁾ This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	Т,	₄ = 25°C	;	T _A = - TO 8		T _A = - TO 12		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			60	70		40		30		MHz
t _{PLH}	RCLK	0 -0		11.2	17.2	1	19.3	1	22.3	ns
t _{PHL}	KOLK	Q _A -Q _H		11.2	17.2	1	19.3	1	22.3	ns
t _{PLH}	SRCLK	0		13.1	22.5	1	25.5	1	28.5	ns
t _{PHL}	SKOLK	Q _H '		13.1	22.5	1	25.5	1	28.5	ns
t _{PHL}	SRCLR	Q _H '		12.4	18.8	1	21.1	1	24.1	ns
t _{PZH}	ŌĒ	Q _A -Q _H		10.8	17	1	18.3	1	21.3	ns
t _{PZL}	OE	$Q_A - Q_H$		13.4	21	1	23	1	26	ns
t _{PHZ}	ŌĒ	0 -0		12.2	18.3	1	19.5	1	22.5	ns
t _{PLZ}	OE	Q _A -Q _H		14	20.9	1	22.6	1	25.6	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $C_{L} = 50 \text{ pF}$ (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	Т,	₄ = 25°C		T _A = - TO 8		T _A = - TO 12		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			55	105		50		40		MHz
t _{PLH}	RCLK	0 -0		7.9	15.4	1	17	1	20	ns
t _{PHL}	KCLK	Q _A -Q _H		7.9	15.4	1	17	1	20	ns
t _{PLH}	SRCLK	0		9.2	16.5	1	18.5	1	21.5	ns
t _{PHL}	SKULK	Q _H '		9.2	16.5	1	18.5	1	21.5	ns
t _{PHL}	SRCLR	Q _H '		9	16.3	1	17.2	1	20.2	ns
t _{PZH}	ŌĒ	0 -0		7.8	15	1	17	1	20	ns
t _{PZL}	OE	Q _A -Q _H		9.6	15	1	17	1	20	ns
t _{PHZ}	ŌĒ	0 -0		8.1	15.7	1	16.2	1	19.2	ns
t _{PLZ}	OE	Q _A -Q _H		9.3	15.7	1	16.2	1	19.2	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	Т,	λ = 25°C		T _A = -		T _A = - TO 12		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			95	140		85		75		MHz
t _{PLH}	RCLK	Q _A -Q _H		5.6	9.4	1	10.5	1	13.5	ns
t _{PHL}	KCLK	Q _A -Q _H		5.6	9.4	1	10.5	1	13.5	ns
t _{PLH}	SRCLK	$Q_{H'}$		6.4	10.2	1	11.4	1	14.4	ns
t _{PHL}	SKULK	QH'		6.4	10.2	1	11.4	1	14.4	ns
t _{PHL}	SRCLR	Q _H '		6.4	10	1	11.1	1	14.1	ns
t _{PZH}	OE	Q _A -Q _H		5.7	10.6	1	12	1	15	ns
t _{PZL}	OL	Q _A -Q _H		6.8	10.6	1	12	1	15	ns
t _{PHZ}	ŌĒ	Q _A -Q _H		3.5	10.3	1	11	1	14	ns
t _{PLZ}	OE .	Q _A −Q _H		3.4	10.3	1	11	1	14	ns

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NOISE CHARACTERISTICS(1)

 $V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$

	PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V _{OL}		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic V _{OL}		-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V _{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

⁽¹⁾ Characteristics are for surface-mount packages only.

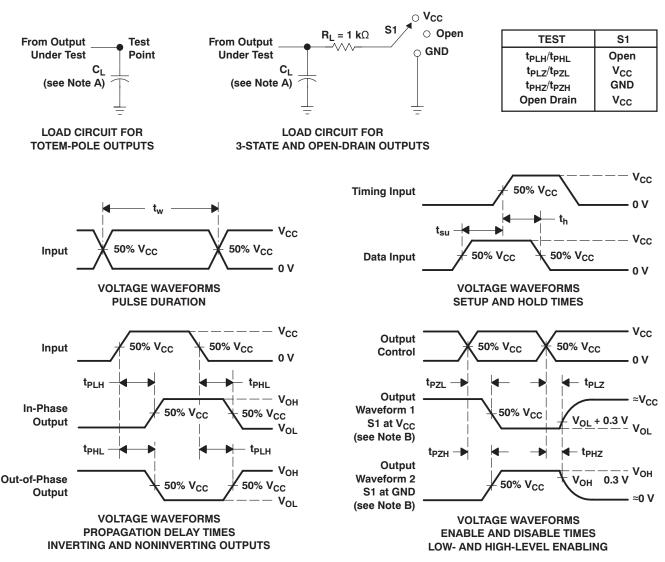
OPERATING CHARACTERISTICS

 $T_A = 25$ °C

	PARAMETER	TEST CONDITION	TYP	UNIT	
C _{pd}	Dower dissipation conscitance	C _ 50 pE f _ 10 MHz	$V_{CC} = 3.3 \text{ V}$	111	n.E
	Power dissipation capacitance	$C_L = 50 \text{ pF, f} = 10 \text{ MHz}$	V _{CC} = 5 V	114	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_0 = 50 \Omega$, $t_r \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status	Package Type	U	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
SN74LV595AIPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV595AI	Samples
SN74LV595AIPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LV595AI	Samples
SN74LV595AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV595AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV595A-Q1:

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.





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• Catalog: SN74LV595A

Enhanced Product: SN74LV595A-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 14-Mar-2013

TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV595AIPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV595AIPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV595AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

7 III GITTIOTIOTOTIO GITO TIOTITIGI								
Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LV595AIPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0	
SN74LV595AIPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0	
SN74LV595AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0	

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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