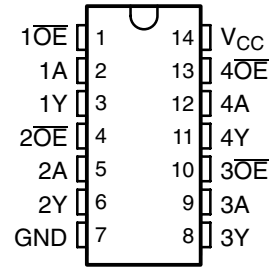


CD74HC125-Q1 HIGH-SPEED CMOS LOGIC QUAD BUFFER WITH 3-STATE OUTPUTS

SCLS579A – APRIL 2004 – REVISED SEPTEMBER 2008

- Qualified for Automotive Applications
- 3-State Outputs
- Separate Output Enable Inputs
- Fanout (Over Temperature Range)
 - Standard Outputs . . . 10 LSTTL Loads
 - Bus Driver Outputs . . . 15 LSTTL Loads
- Extended Temperature Performance of –40°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction, Compared to LSTTL Logic ICs
- 2-V to 6-V V_{CC} Operation
- High Noise Immunity N_{IL} or $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{ V}$

M OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC125 contains four independent 3-state buffers, each having its own output enable input which, when HIGH, puts the output in the high-impedance state.

ORDERING INFORMATION[†]

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Reel of 2500	CD74HC125QM96Q1	HC125Q
	TSSOP – PW	Reel of 2000	CD74HC125QPWRQ1	HC125Q

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	\overline{OE}	Y
H	L	H
L	L	L
X	H	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



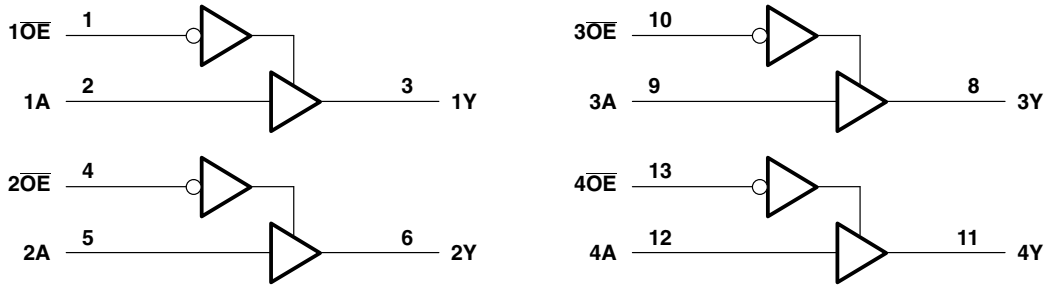
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CD74HC125-Q1
HIGH-SPEED CMOS LOGIC
QUAD BUFFER WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V)	± 35 mA
Output source or sink current per output pin, I_O ($V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V)	± 25 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): M package	86°C/W
..... PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
t_t	Input transition rise/fall time	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
T_A	Operating free-air temperature	-40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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HIGH-SPEED CMOS LOGIC
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I _O (mA)	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V _{OH}	V _I = V _{IH} or V _{IL}	CMOS loads	-0.02	2 V	1.9			1.9		V
			-0.02	4.5 V	4.4			4.4		
			-0.02	6 V	5.9			5.9		
		TTL loads	-6	4.5 V	3.98			3.7		
			-7.8	6 V	5.48			5.2		
V _{OL}	V _I = V _{IH} or V _{IL}	CMOS loads	0.02	2 V				0.1	0.1	V
			0.02	4.5 V				0.1	0.1	
			0.02	6 V				0.1	0.1	
		TTL loads	6	4.5 V				0.26	0.4	
			7.8	6 V				0.26	0.4	
I _I	V _I = V _{CC} or GND			6 V				±0.1	±1	μA
I _{CC}	V _I = V _{CC} or GND		0	6 V				8	160	μA
I _{OZ}	V _I = V _{IL} or V _{IH}			6 V				±0.5	±10	μA
C _I								10	10	pF
C _O	3-state							20	20	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t _{pd}	A	Y	C _L = 15 pF	5 V	8					ns
				2 V				100	150	
			C _L = 50 pF	4.5 V				20	30	
				6 V				17	26	
t _{en}	OE	Y	C _L = 15 pF	5 V	10					ns
				2 V				125	190	
			C _L = 50 pF	4.5 V				25	38	
				6 V				21	32	
t _{dis}	OE	Y	C _L = 15 pF	5 V	10					ns
				2 V				125	190	
			C _L = 50 pF	4.5 V				25	38	
				6 V				21	32	
t _t		Y	C _L = 50 pF	2 V				60	90	ns
				4.5 V				12	18	
				6 V				10	15	



CD74HC125-Q1

HIGH-SPEED CMOS LOGIC

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operating characteristics, $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate (see Note 4)	No load	29	pF

NOTE 4: C_{pd} is used to determine the dynamic power consumption, per channel.

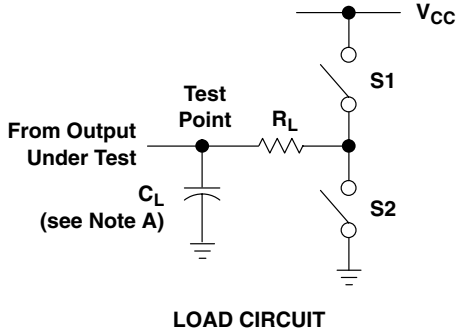
$$P_D = V_{CC}^2 f_i (C_{pd} + C_L)$$

f_i = input frequency

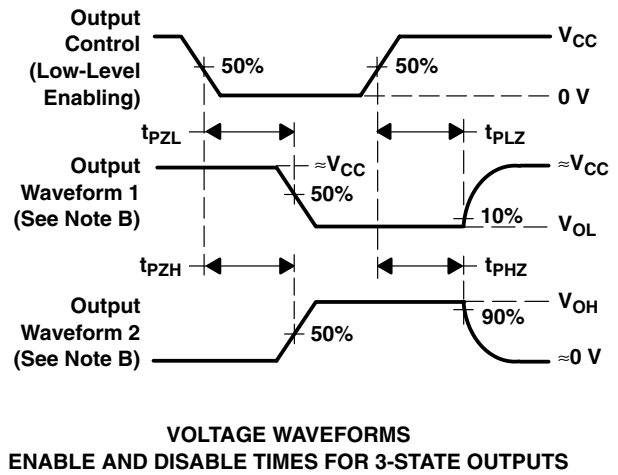
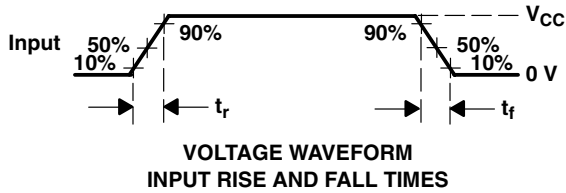
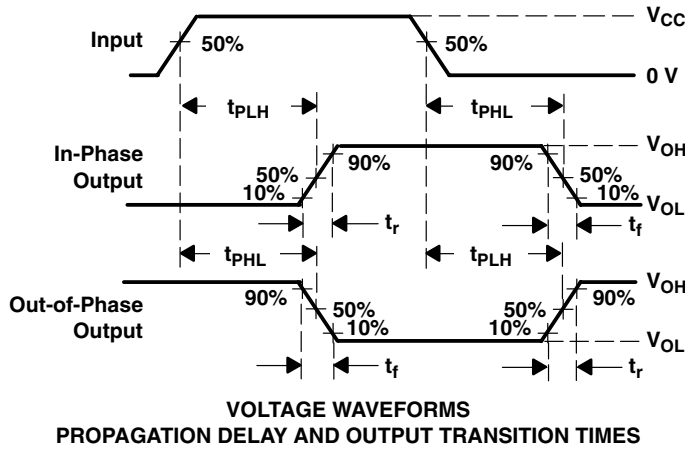
C_L = output load capacitance

V_{CC} = supply voltage

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2	
t_{en}	t_{pZH}	1 k Ω	50 pF	Open	Closed
	t_{pZL}	1 k Ω	50 pF	Closed	Open
t_{dis}	t_{pHZ}	1 k Ω	50 pF	Open	Closed
	t_{pLZ}	1 k Ω	50 pF	Closed	Open
t_{pd} or t_t	--	50 pF	Open	Open	



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - F. t_{pZL} and t_{pZH} are the same as t_{en} .
 - G. t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74HC125QM96G4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC125Q	Samples
CD74HC125QM96Q1	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	HC125Q	
CD74HC125QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC125Q	Samples
CD74HC125QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	HC125Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF CD74HC125-Q1 :

- Catalog: [CD74HC125](#)
- Military: [CD54HC125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC125QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC125QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC125QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
CD74HC125QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

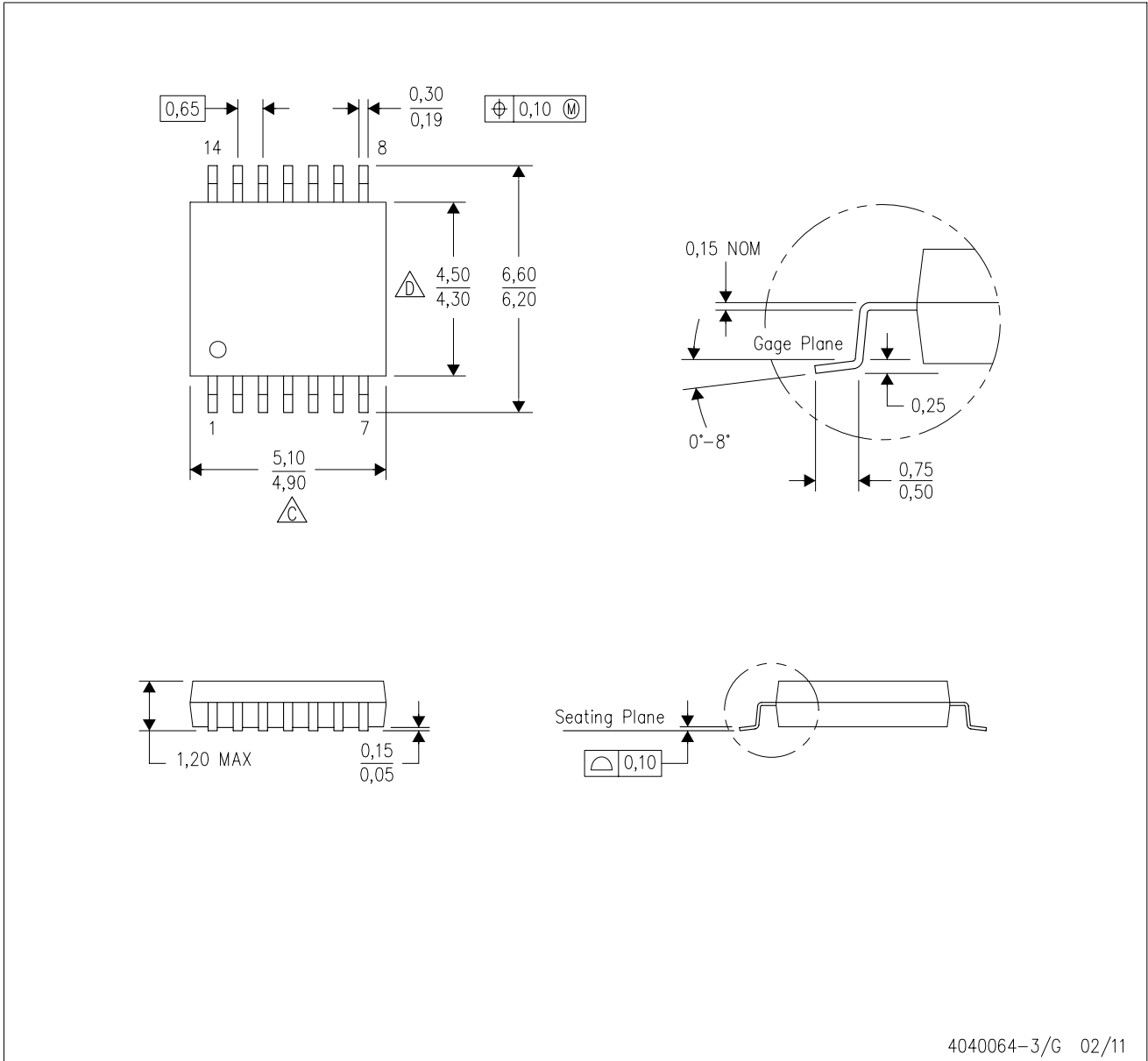
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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