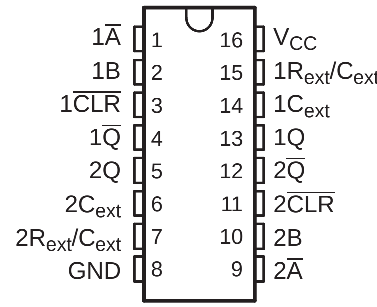
DUAL MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

Check for Samples: SN74LV221A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **2-V to 5.5-V V_{CC} Operation**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Transition Rates**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**

PW PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LV221A is a dual multivibrator designed for 2-V to 5.5-V V_{CC} operation. Each multivibrator has a negative-transition-triggered ($\overline{A}$) input and a positive-transition-triggered (B) input, either of which can be used as an inhibit input.

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext}(positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistor between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not related directly to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse duration can be varied by choosing the appropriate timing components. Output rise and fall times are TTL compatible and independent of pulse duration. Typical triggering and clearing sequences are illustrated in the input/output timing diagram.

The variance in output pulse duration from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the SN74LV221A-Q1 is shown in Figure 8. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 5.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Reel of 2000	SN74LV221AQPWRQ1	LV221AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Pin assignments are identical to those of the SN74AHC123A and SN74AHCT123A devices, so the SN74LV221A-Q1 can be substituted for those devices not using the retrigger feature.

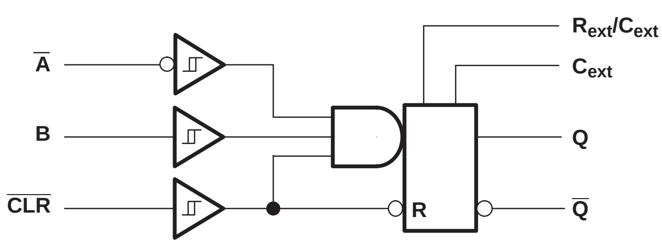
For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

FUNCTION TABLE
(EACH MULTIVIBRATOR)

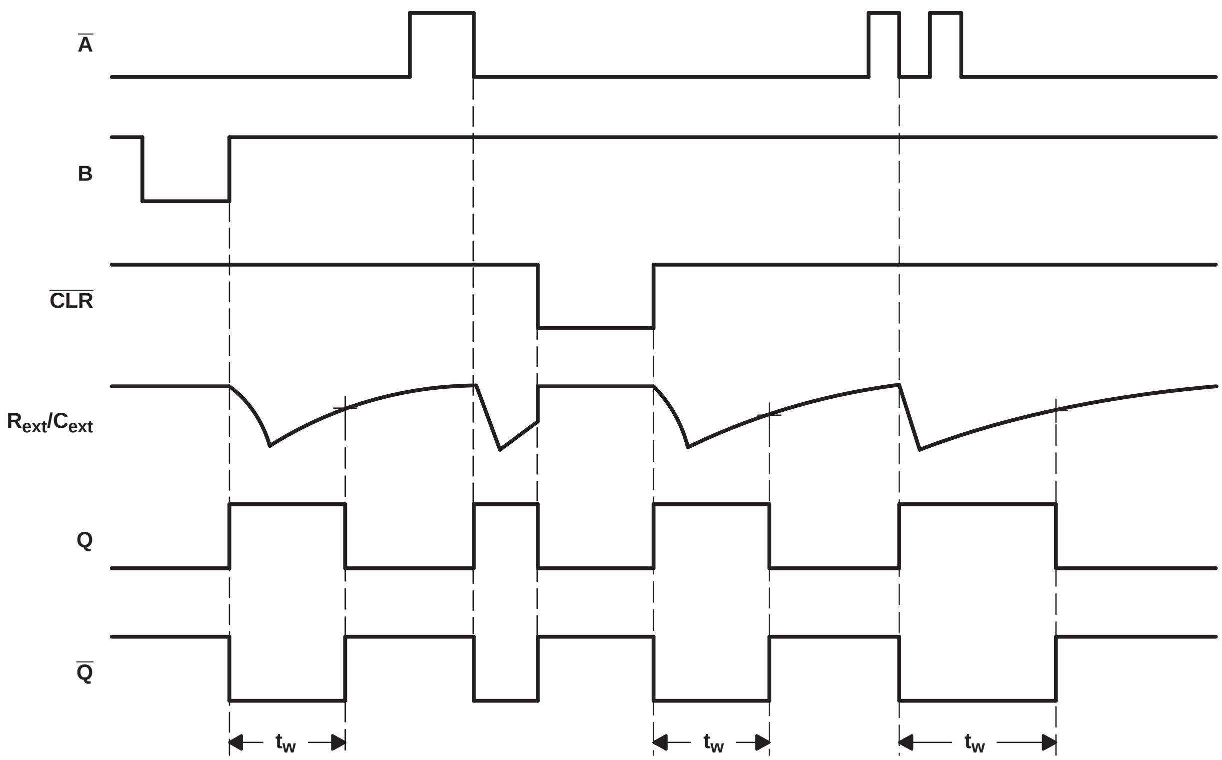
INPUTS			OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$	
L	X	X	L	H	Reset
H	H	X	L	H	Inhibit
H	X	L	L	H	Inhibit
H	L	↑	⎍	⎎	Outputs enabled
H	↓	H	⎍	⎎	Outputs enabled
↑(1)	L	H	⎍	⎎	Outputs enabled

(1) This condition is true only if the output of the latch formed by the NAND gate has been conditioned to the logic 1 state prior to $\overline{CLR}$ going high. This latch is conditioned by taking either $\overline{A}$ high or B low while $\overline{CLR}$ is inactive (high).

LOGIC DIAGRAM (POSITIVE LOGIC)



INPUT/OUTPUT TIMING DIAGRAM



Absolute Maximum Ratings[1]

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
V_O	Output voltage range in high or low state[2] [3]		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range in power-off state[2]		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
$θ_{JA}$	Package thermal impedance[4]			108	°C/W
	ESD rating[5]	Human-Body Model		2 (H2)	kV
		Charged-Device Model		1 (C5)	kV
		Machine Model		200 (M3)	V
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) ESD protection level per AEC Q100 classification

Recommended Operating Conditions[1]

			–40°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
R_{ext}	External timing resistance	V_{CC} = 2 V	5k		5k		Ω
		V_{CC} ≥ 3 V	1k		1k		
C_{ext}	External timing capacitance		No restriction		No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		1		1		ms/V
T_A	Operating free-air temperature		–40	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–40°C to 125°C MIN	–40°C to 125°C TYP	–40°C to 125°C MAX	–40°C to 85°C MIN	–40°C to 85°C TYP	–40°C to 85°C MAX	UNIT
V_{OH}		I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			2			
		I_{OH} = –6 mA	3 V	2.48			2.48			
		I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4	
		I_{OL} = 6 mA	3 V			0.44			0.44	
		I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	$\overline{A}$, B, and $\overline{CLR}$	V_I = 5.5 V or GND	0			±1			±1	µA
			0 to 5.5 V			±1			±1	
I_{CC}	Quiescent	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{CC}	Active state (per circuit)	V_I = V_{CC} or GND, R_{ext}/C_{ext} = 0.5 V_{CC}	3 V			280			280	µA
			4.5 V			650			650	
			5.5 V			975			975	
I_{off}		V_I or V_O = 0 to 5.5 V	0			10			5	µA
C_i		V_I = V_{CC} or GND	3.3 V		1.9			1.9		pF
			5 V		1.9			1.9		

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C MIN	T_A = 25°C MAX	–40°C to 125°C MIN	–40°C to 125°C MAX	–40°C to 85°C MIN	–40°C to 85°C MAX	UNIT
t_w	Pulse duration	$\overline{CLR}$	5		7		5		ns
		$\overline{A}$ or B trigger	5		7		5		

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C MIN	T_A = 25°C MAX	–40°C to 125°C MIN	–40°C to 125°C MAX	–40°C to 85°C MIN	–40°C to 85°C MAX	UNIT
t_w	Pulse duration	$\overline{CLR}$	5		7		5		ns
		$\overline{A}$ or B trigger	5		7		5		

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	–40°C to 125°C MIN	–40°C to 125°C MAX	–40°C to 85°C MIN	–40°C to 85°C MAX	UNIT
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		11.8	24.1	1	30.5	1	27.5	ns
	$\overline{CLR}$				10.6	19.3	1	25	1	22	
	$\overline{CLR}$ trigger				12.3	25.9	1	32.5	1	29.5	
t_w (1)		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		186	240		340		300	ns
			C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	90	100	110	85	115	90	110	μs
			C_L = 50 pF, C_{ext} = 0.1 pF, R_{ext} = 10 kΩ	0.9	1	1.1	0.85	1.15	0.9	1.1	ms
Δt_w (2)			C_L = 50 pF		±1						%

(1) t_w = Pulse duration at Q and $\overline{Q}$ outputs
(2) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	–40°C to 125°C MIN	–40°C to 125°C MAX	–40°C to 85°C MIN	–40°C to 85°C MAX	UNIT
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		8.2	14	1	19	1	16	ns
	$\overline{CLR}$				7.4	11.4	1	16	1	13	
	$\overline{CLR}$ trigger				8.6	14.9	1	20	1	17	
t_w (1)		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		171	200		280		240	ns
			C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	90	100	110	85	115	90	110	μs
			C_L = 50 pF, C_{ext} = 0.1 pF, R_{ext} = 10 kΩ	0.9	1	1.1	0.85	1.15	0.9	1.1	ms
Δt_w (2)			C_L = 50 pF		±1						%

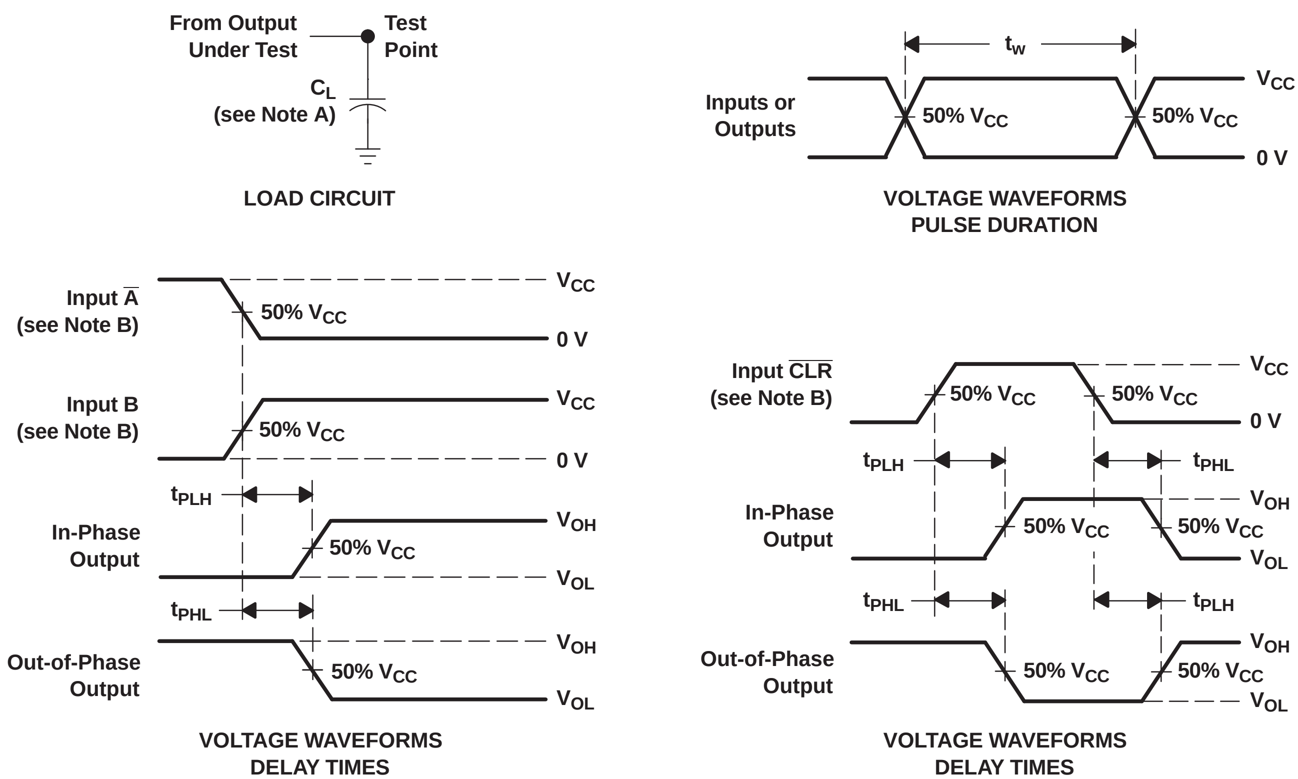
(1) t_w = Pulse duration at Q and $\overline{Q}$ outputs
(2) Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	50	pF
			5 V	51	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.

C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Caution in Use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

Power-Down Considerations

Large values of C_{ext} can cause problems when powering down the SN74LV221A-Q1 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if V_{CC} = 5 V and C_{ext} = 15 pF, the V_{CC} supply must turn off no faster than t = (5 V) × (15 pF)/30 mA = 2.5 ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the SN74LV221A-Q1 can sustain damage. To avoid this possibility, use external clamping diodes.

Output Pulse Duration

The output pulse duration, t_w, is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 2.

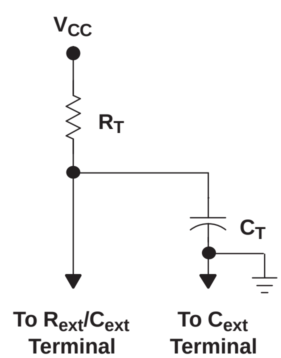


Figure 2. Timing-Component Connections

The pulse duration is given by:

$t_w = K \times R_T \times C_T$

if C_T is ≥ 1000 pF, K = 1.0

or

if C_T is < 1000 pF, K can be determined from Figure 7

where:

t_w = pulse duration in ns

R_T = external timing resistance in kΩ

C_T = external capacitancein pF

K = multiplier factor (1)

Equation 1 and Figure 3 or Figure 4 can be used to determine values for pulse duration, external resistance, and external capacitance.

APPLICATION INFORMATION

Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

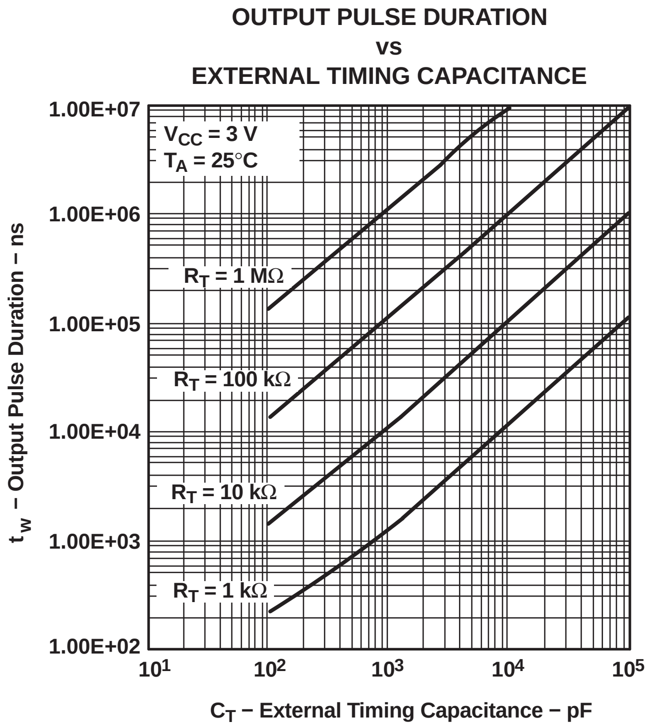


Figure 3.

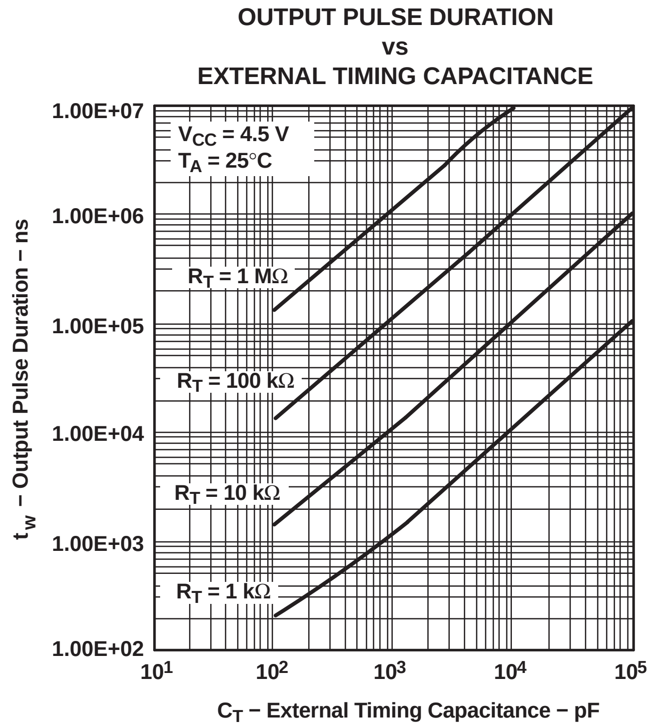


Figure 4.

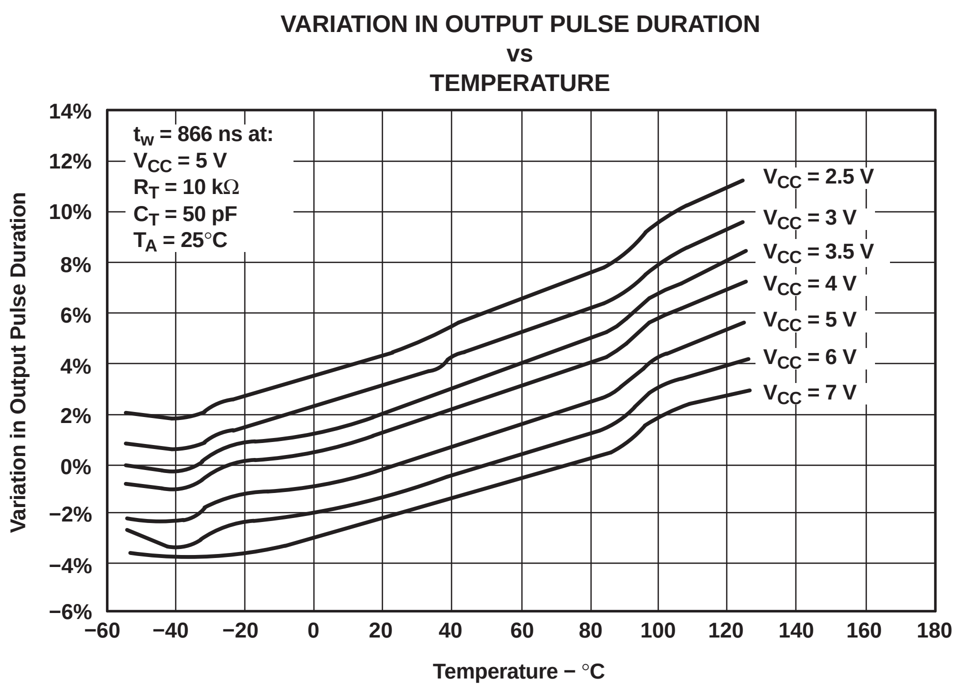


Figure 5.

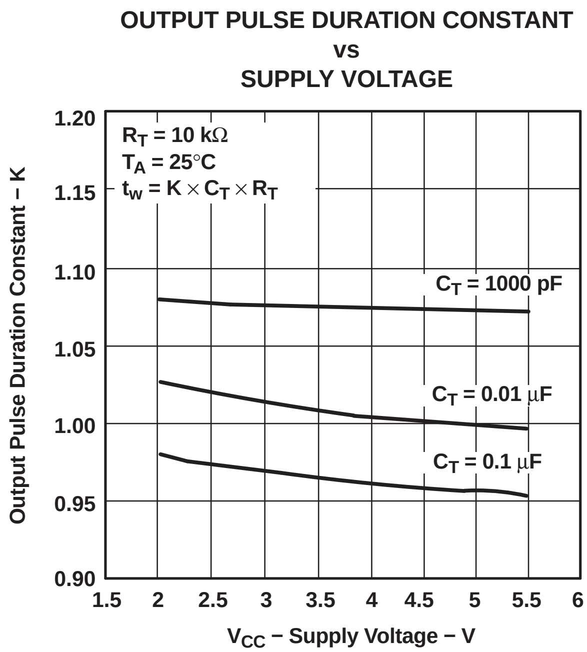


Figure 6.

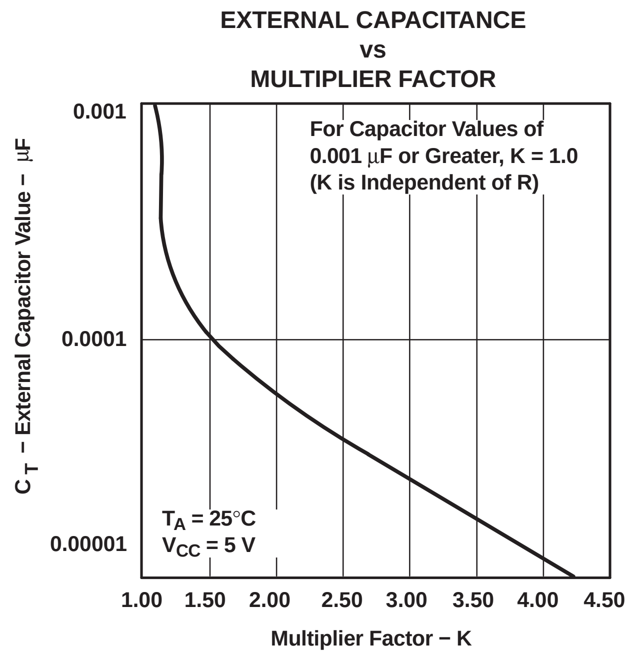


Figure 7.

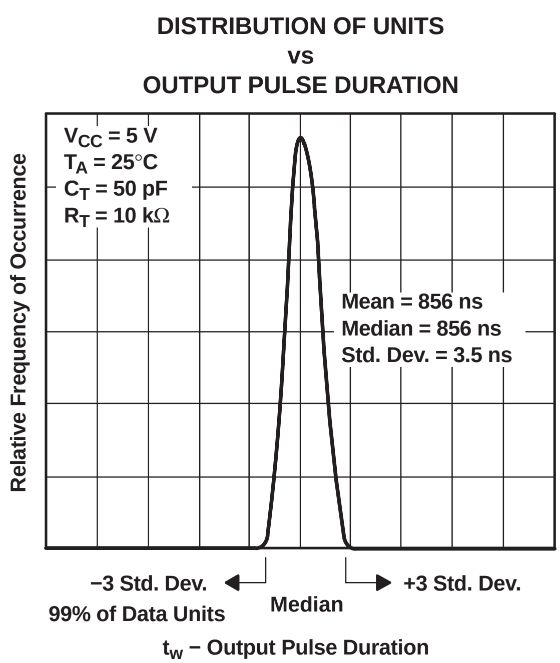


Figure 8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LV221AQPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV221AQ	Samples
SN74LV221AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	LV221AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74LV221A-Q1 :

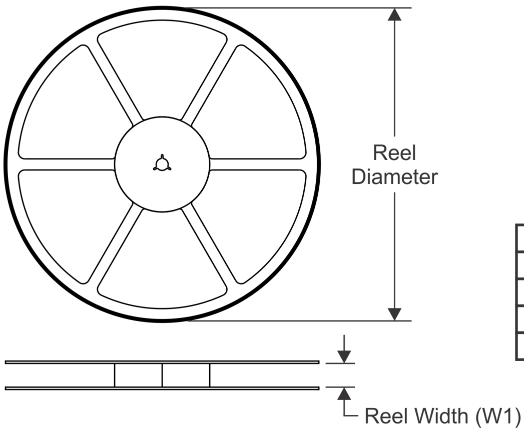
- Catalog: SN74LV221A

NOTE: Qualified Version Definitions:

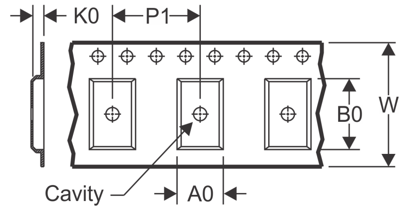
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

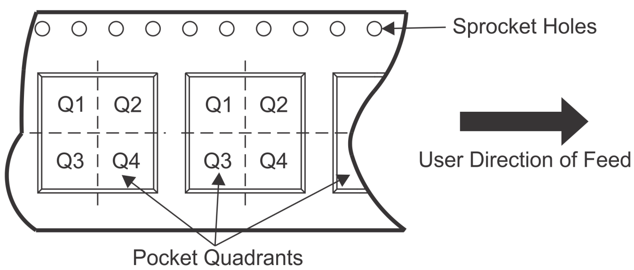


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

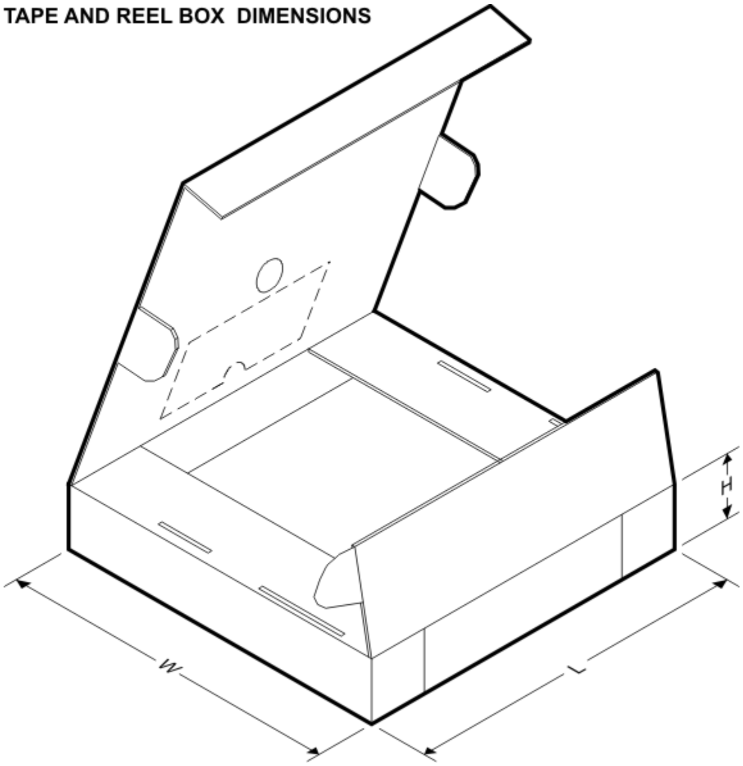
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV221AQPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV221AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

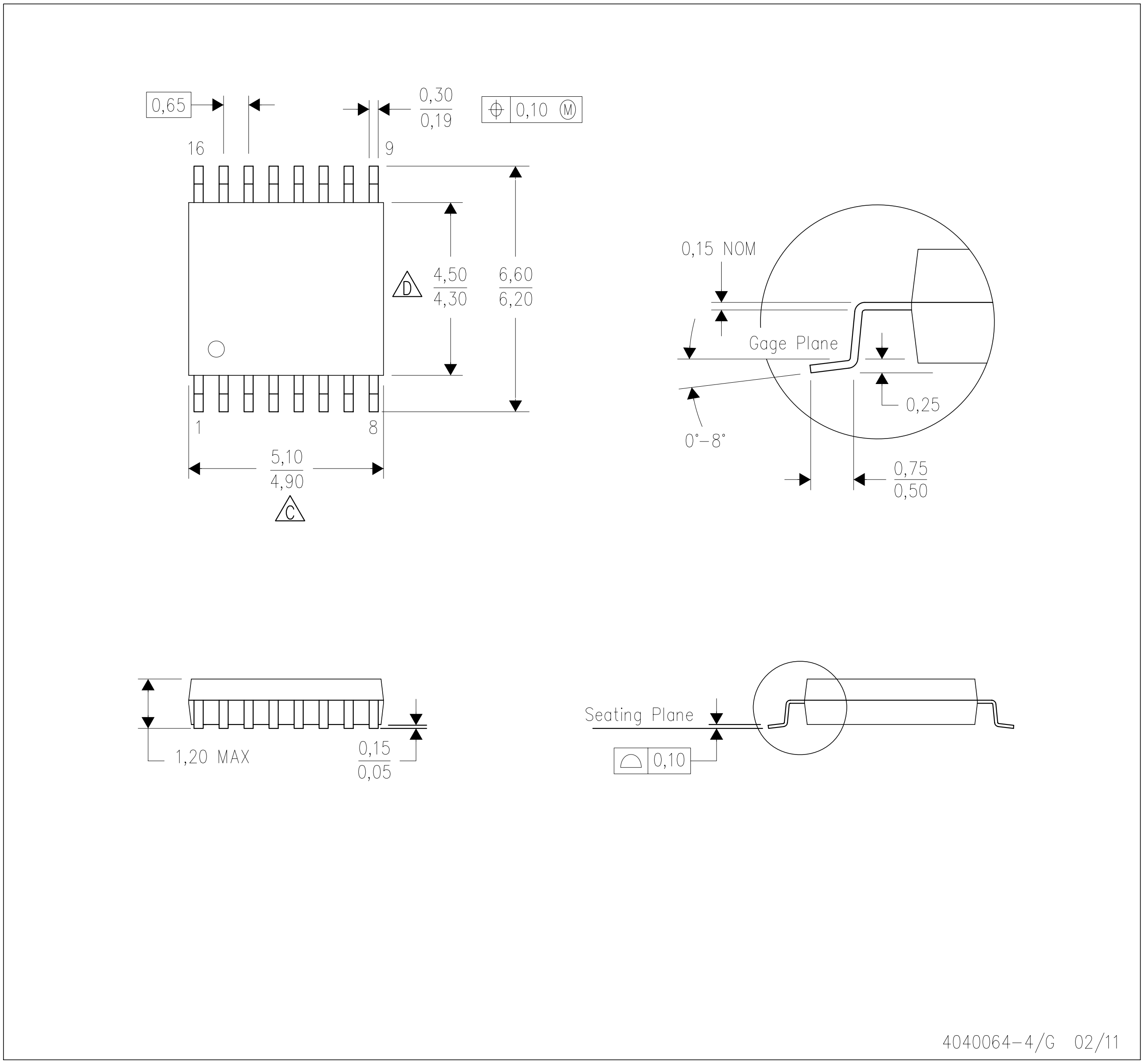
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV221AQPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV221AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

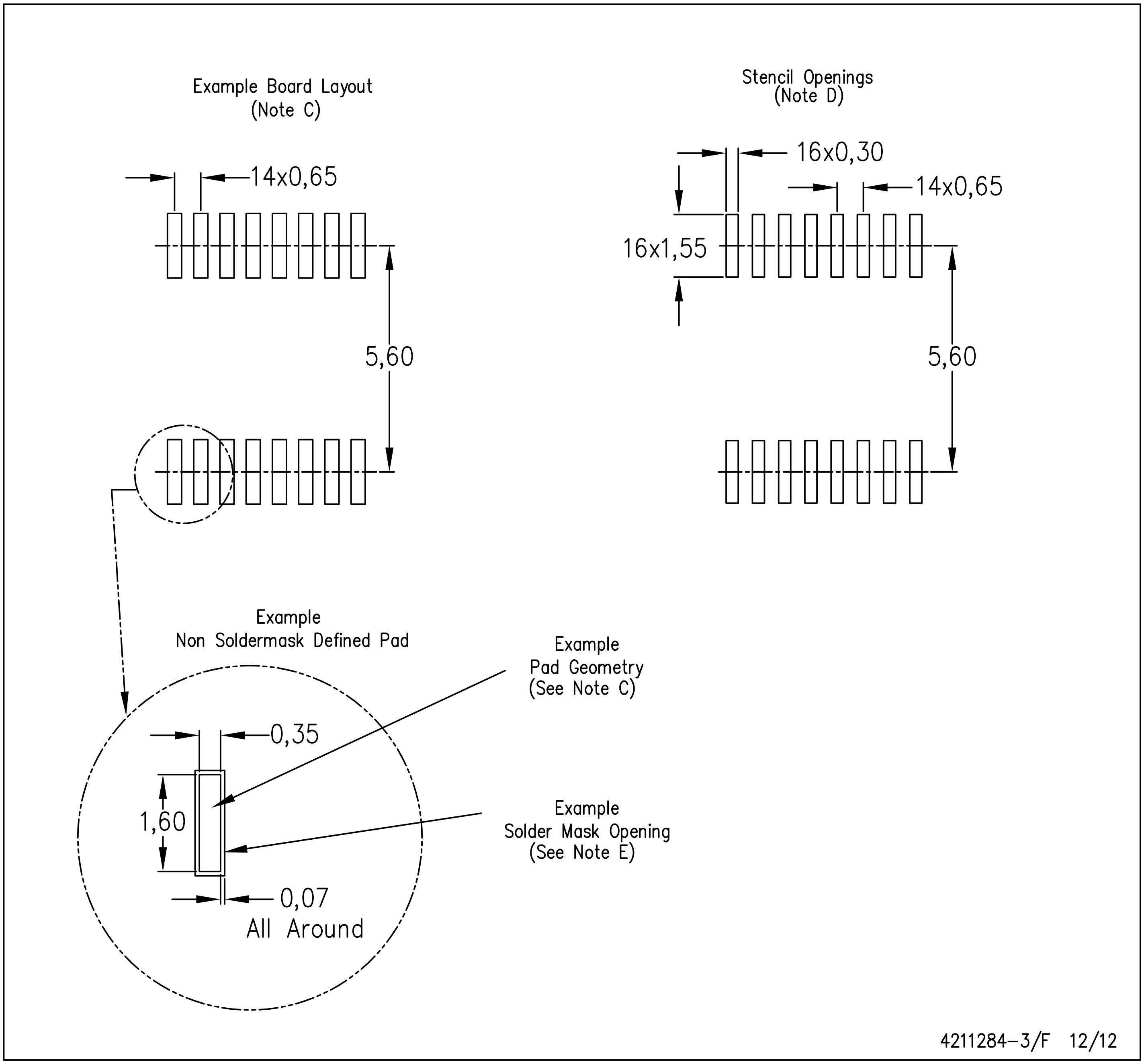
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO–153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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