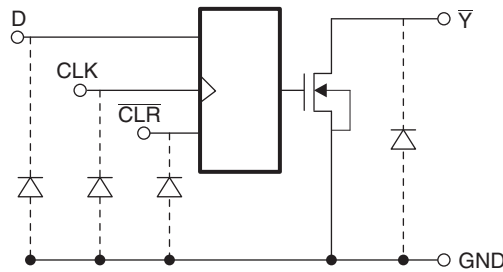


**FUNCTION TABLE
(EACH LATCH)⁽¹⁾**

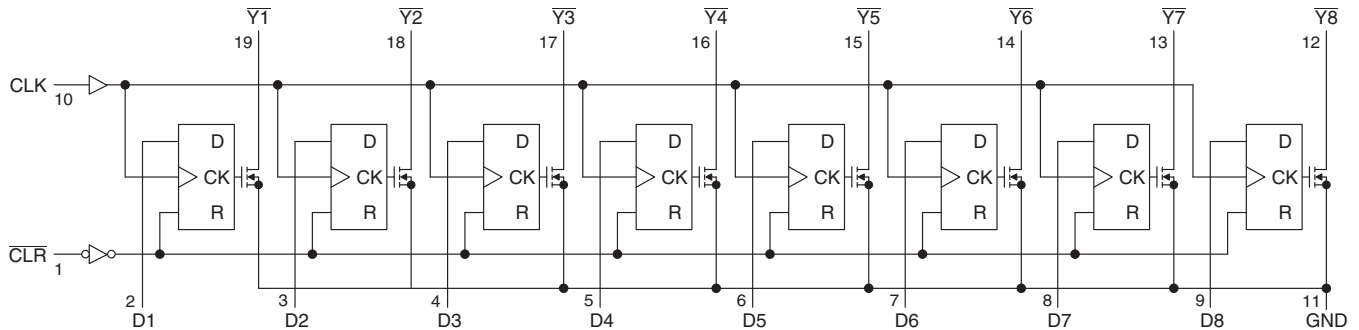
INPUTS			OUTPUT Y
CLR	CLK	D	
L	X	X	H*
H	↑	L	H*
H	↑	H	L
H	L	X	Y ₀
H	↓	X	Y ₀

- (1) L: Low-level
 H: High-level
 H*: with pullup resistor
 X: Irrelevant
 ↑: Rising edge
 ↓: Falling edge
 Z: High-impedance (OFF)

OUTPUT SCHEMATIC



LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
D	Input voltage range		-0.5	7	V
V_{ds}	Output voltage range	H output	-0.5	32	V
I_{ds}	Output current range	1 bit for output low,	$V_{CC} = 3\text{ V to }3.6\text{ V}$	100	mA
			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	200	
I_{IK}	Input clamp current	$V_I < 0\text{ V}$		-20	mA
θ_{JA}	Package thermal impedance ⁽²⁾	N package		69	°C/W
		PW package		83	
Operating free-air temperature range			-40	85	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage		3	5.5	V
V_{IH}	High-level input voltage		$V_{CC} \times 0.7$	V_{CC}	V
V_{IL}	Low-level input voltage		0	$V_{CC} \times 0.3$	V
V_{ds}	Output voltage			30	V
I_{ds}	Output current	N package, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	Duty cycle < 42%	200	mA
			Duty cycle < 100%	130	
		PW package, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	Duty cycle < 24%	200	
			Duty cycle < 100%	95	
T_A	Operating free-air temperature		-40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{T+}	Positive-going input threshold	D, $\overline{\text{CLR}}$, CLK			3.5	V	
V_{T-}	Negative-going input threshold	D, $\overline{\text{CLR}}$, CLK	1.5			V	
V_{HYS}	Hysteresis	D, $\overline{\text{CLR}}$, CLK	0.5		2	V	
I_{IH}	High-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$		0	1	μA	
I_{IL}	Low-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = 0\text{ V}$		0	-1	μA	
I_{OZ}	Leakage current	$V_{ds} = 30\text{ V}$			5	μA	
I_{off}	Leakage current	$V_I = 0\text{ to }5\text{ V}$, $V_O = 0\text{ to }30\text{ V}$, $V_{CC} = 0$		0	5	μA	
I_{CC}	Supply current	$V_I = 0\text{ to }5\text{ V}$, $V_O = 0\text{ to }30\text{ V}$, $V_{CC} = 0$	Output = all OFF		0	5	μA
			Output = all ON		0	5	
V_{OL}	Low-level output voltage	$V_{CC} = 4.5\text{ V}$, $I_O = 100\text{ mA}$		0.2	0.35	V	
		$V_{CC} = 4.5\text{ V}$, $I_O = 200\text{ mA}$		0.5	0.7	V	
r_{ON}	ON-state resistance	$V_{CC} = 4.5\text{ V}$, $I_O = 100\text{ mA}$		2	3.5	Ω	
C_i	Input capacitance	$V_I = V_{CC}$ or GND		5		pF	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted), see [Figure 1](#)

PARAMETER	TEST CONDITIONS	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to }85^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{TLH}	Output = low to high	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		180	230		260	ns
t_{THL}	Output = high to low	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		300	450		500	ns
t_{PLH}	Output = low to high	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		320	480		550	ns
t_{PHL}	Output = high to low	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		320	480		550	ns
t_{PHLR}	$\overline{\text{CLR}}-\bar{Y}$	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		320	480		550	ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, O/C to Y (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A = -40^\circ\text{C to }85^\circ\text{C}$		UNIT
			MIN	MAX	
t_{su}	Setup time	CLK \uparrow	$V_{DD} = 4.5\text{ V}$	10	ns
t_h	Hold time	CLK \uparrow	$V_{DD} = 4.5\text{ V}$	10	ns
t_w	Pulse width	CLK, $\overline{\text{CLR}}$	$V_{DD} = 4.5\text{ V}$	30	ns

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{T+}	Positive-going input threshold	D, $\overline{\text{CLR}}$, CLK			2.52	V	
V_{T-}	Negative-going input threshold	D, $\overline{\text{CLR}}$, CLK	0.9			V	
V_{HYS}	Hysteresis	D, $\overline{\text{CLR}}$, CLK	0.33		1.32	V	
I_{IH}	High-level input current	$V_{CC} = 3.6\text{ V}$, $V_I = 3.6\text{ V}$		0	1	μA	
I_{IL}	Low-level input current	$V_{CC} = 3.6\text{ V}$, $V_I = 0\text{ V}$		0	-1	μA	
I_{OZ}	Leakage current	$V_O = 30\text{ V}$			5	μA	
I_{off}	Leakage current	$V_{CC} = 0\text{ V}$, $V_I = 0\text{ to }3.6\text{ V}$, $V_O = 0\text{ to }30\text{ V}$		0	5	μA	
I_{CC}	Supply current	$V_{CC} = 3.6\text{ V}$, $V_I = 0\text{ to }3.6\text{ V}$, $V_O = 0\text{ to }30\text{ V}$	Output = all OFF		0	5	μA
			Output = all ON		0	5	
V_{OL}	Low-level output voltage	$V_{CC} = 3\text{ V}$, $I_O = 100\text{ mA}$		0.35	0.7	V	
r_{ON}	ON-state resistance	$V_{CC} = 4.5\text{ V}$, $I_O = 100\text{ mA}$		3.5	7	Ω	
C_i	Input capacitance	$V_I = V_{CC}\text{ or GND}$		5		pF	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted), see [Figure 1](#)

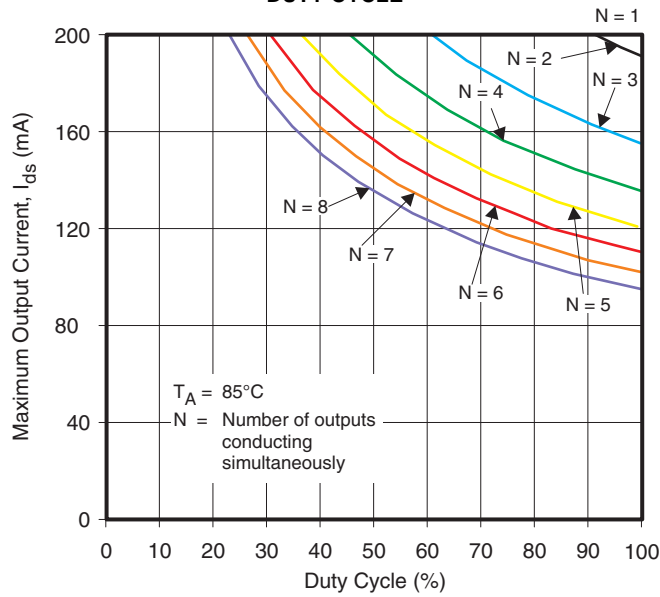
PARAMETER	TEST CONDITIONS	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to }85^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{TLH}	Output = low to high	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		300	450		500	ns
t_{THL}	Output = high to low	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		300	450		500	ns
t_{PLH}	Output = low to high	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		500	700		850	ns
t_{PHL}	Output = high to low	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		500	700		850	ns
t_{PHLR}	$\overline{\text{CLR}}-\bar{Y}$	$C_L = 30\text{ pF}$, $R_L = 240\ \Omega$, 24-V pullup		500	700		850	ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CC} = 3\text{ V to }3.6\text{ V}$, O/C to Y (unless otherwise noted)

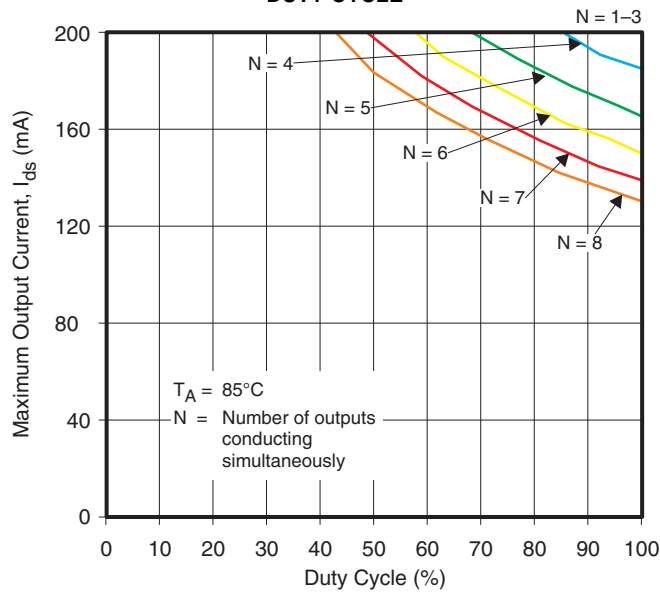
PARAMETER		TEST CONDITIONS	$T_A = -40^\circ\text{C to }85^\circ\text{C}$		UNIT
			MIN	MAX	
t_{su}	Setup time	CLK \uparrow	$V_{DD} = 3\text{ V}$	10	ns
t_h	Hold time	CLK \uparrow	$V_{DD} = 3\text{ V}$	10	ns
t_w	Pulse width	CLK, $\overline{\text{CLR}}$	$V_{DD} = 3\text{ V}$	30	ns

THERMAL INFORMATION
MAXIMUM OUTPUT CURRENT
vs
DUTY CYCLE

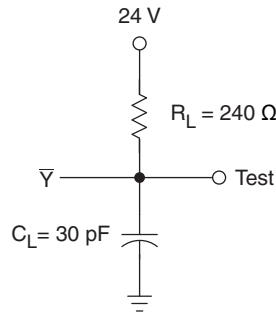


TSSOP (PW) PACKAGE

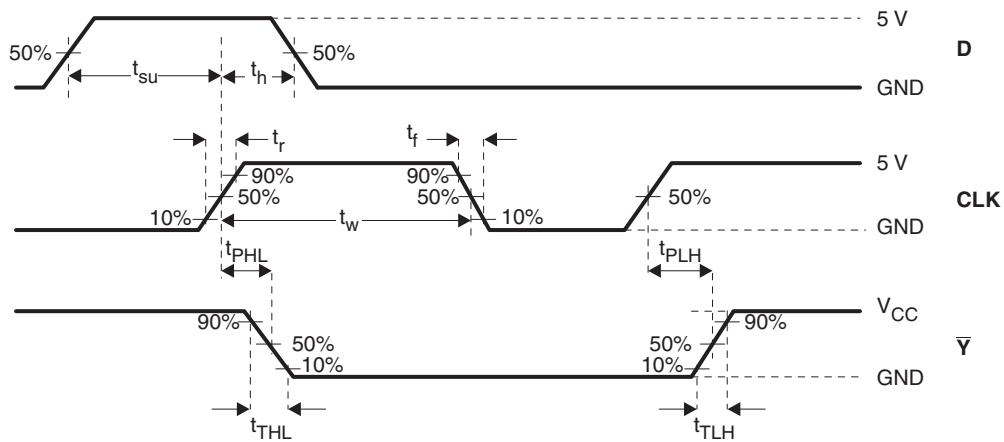
MAXIMUM OUTPUT CURRENT
vs
DUTY CYCLE



PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT
FOR O/D OUTPUT

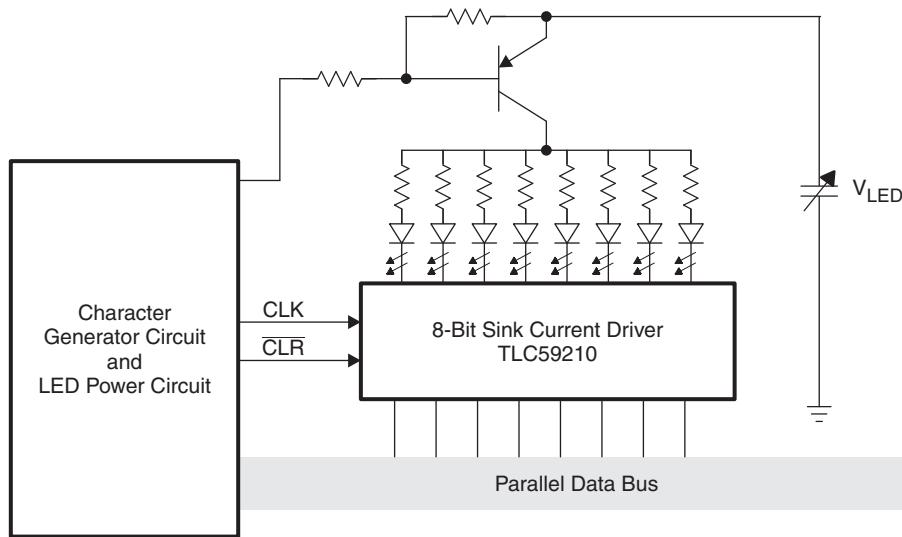


VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, and $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC59210IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC59210IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59210IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

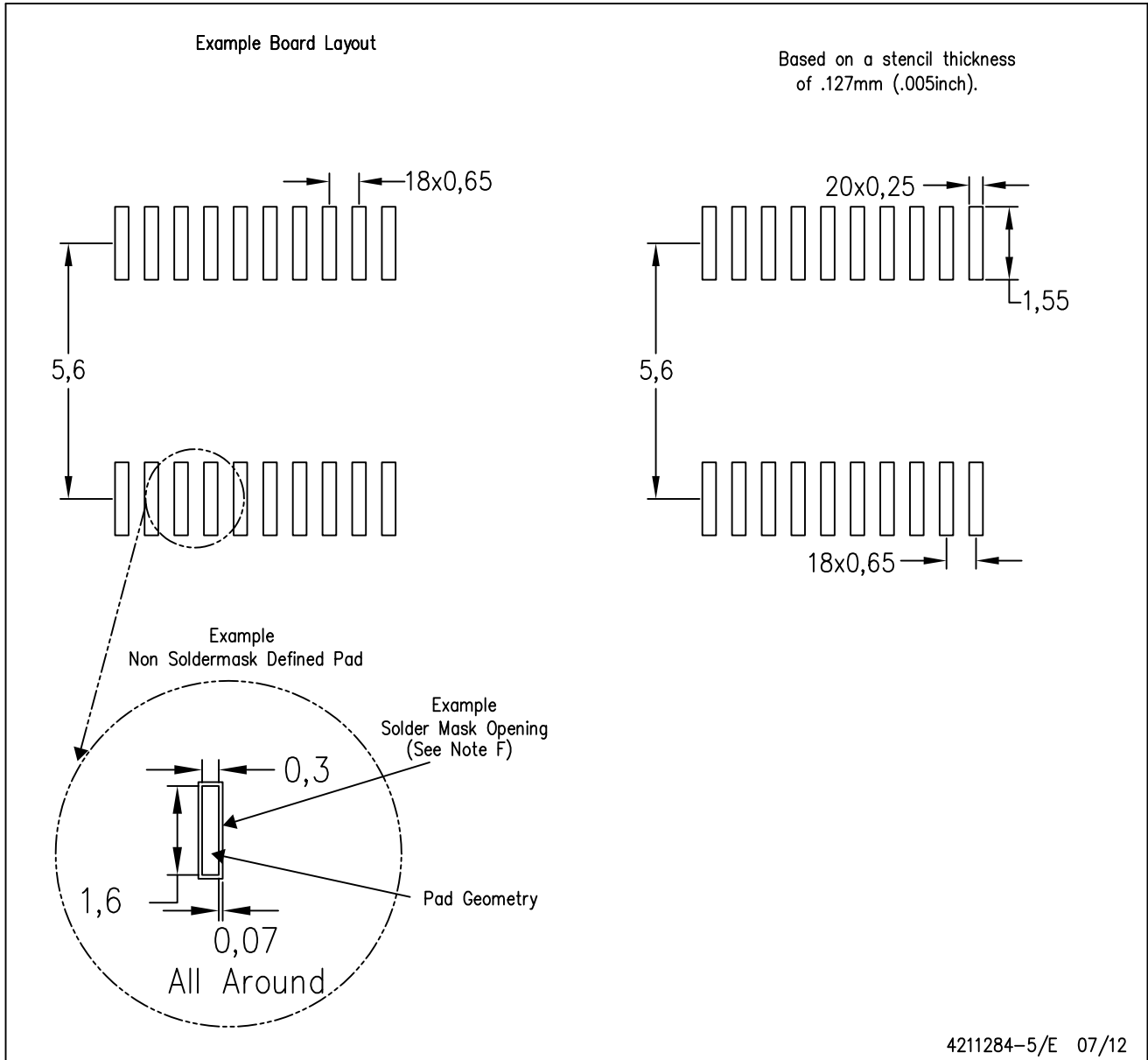


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59210IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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