

OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

 Check for Samples: [SN54HC373-DIE](#)

FEATURES

- Wide Operating Voltage Range
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption
- Typical $t_{pd} = 13$ ns
- Low Input Current
- Full Parallel Access for Loading

DESCRIPTION

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the SN54HC373-DIE are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
SN54HC373V	TD	Bare die in waffle pack ⁽²⁾	SN54HC373VTDG1	100
			SN54HC373VTDG2	10

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Processing is per the Texas Instruments space production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	AlCu(2%) TiW	1199 nm



Table 1. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
OE	1	143.1	693	243.9	793.8
1Q	2	143.1	303.3	243.9	404.1
1D	3	143.1	162.9	243.9	263.7
2D	4	593.1	162.9	693.9	263.7
2Q	5	1003.5	162.9	1104.3	263.7
3Q	6	1214.1	162.9	1314.9	263.7
3D	7	1692.9	162.9	1793.7	263.7
4D	8	2070.9	162.9	2171.7	263.7
4Q	9	2254.5	307.8	2355.3	408.6
GND	10	2254.5	473.4	2355.3	574.2
GND	11	2254.5	613.8	2355.3	714.6
LE	12	2254.5	831.6	2355.3	932.4
5Q	13	2254.5	1221.3	2355.3	1322.1
5D	14	2254.5	1361.7	2355.3	1462.5
6D	15	1804.5	1361.7	1905.3	1462.5
6Q	16	1394.1	1361.7	1494.9	1462.5
7Q	17	1183.5	1361.7	1284.3	1462.5
7D	18	704.7	1361.7	805.5	1462.5
8D	19	326.7	1361.7	427.5	1462.5
8Q	20	143.1	1216.8	243.9	1317.6
VCC	21	143.1	1051.2	243.9	1152
VCC	22	143.1	910.8	243.9	1011.6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54HC373VTDG1	ACTIVE			0	100	TBD	Call TI	N / A for Pkg Type			Samples
SN54HC373VTDG2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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