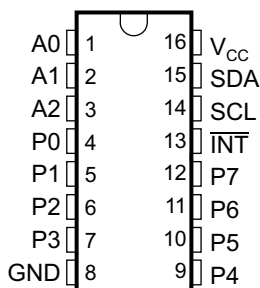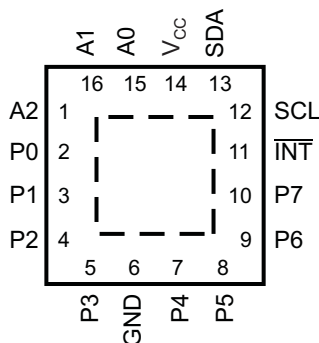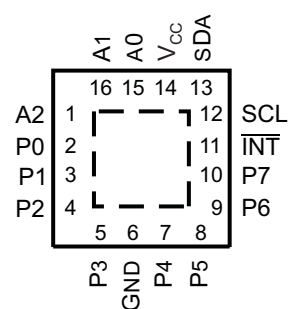# REMOTE 8-BIT I^{2}C AND SMBus LOW-POWER I/O EXPANDER
WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

Check for Samples: PCA9534A

FEATURES

- **Low Standby Current Consumption of 1 μA Max**
- **I^{2}C to Parallel Port Expander**
- **Open-Drain Active-Low Interrupt Output**
- **Operating Power-Supply Voltage Range of 2.3 V to 5.5 V**
- **5-V Tolerant I/O Ports**
- **400-kHz Fast I^{2}C Bus**
- **Three Hardware Address Pins Allow Up to Eight Devices on the I^{2}C/SMBus**
- **Allows Up to 16 Devices on the I^{2}C/SMBus When Used in Conjunction with the PCA9534 See Table 1 for I^{2}C Expander offerings**
- **Input/Output Configuration Register**

- **Polarity Inversion Register**
- **Internal Power-On Reset**
- **Power-Up With All Channels Configured as Inputs**
- **No Glitch on Power-Up**
- **Noise Filter on SCL/SDA Inputs**
- **Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

A0	1	16	V$_{CC}$
A1	2	15	SDA
A2	3	14	SCL
P0	4	13	INT
P1	5	12	P7
P2	6	11	P6
P3	7	10	P5
GND	8	9	P4

RGV PACKAGE
(TOP VIEW)

Top: A1 (16), A0 (15), V$_{CC}$ (14), SDA (13)
Left: A2 (1), P0 (2), P1 (3), P2 (4)
Right: SCL (12), INT (11), P7 (10), P6 (9)
Bottom: P3 (5), GND (6), P4 (7), P5 (8)

RGT PACKAGE
(TOP VIEW)

Top: A1 (16), A0 (15), V$_{CC}$ (14), SDA (13)
Left: A2 (1), P0 (2), P1 (3), P2 (4)
Right: SCL (12), INT (11), P7 (10), P6 (9)
Bottom: P3 (5), GND (6), P4 (7), P5 (8)

DESCRIPTION/ORDERING INFORMATION

This 8-bit I/O expander for the two-line bidirectional bus (I^{2}C) is designed for 2.3-V to 5.5-V V$_{CC}$ operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface [serial clock (SCL), serial data (SDA)].

The PCA9534A consists of one 8-bit configuration (input or output selection), input port, output port, and polarity inversion (active high or active low) register. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system master.

The system master can reset the PCA9534A in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I^{2}C/SMBus state machine.

The PCA9534A open-drain interrupt (INT) output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^{2}C bus. Thus, the PCA9534A can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs. It has low current consumption.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^{2}C address and allow up to eight devices to share the same I^{2}C bus or SMBus.

The PCA9534A is pin-to-pin and I^{2}C address compatible with the PCF8574A. However, software changes are required due to the enhancements in the PCA9534A over the PCF8574A.

The PCA9534A is a low-power version of the PCA9554A. The only difference between the PCA9534A and PCA9554A is that the PCA9534A eliminates an internal I/O pullup resistor, which dramatically reduces power consumption in the standby mode when the I/Os are held low.

The PCA9534A and PCA9534 are identical, except for their fixed I^{2}C address. This allows for up to 16 of these devices (8 of each) on the same I^{2}C bus.

ORDERING INFORMATION

T$_A$	PACKAGE[1] [2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGT	Reel of 3000	PCA9534ARGTR	ZVJ
	QFN – RGV	Reel of 2500	PCA9534ARGVR	PD534A
	QSOP – DBQ	Reel of 2500	PCA9534ADBQR	PDA534A
	SOIC – DW	Tube of 40	PCA9534ADW	PCA9534A
		Reel of 2000	PCA9534ADWR	
	SSOP – DB	Reel of 2000	PCA9534ADBR	PDA534A
		Tube of 80	PCA9534ADB	
	TSSOP – PW	Tube of 90	PCA9534APW	PD534A
		Reel of 2000	PCA9534APWR	
	TVSOP – DGV	Reel of 2000	PCA9534ADGVR	PD534A

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. I²C Expander offerings

DEVICE	MAX FREQUENCY	I²C ADDRESS	V_CC RANGE	NO. OF GPIOs	INTERRUPT OUTPUT	RESET INPUT	CONFIGURATION REGISTERS	5-V TOLERANT	PUSH-PULL I/O TYPE	OPEN-DRAIN I/O TYPE	COMMENT
TCA6408	400	0100 00x	1.65 to 5.5	8	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and t_r (ramp time) < 10 ms
TCA6408	400	0100 00x	1.65 to 5.5	8	Yes	Yes	Yes	Yes	Yes	No	Unrestricted power on reset ramp/fall time. Both t_f (fall time) and TRT (ramp time) can be between 0.1 ms and 2000 ms
TCA6416	400	0100 00x	1.65 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and TRT (ramp time) < 10 ms
TCA6416A	400	0100 00x	1.65 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	Unrestricted power on reset ramp/fall time. Both t_f (fall time) and TRT (ramp time) can be between 0.1 ms and 2000ms
TCA6424	400	0100 00x	1.65 to 5.5	24	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and TRT (ramp time) < 10 ms
TCA9535	400	0100 xxx	1.65 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
TCA9539	400	1110 1xx	1.65 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	
TCA9555	400	0100 xxx	1.65 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
PCA6107	400	0011 xxx	2.3 to 5.5	8	Yes	Yes	Yes	Yes	Yes P1—P7 bits	Yes P0 bit	One open drain output; eight push pull outputs
PCA9534	400	0100 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	PCA9534 has a different slave address as the PCA9534A, allowing up to 16 devices '9534 type devices on the same I²C bus
PCA9534A	400	0111 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	PCA9534A has a different slave address as the PCA9534, allowing up to 16 devices '9534 type devices on the same I²C bus
PCA9535	400	0100 xxx	2.3 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
PCA9536	400	1000 001	2.3 to 5.5	4	No	No	Yes	Yes	Yes	No	
PCA9538	400	1110 0xx	2.3 to 5.5	8	Yes	Yes	Yes	Yes	Yes	No	
PCA9539	400	1110 1xx	2.3 to 5.5	16	Yes	Yes	Yes	Yes	Yes	No	
PCA9554	400	0100 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	
PCA9554A	400	0111 xxx	2.3 to 5.5	8	Yes	No	Yes	Yes	Yes	No	
PCA9555	400	0100 xxx	2.3 to 5.5	16	Yes	No	Yes	Yes	Yes	No	
PCA9557	400	0011 xxx	2.3 to 5.5	8	No	Yes	Yes	Yes	Yes	Yes	
PCF8574	400	0100 xxx	2.5 to 6.0	8	Yes	No	No	Yes	Yes	No	PCA8574 has a different slave address as the PCA8574A, allowing up to 16 devices '9534 type devices on the same I²C bus
PCF8574A	400	0111 xxx	2.5 to 6.0	8	Yes	No	No	Yes	Yes	No	PCA8574A has a different slave address as the PCA8574, allowing up to 16 devices '9534 type devices on the same I²C bus
PCF8575	400	0100 xxx	2.5 to 5.5	16	Yes	No	No	Yes	Yes	No	
PCF8575C	400	0100 xxx	4.5 to 5.5	16	Yes	No	No	Yes	No	Yes	

Product Folder Link(s): *PCA9534A*

PCA9534A

Table 2. TERMINAL FUNCTIONS

QSOP (DBQ), SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT) AND QFN (RGV)	NAME	DESCRIPTION
1	15	A0	Address input. Connect directly to V_{CC} or ground.
2	16	A1	Address input. Connect directly to V_{CC} or ground.
3	1	A2	Address input. Connect directly to V_{CC} or ground.
4	2	P0	P-port input/output. Push-pull design structure.
5	3	P1	P-port input/output. Push-pull design structure.
6	4	P2	P-port input/output. Push-pull design structure.
7	5	P3	P-port input/output. Push-pull design structure.
8	6	GND	Ground
9	7	P4	P-port input/output. Push-pull design structure.
10	8	P5	P-port input/output. Push-pull design structure.
11	9	P6	P-port input/output. Push-pull design structure.
12	10	P7	P-port input/output. Push-pull design structure.
13	11	$\overline{INT}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
14	12	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
15	13	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
16	14	V_{CC}	Supply voltage

LOGIC DIAGRAM (POSITIVE LOGIC)
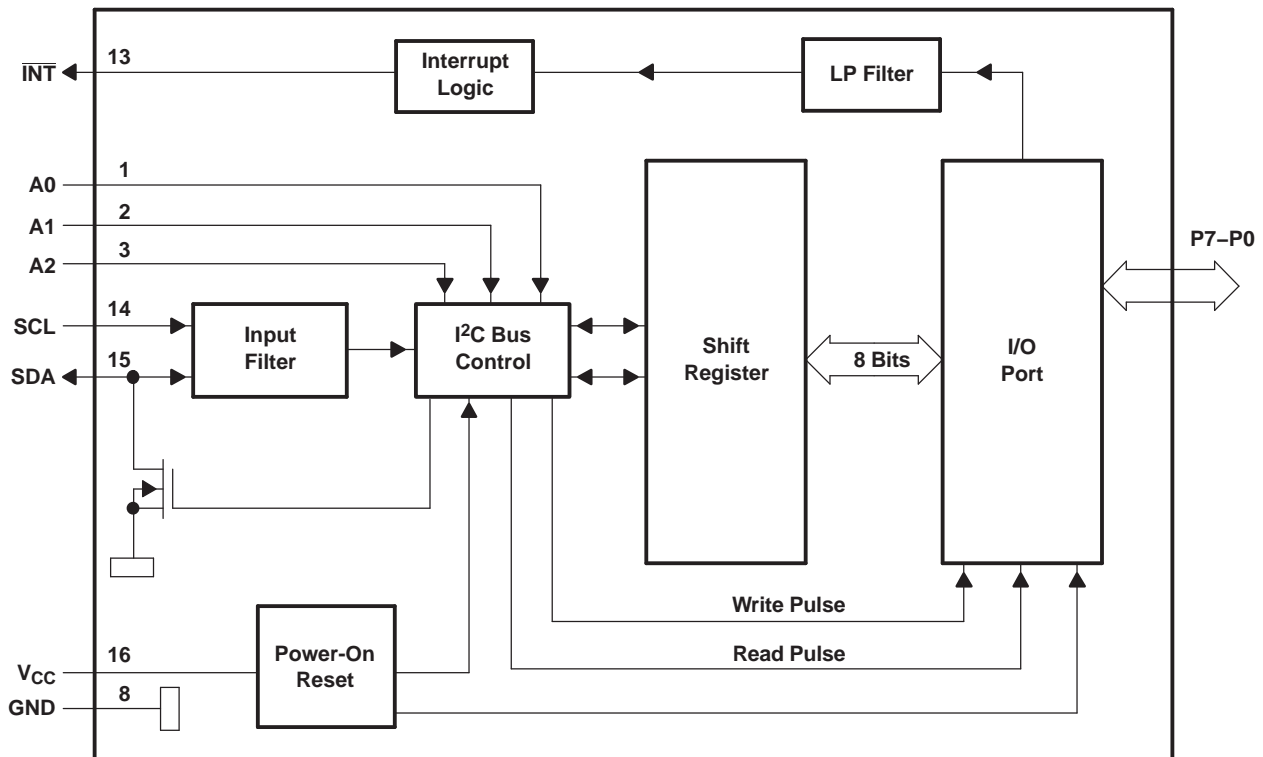
A. Pin numbers shown are for DB, DBQ, DGV, DW, or PW package.

B. All I/Os are set to inputs at reset.

Product Folder Link(s): *PCA9534A*

SIMPLIFIED SCHEMATIC OF P0 TO P7
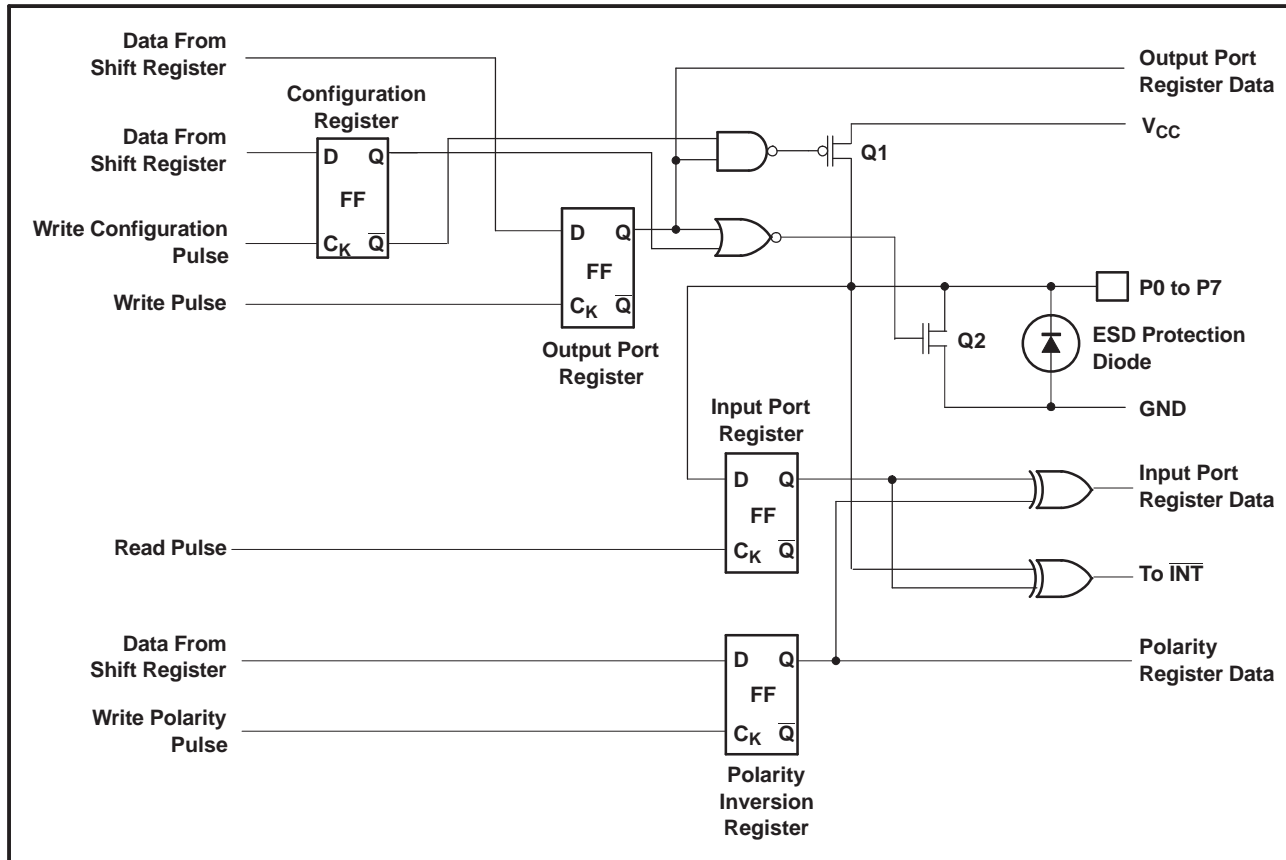
A.   At power-on reset, all registers return to default values.

I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 2).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.
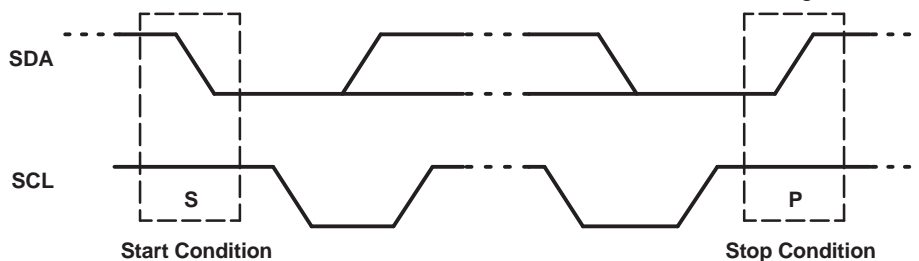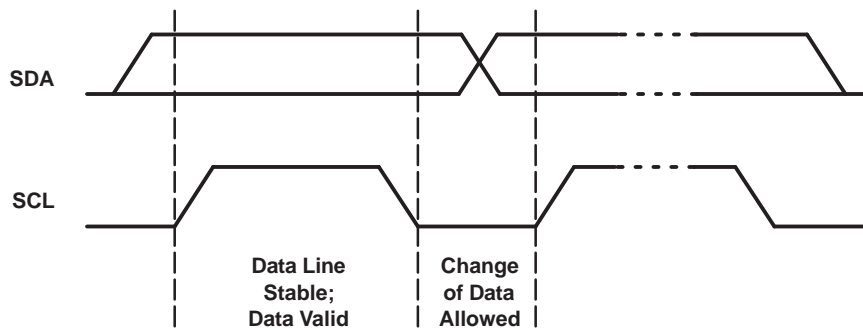

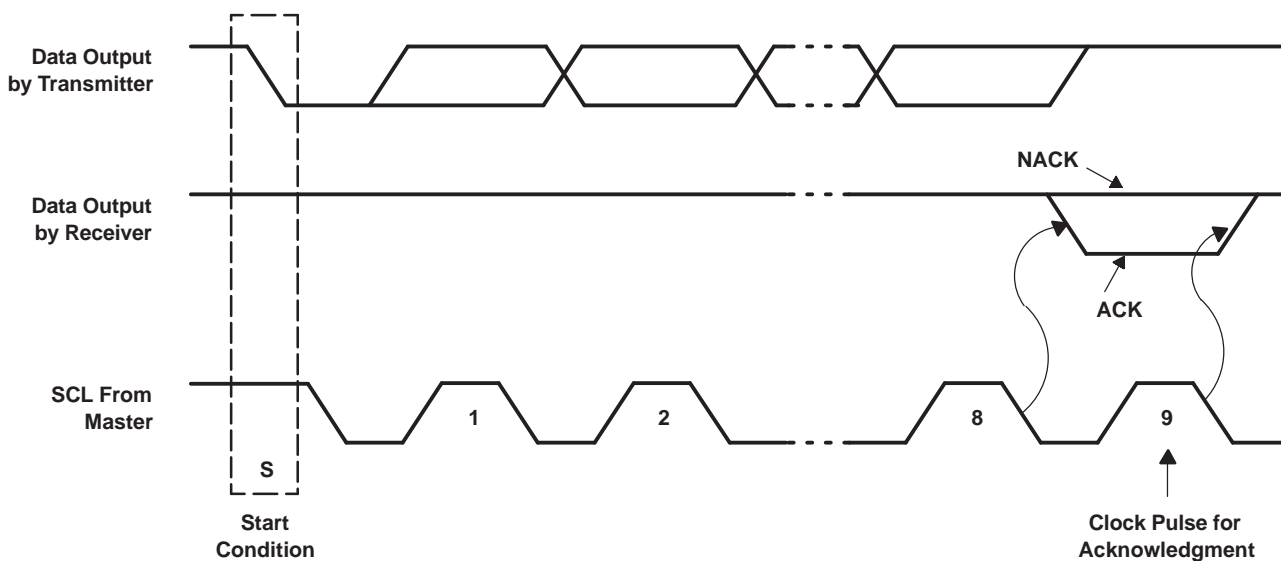Figure 1. Definition of Start and Stop Conditions

Figure 2. Bit Transfer

Figure 3. Acknowledgment on I²C Bus

Product Folder Link(s): PCA9534A

Table 3. Interface Definition

BYTE	BIT							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
I²C slave address	L	H	H	H	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

Device Address

Figure 4 shows the address byte of the PCA9534A.

Slave Address

0	1	1	1	A2	A1	A0	R/$\overline{W}$

Fixed   **Hardware Selectable**
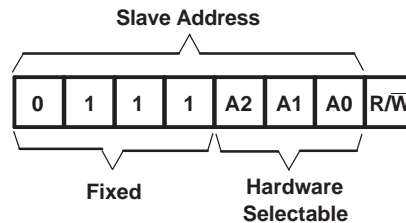
Figure 4. PCA9534A Address

Table 4. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	**A1**	**A0**	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte which is stored in the control register in the PCA9534A. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	0	B1	B0
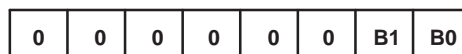
Figure 5. Control Register Bits

PCA9534A

Table 5. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	xxxx xxxx
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

Register Descriptions

The input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the input port register will be accessed next.

Table 6. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 7. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

Table 8. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 9. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9534A in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9534A registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Product Folder Link(s): *PCA9534A*

Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

Bus Transactions

Data is exchanged between the master and PCA9534A through write and read commands.

Writes

Data is transmitted to the PCA9534A by sending the device address and setting the least-significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 6 and Figure 7). There is no limitation on the number of data bytes sent in one write transmission.
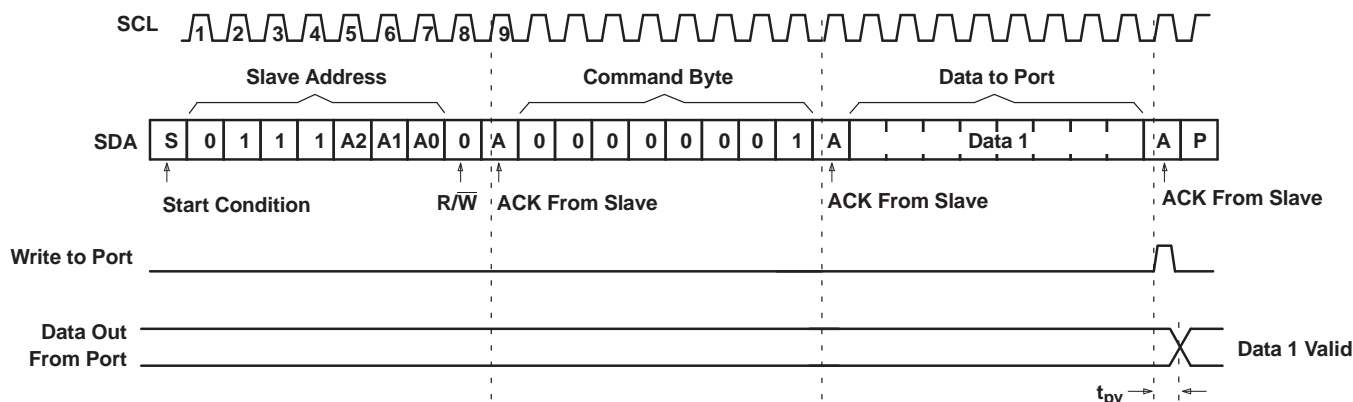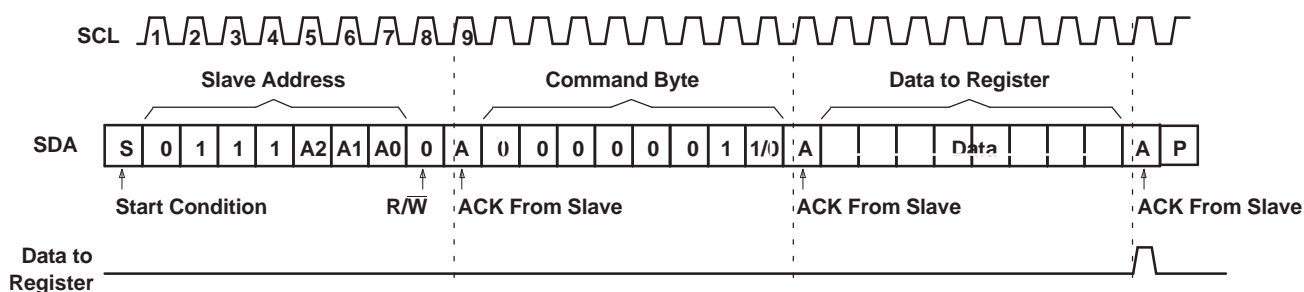

**Figure 6. Write to Output Port Register**

Figure 7. Write to Configuration or Polarity Inversion Registers

Reads

The bus master first must send the PCA9534A address with the least-significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9534A (see Figure 8 and Figure 9). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.
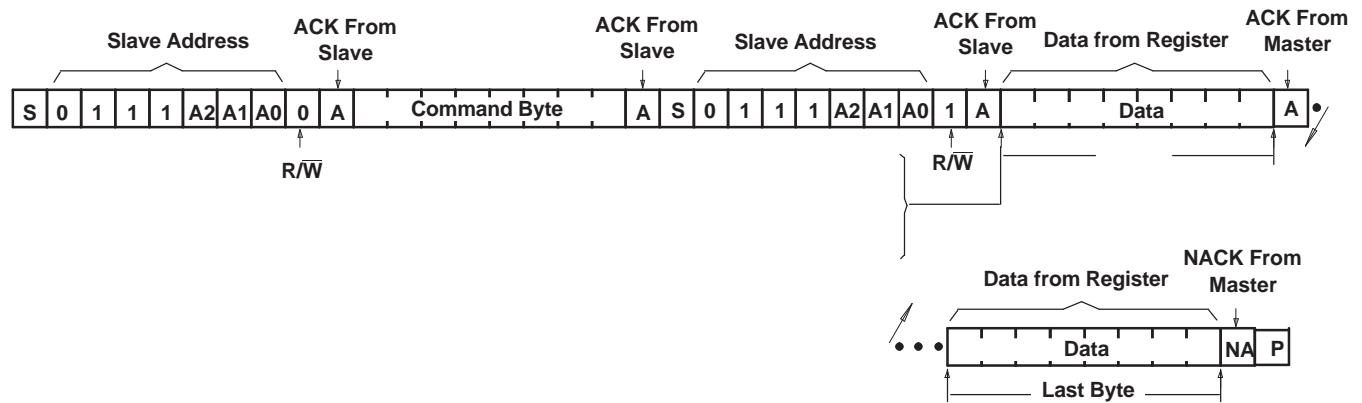
Figure 8. Read From Register

Figure 9. Read Input Port Register
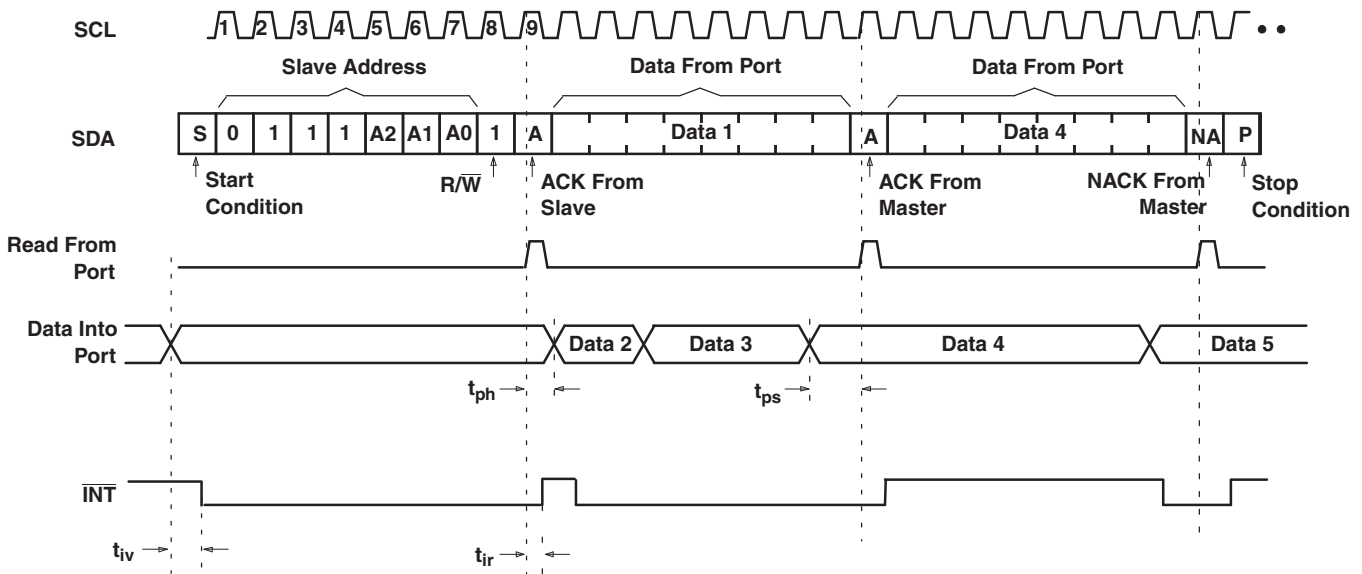
A. This figure assumes that the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a stop condition.

C. This figure eliminates the command byte transfer, a restart and slave address call between the initial slave address call and the actual data transfer from the P Port. See Figure 8 for these details.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
V_I	Input voltage range[2]		−0.5	6	V
V_O	Output voltage range[2]		−0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND			−250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance[3]	DB package		82	°C/W
		DBQ package		90	
		DGV package		86	
		DW package		46	
		N package		67	
		PW package		88	
		RGT package		TBD	
		RGV package		51	
T_{stg}	Storage temperature range		−65	150	°C

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3)   The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P7–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	V
		A2–A0, P7–P0	−0.5	0.8	
I_{OH}	High-level output current	P7–P0		−10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		−40	85	°C

PCA9534A

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.3 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage[2]	$I_{OH} = -8$ mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		$I_{OH} = -10$ mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	8		mA
	P port[3]	$V_{OL} = 0.5$ V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		$V_{OL} = 0.7$ V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	μA
	A2–A0					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	μA
I_{IL}	P port	$V_I = $ GND	2.3 V to 5.5 V			−1	μA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{scl} = 400$ kHz	5.5 V		104	175	μA
			3.6 V		50	90	
			2.7 V		20	65	
		$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, $f_{scl} = 100$ kHz	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	$V_I = $ GND, $I_O = 0$, I/O = inputs, $f_{scl} = 0$ kHz	5.5 V		0.25	1	
			3.6 V		0.2	0.9	
			2.7 V		0.1	0.8	
ΔI_{CC}	Additional current in standby mode	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		All LED I/Os at $V_I = 4.3$ V, $f_{scl} = 0$ kHz	5.5 V			1	
C_I	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25°C$.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7–P0) must be limited to a maximum current of 200 mA.

Product Folder Link(s): *PCA9534A*

I²C INTERFACE TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted) (see Figure 10)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		µs
t_{scl}	I²C clock low time	4.7		1.3		µs
t_{sp}	I²C spike time		50		50	ns
t_{sds}	I²C serial-data setup time	250		100		ns
t_{sdh}	I²C serial-data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$ [(1)]	300	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$ [(1)]	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ [(1)]	300	ns
t_{buf}	I²C bus free time between stop and start	4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup	4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold	4		0.6		µs
t_{sps}	I²C stop condition setup	4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	µs
C_b	I²C bus capacitive load		400		400	ns

(1) C_b = total capacitive of one bus in pF

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (see Figure 11 and Figure 12)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		200		200	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
TEMPERATURE
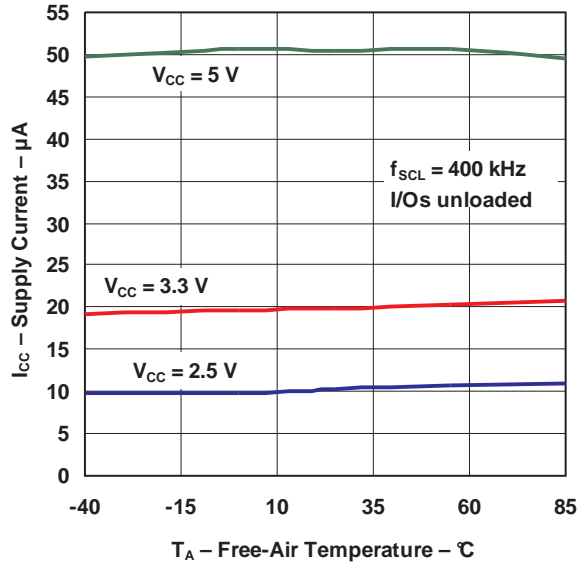
QUIESCENT SUPPLY CURRENT
vs
TEMPERATURE
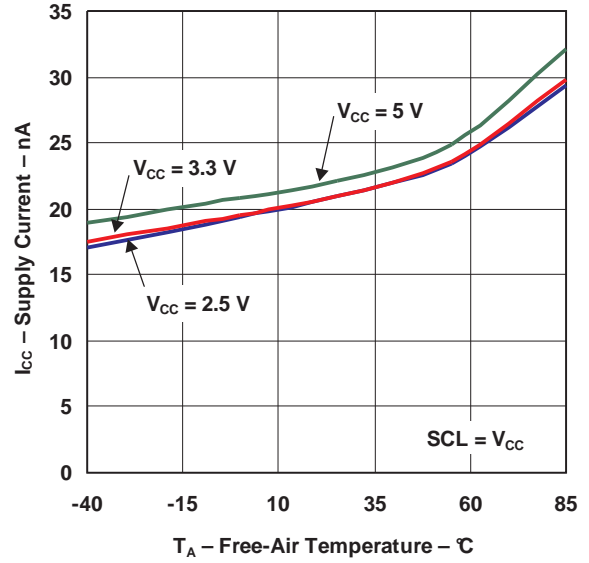
SUPPLY CURRENT
vs
SUPPLY VOLTAGE
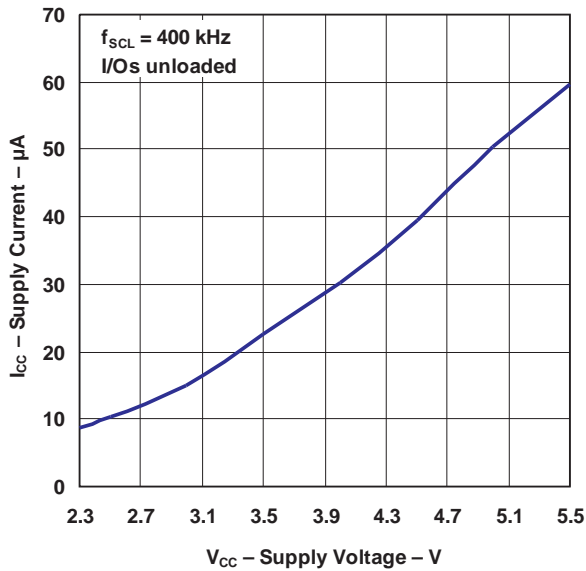
SUPPLY CURRENT
vs
NUMBER OF I/Os HELD LOW
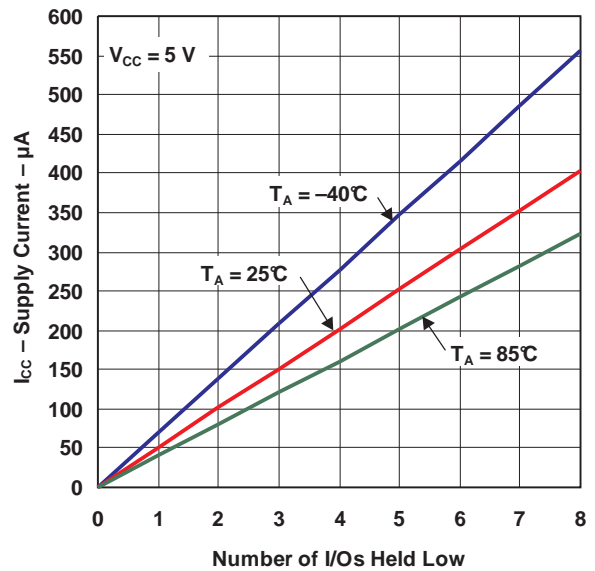
TYPICAL CHARACTERISTICS (continued)

**I/O OUTPUT LOW VOLTAGE
vs
TEMPERATURE**
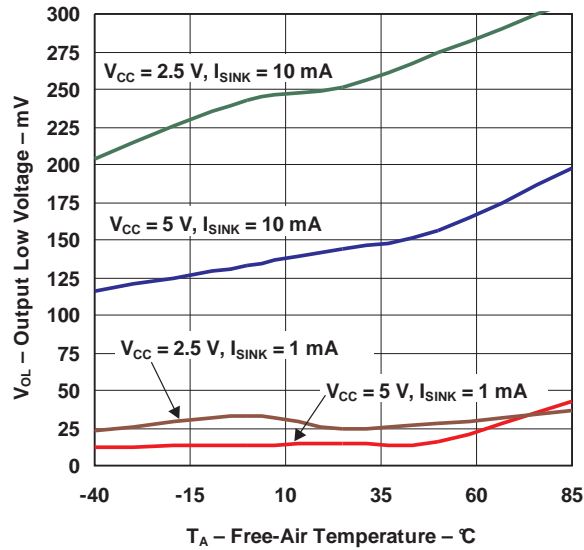
**I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE**
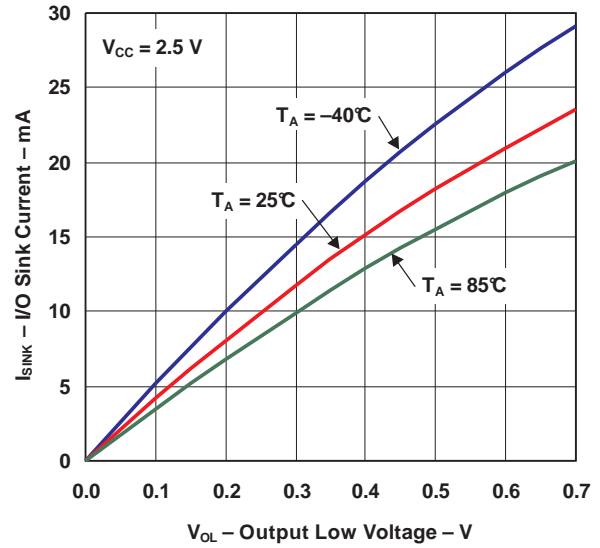
**I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE**

**I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE**

Product Folder Link(s): *PCA9534A*
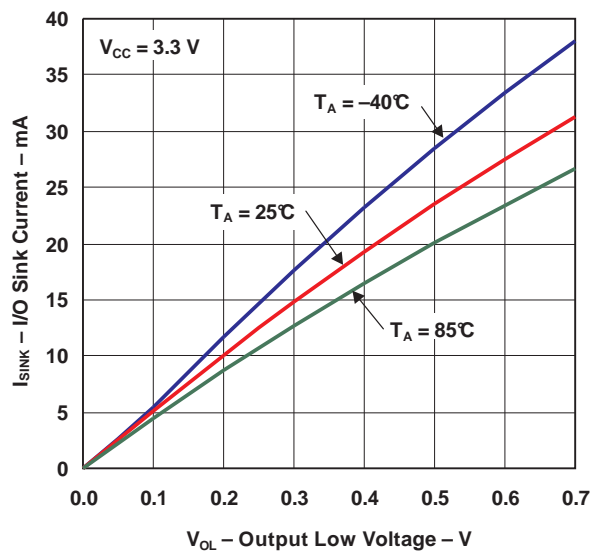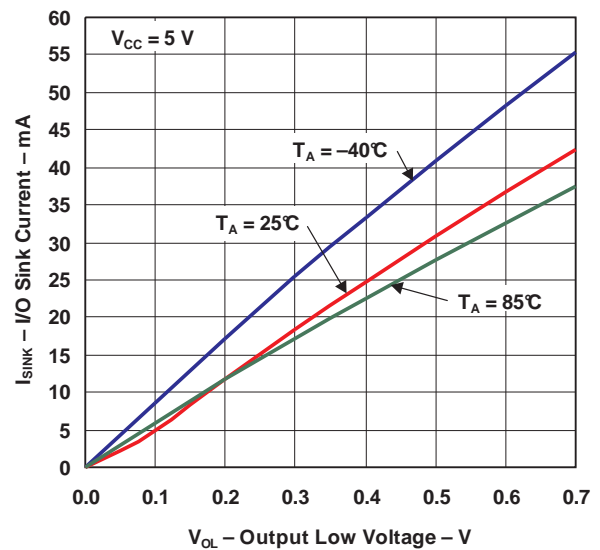
TYPICAL CHARACTERISTICS (continued)

I/O OUTPUT HIGH VOLTAGE
vs
TEMPERATURE
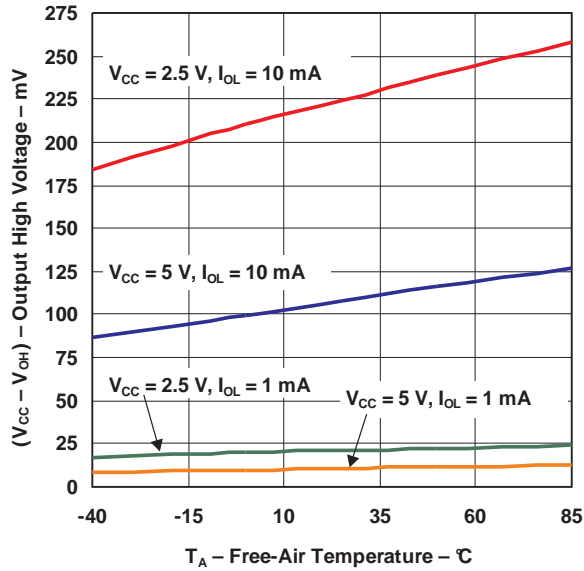
I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE
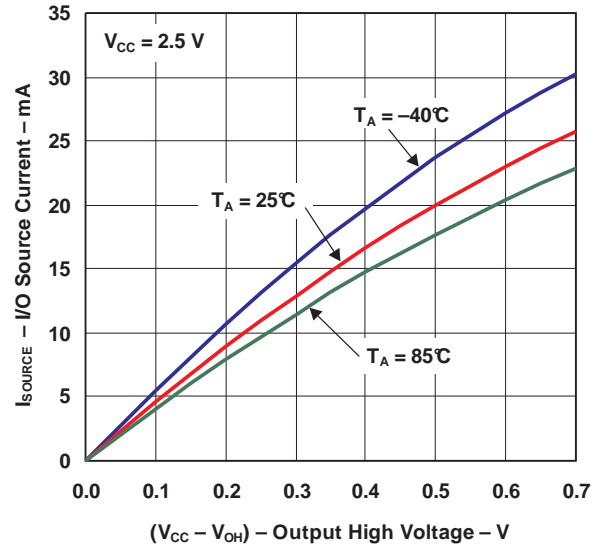
I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE

Product Folder Link(s): *PCA9534A*
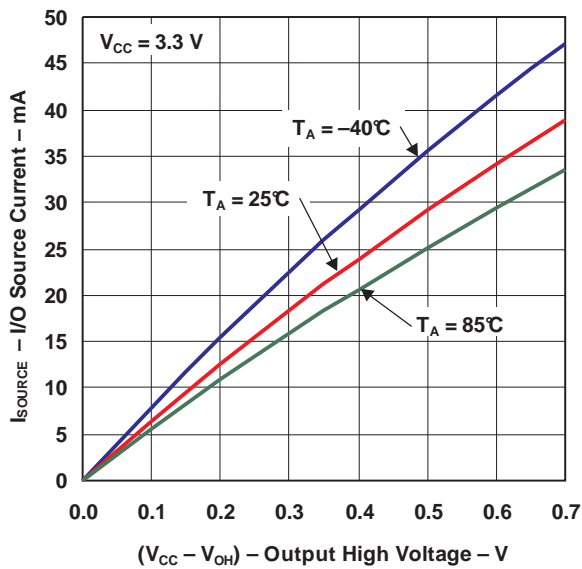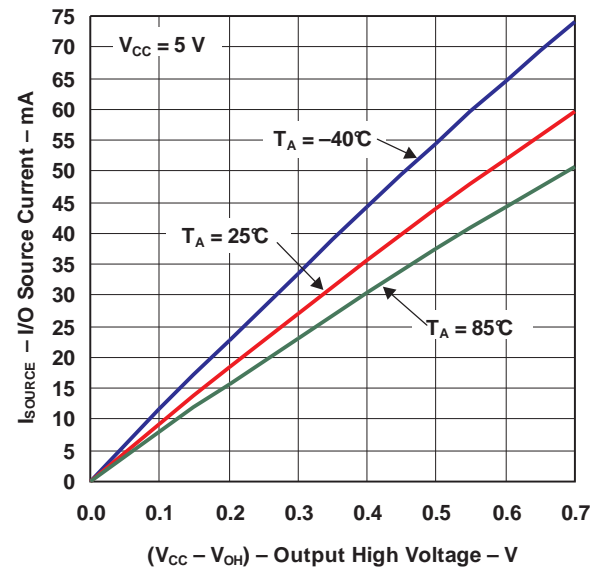
TYPICAL CHARACTERISTICS (continued)

OUTPUT HIGH VOLTAGE
vs
SUPPLY VOLTAGE

$T_A = 25°C$

$I_{OH} = -8$ mA

$I_{OH} = -10$ mA

V_{OH} – Output High Voltage – V

V_{CC} – Supply Voltage – V

Product Folder Link(s): PCA9534A
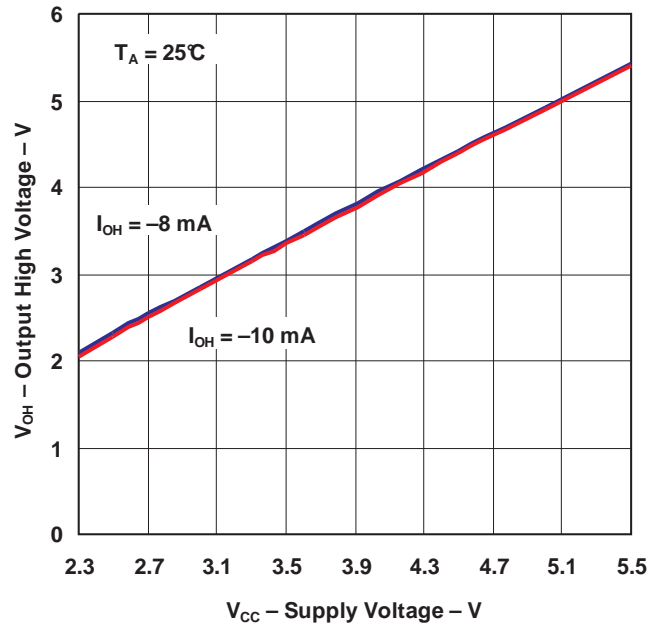
PARAMETER MEASUREMENT INFORMATION
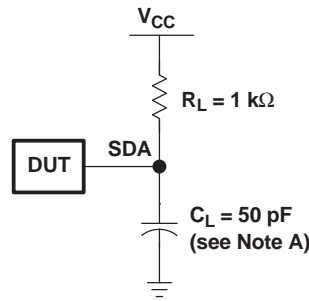
SDA LOAD CONFIGURATION
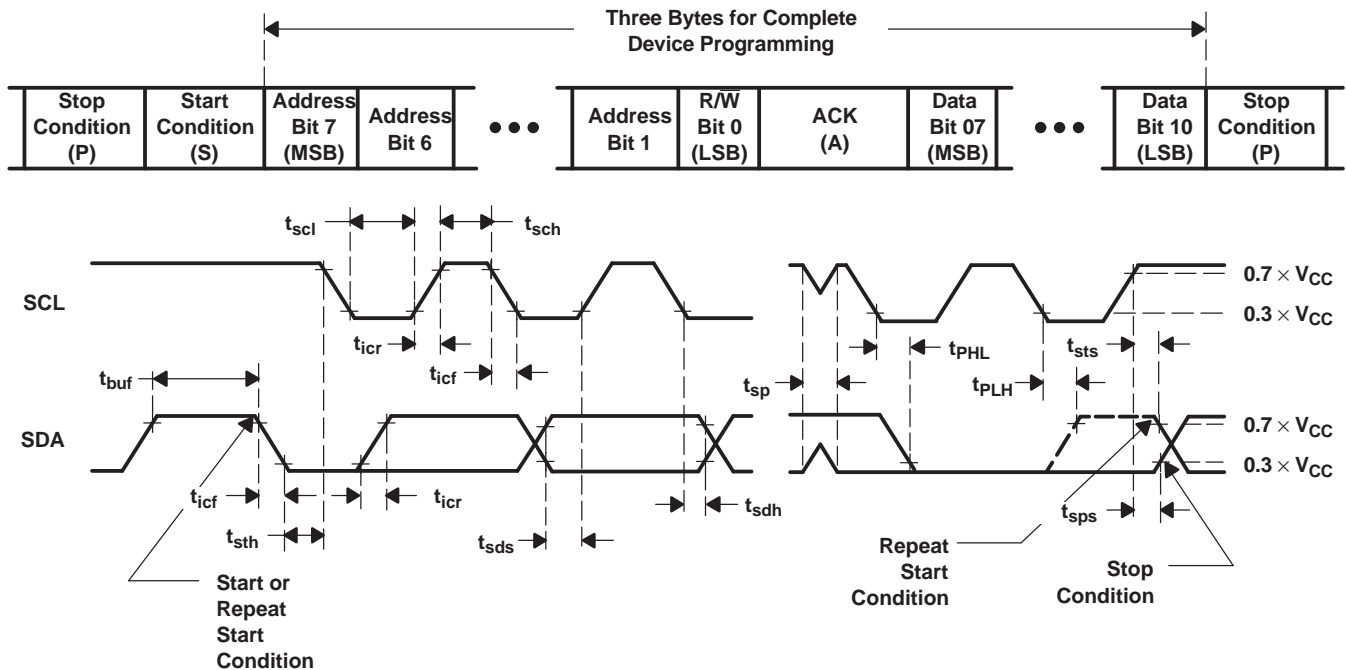
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C.   All parameters and waveforms are not applicable to all devices.

Figure 10. I^2C Interface Load Circuit and Voltage Waveforms
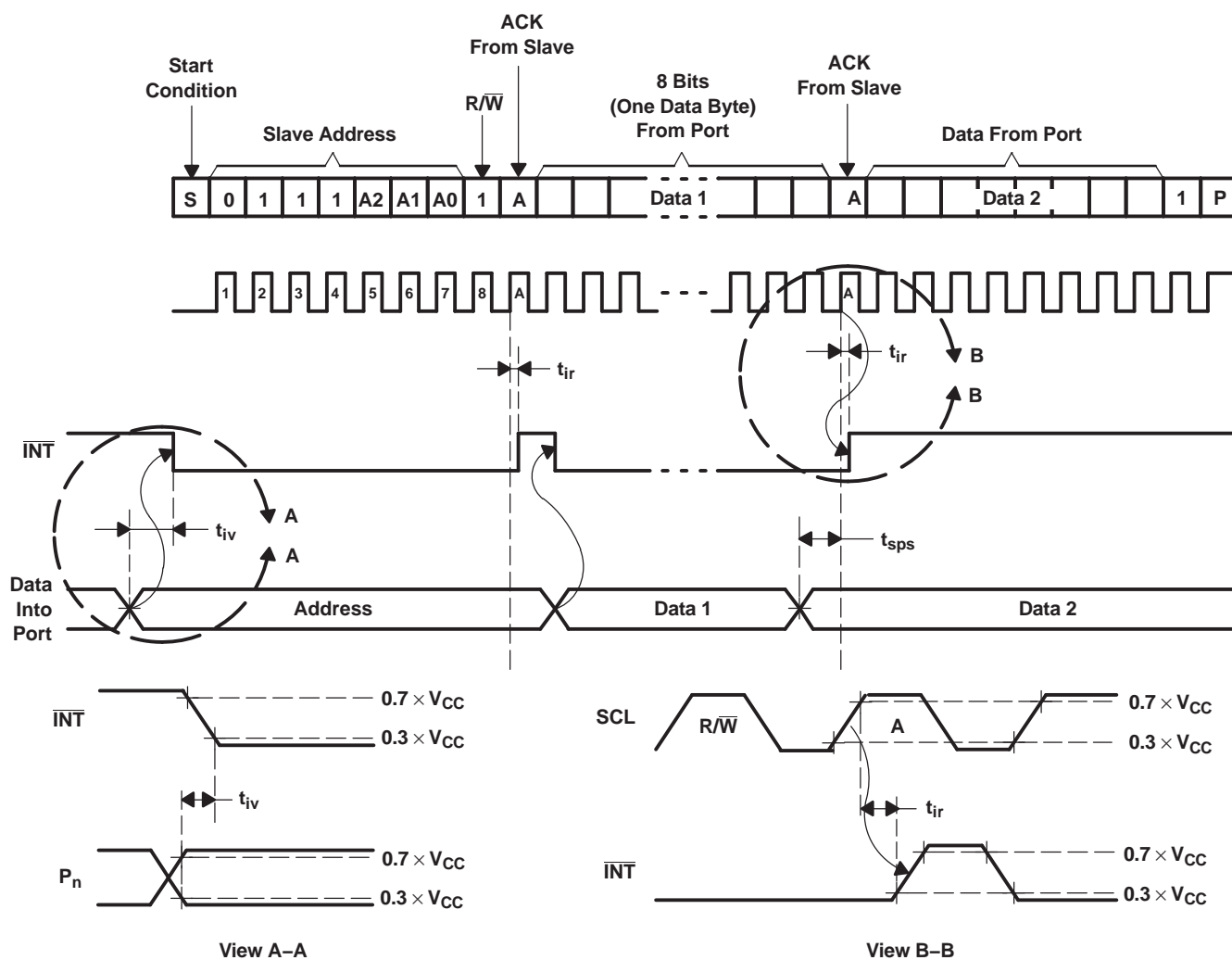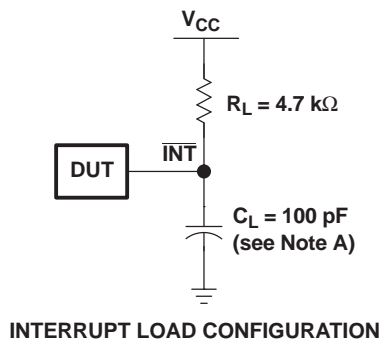
PARAMETER MEASUREMENT INFORMATION (continued)

INTERRUPT LOAD CONFIGURATION

View A–A

View B–B

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 11. Interrupt Load Circuit and Voltage Waveforms

Product Folder Link(s): *PCA9534A*

PARAMETER MEASUREMENT INFORMATION (continued)
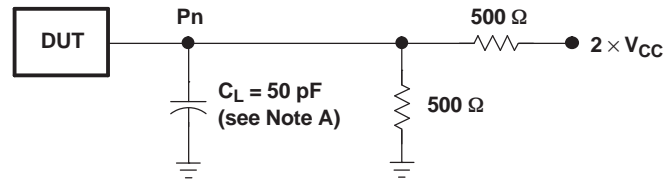
P-PORT LOAD CONFIGURATION
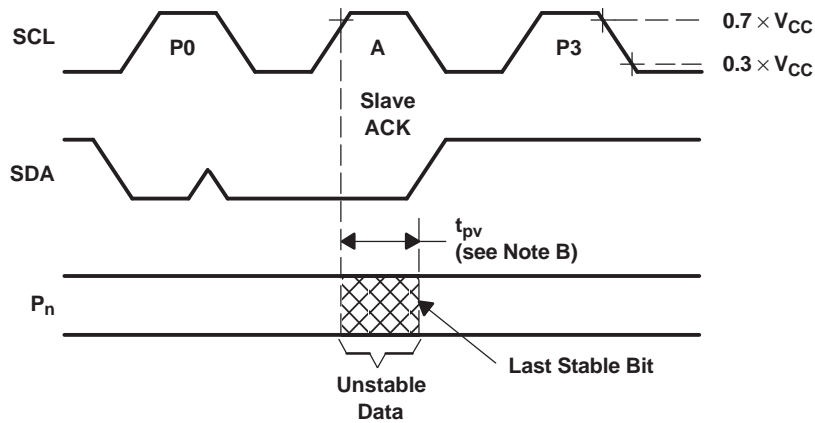
WRITE MODE (R/$\overline{W}$ = 0)
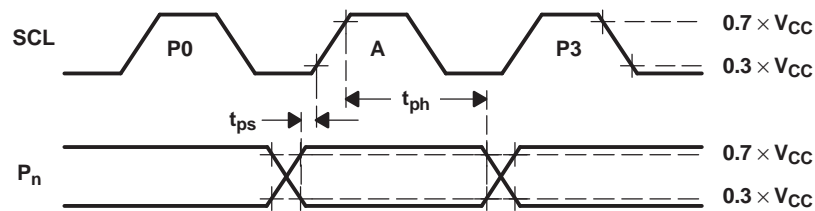
READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.

C.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D.   The outputs are measured one at a time, with one transition per measurement.

E.   All parameters and waveforms are not applicable to all devices.

Figure 12. P-Port Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)
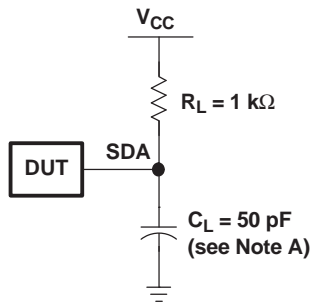
SDA LOAD CONFIGURATION
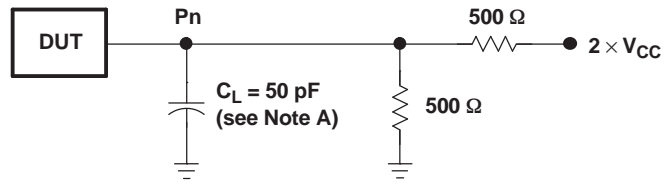
P-PORT LOAD CONFIGURATION
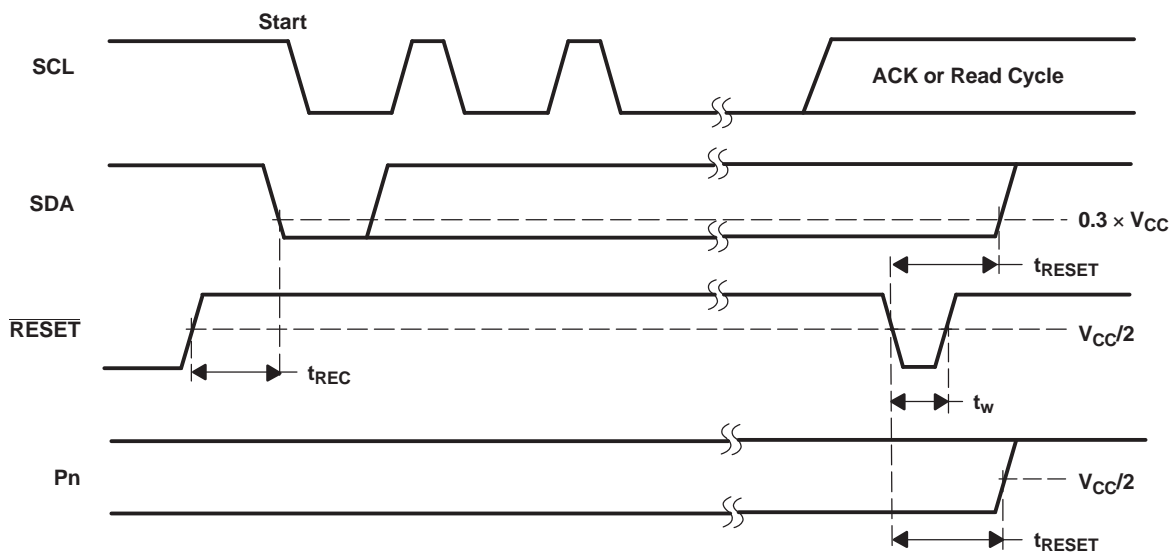
A. C_L includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C.   I/Os are configured as inputs.

D.   All parameters and waveforms are not applicable to all devices.

Figure 13. Reset Load Circuits and Voltage Waveforms

Product Folder Link(s): *PCA9534A*

APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9534A can be used.
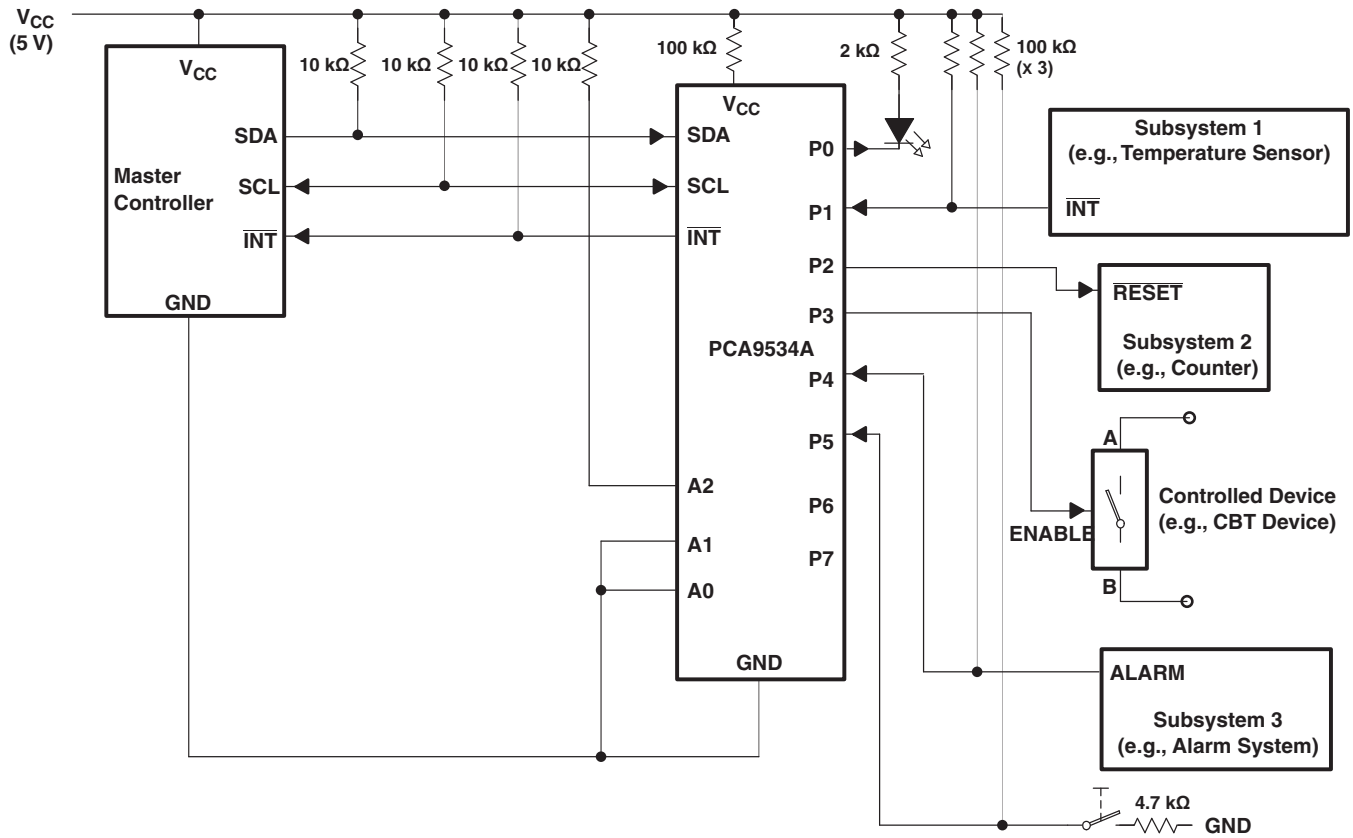
A. Device address is configured as 0111100 for this example.

B. P0, P2, and P3 are configured as outputs.

C. P1, P4, and P5 are configured as inputs.

D. P6 and P7 are not used and must be configured as outputs.

Figure 14. Typical Application

Minimizing I_{CC} When the I/O Controls LEDs

When the I/Os are used to control LEDs, they normally are connected to V_{CC} through a resistor as shown in Figure 14. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of the I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.
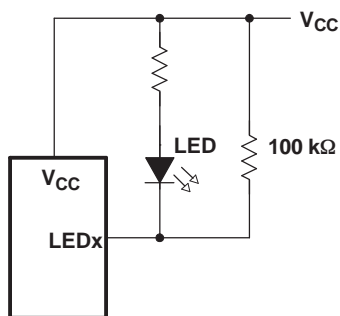
Figure 15. High-Value Resistor in Parallel With the LED
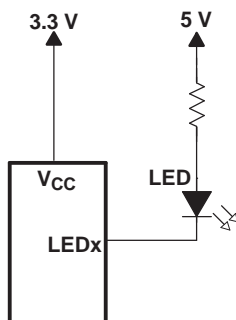
Figure 16. Device Supplied by a Lower Voltage

Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9534A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 17 and Figure 18.
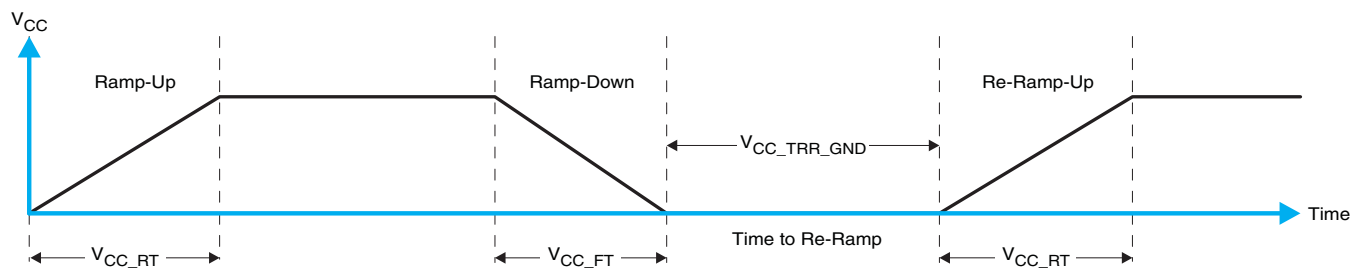
Figure 17. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}
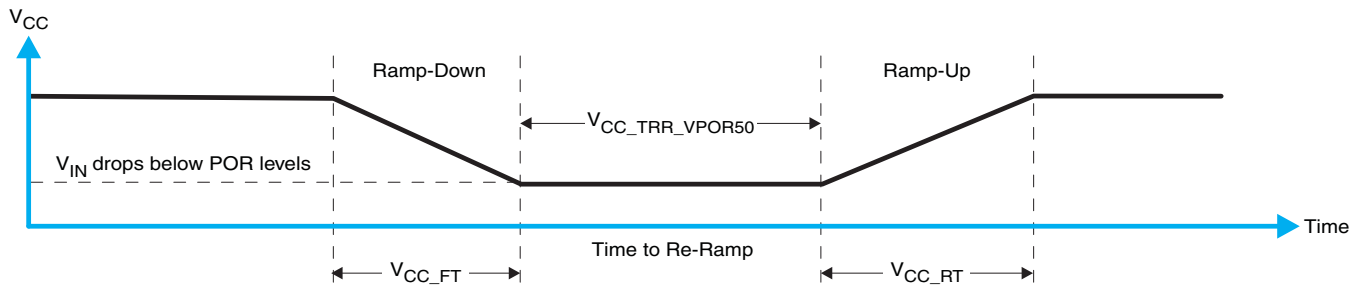
Figure 18. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 10 specifies the performance of the power-on reset feature for PCA9534A for both types of power-on reset.

Table 10. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES[1]

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 17	1		100	ms
V_{CC_RT}	Rise rate	See Figure 17	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 17	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR\_MIN} - 50$ mV)	See Figure 18	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ μs	See Figure 19			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCx}$	See Figure 19				μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}			0.767	1.144	V
V_{PORR}	Voltage trip point of POR on fising V_{CC}			1.033	1.428	V

(1) $T_A = -40°C$ to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 19 and Table 10 provide more information on how to measure these specifications.

Figure 19. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^{2}C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 20 and Table 10 provide more details on this specification.
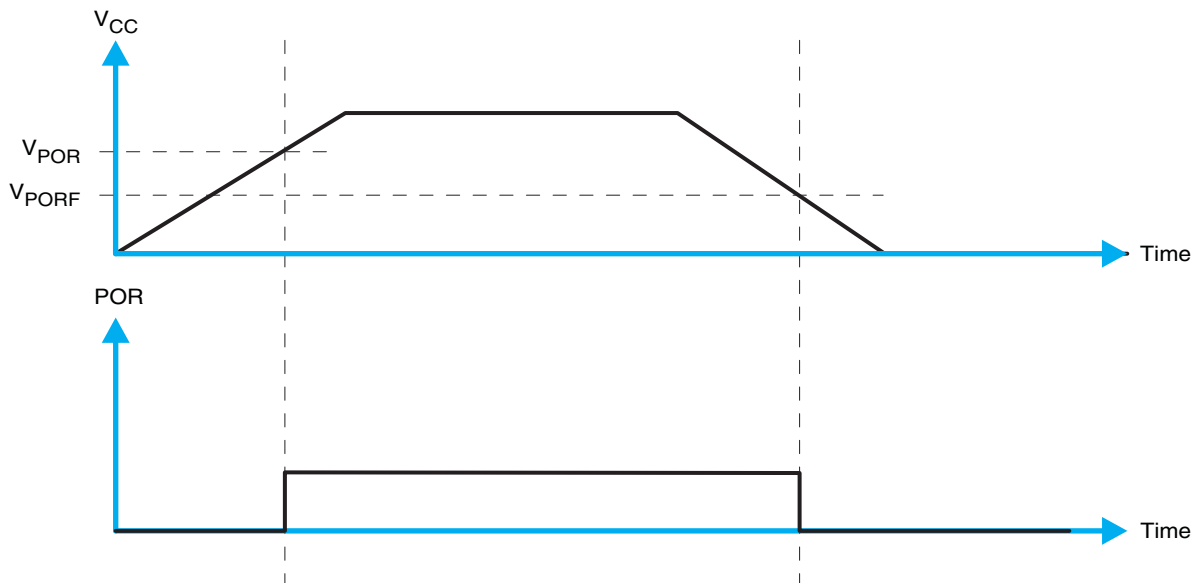
Figure 20. V$_{POR}$

Interrupt Requirements
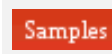
The expected performance of the interrupt feature is that $\overline{INT}$ is to be cleared (de-asserted) when the input register is read or all inputs return to the last read values. $\overline{INT}$ is also de-asserted when both of the following occur:

- The last I^{2}C command byte (register pointer) written was 00h. This generally means the last operation with the device was a read of the input register, but the command byte may have been written with 00h without ever going on to read the Input register.
- Any other slave device on the I^{2}C bus acknowledges an address byte with the R/$\overline{W}$ bit set high. This occurs when reading any other valid device on the bus.

In order to prevent $\overline{INT}$ from de-asserting when another device is read on the I^{2}C bus, the user needs to change the command byte to something other than 00 (hex) after a read operation to the device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9534ADB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534A	Samples
PCA9534ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534A	Samples
PCA9534ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534A	Samples
PCA9534ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534A	Samples
PCA9534APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534A	Samples
PCA9534ARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVJ	Samples
PCA9534ARGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVJ	Samples
PCA9534ARGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD534A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9534ARGVRG4	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD534A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9534ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
PCA9534ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9534ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9534APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9534ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9534ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
PCA9534ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
PCA9534ADWR	SOIC	DW	16	2000	367.0	367.0	38.0
PCA9534APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
PCA9534ARGTR	QFN	RGT	16	3000	367.0	367.0	35.0

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 | Ⓜ

16   9

Ⓓ   4,50
    4,30

6,60
6,20

1   8

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌓ | 0,10

4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         Ⓒ   Body length does not include mold flash, protrusions, or gate burrs.   Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         Ⓓ   Body width does not include interlead flash.   Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

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PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x0,65

16x0,30

14x0,65

16x1,55

5,60

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211284−3/F   12/12

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{3,15}{2,85}$ A

B

$\frac{3,15}{2,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

◯ 0,08

$\frac{0,05}{0,00}$ C

16X $\frac{0,50}{0,30}$

1   4

16   5

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE
SHEET

13   8

12   9

16X $\frac{0,30}{0,18}$

0,50

⊕ | 0,10 Ⓜ | C | A | B
  | 0,05 Ⓜ | C

4203495/H 10/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. Quad Flatpack, No−leads (QFN) package configuration.
         D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F. Falls within JEDEC MO−220.

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RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C=0.30

Exposed Thermal Pad

1,45 ±0,10

1,45±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206349−2/S 04/13

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16)   PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

Note D

12x0,5

2,1 3,8

2,1

3,8

Non Solder Mask
Defined Pad

R0,14   0,08

0,85
0,07
All around

0,28

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

Example Stencil Design
(Note E)

12x0,5

R0,115

16x0,230

1,2

1,2

2,15 3,75

2,15

3,75

68% solder coverage on center pad

Example Via Layout Design
Via pattern may vary due
to layout constraints
(Note D, F)

5xØ0,3   1,45

1,45

0,45

0,45   0,9

0,45
0,9

4208050–4/H   05/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC–7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RGV (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

$\dfrac{4,15}{3,85}$ A

B

$\dfrac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\dfrac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

| 0,08

$\dfrac{0,05}{0,00}$ C

16X $\dfrac{0,65}{0,45}$

0,65

1

4

16

5

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

13

8

12

9

16X $\dfrac{0,38}{0,23}$

⊕	0,10 Ⓜ C A B
	0,05 Ⓜ C

4203497/F 06/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No−leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO−220.

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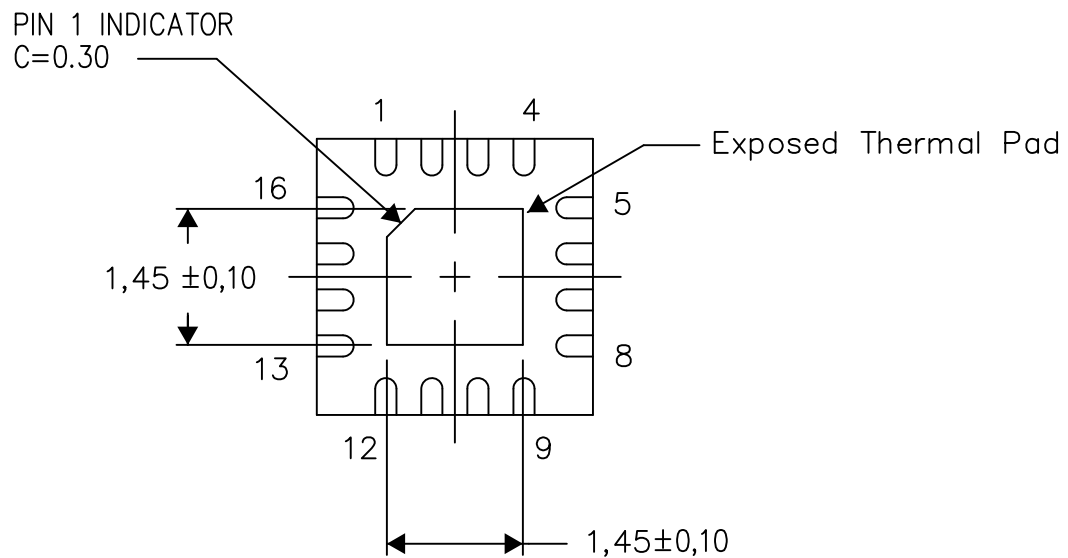RGV (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Pin 1 indicator is electrically tied
to the exposed thermal pad
Pin 1 indicator metal feature may
not be present on some devices

0,18±0,05 (2 Places)

0,35±0,05 (2 Places)

1   4

Exposed Thermal Pad

16   5

2,16±0,10

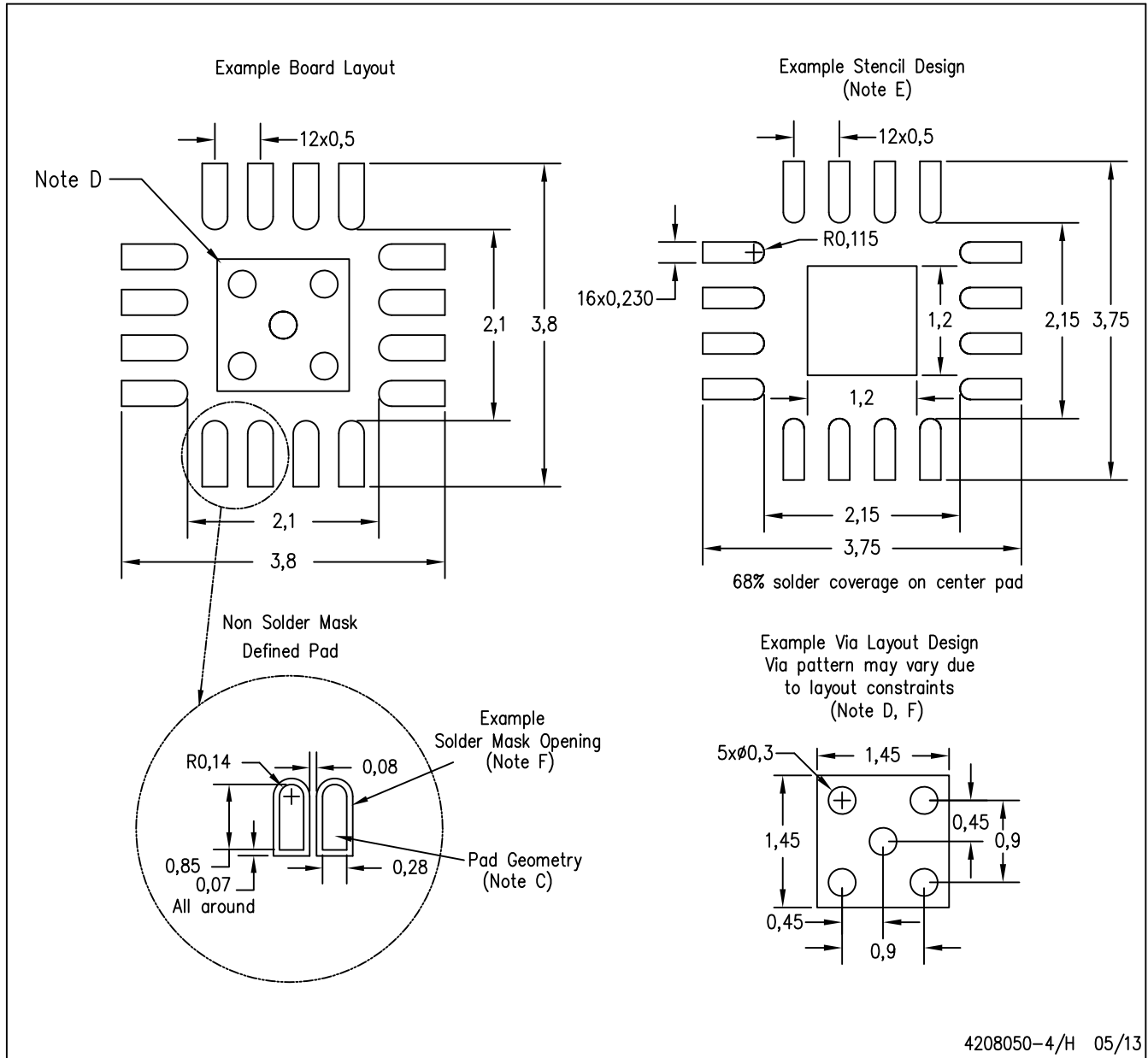13   8

12   9

2,16±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206351−2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD
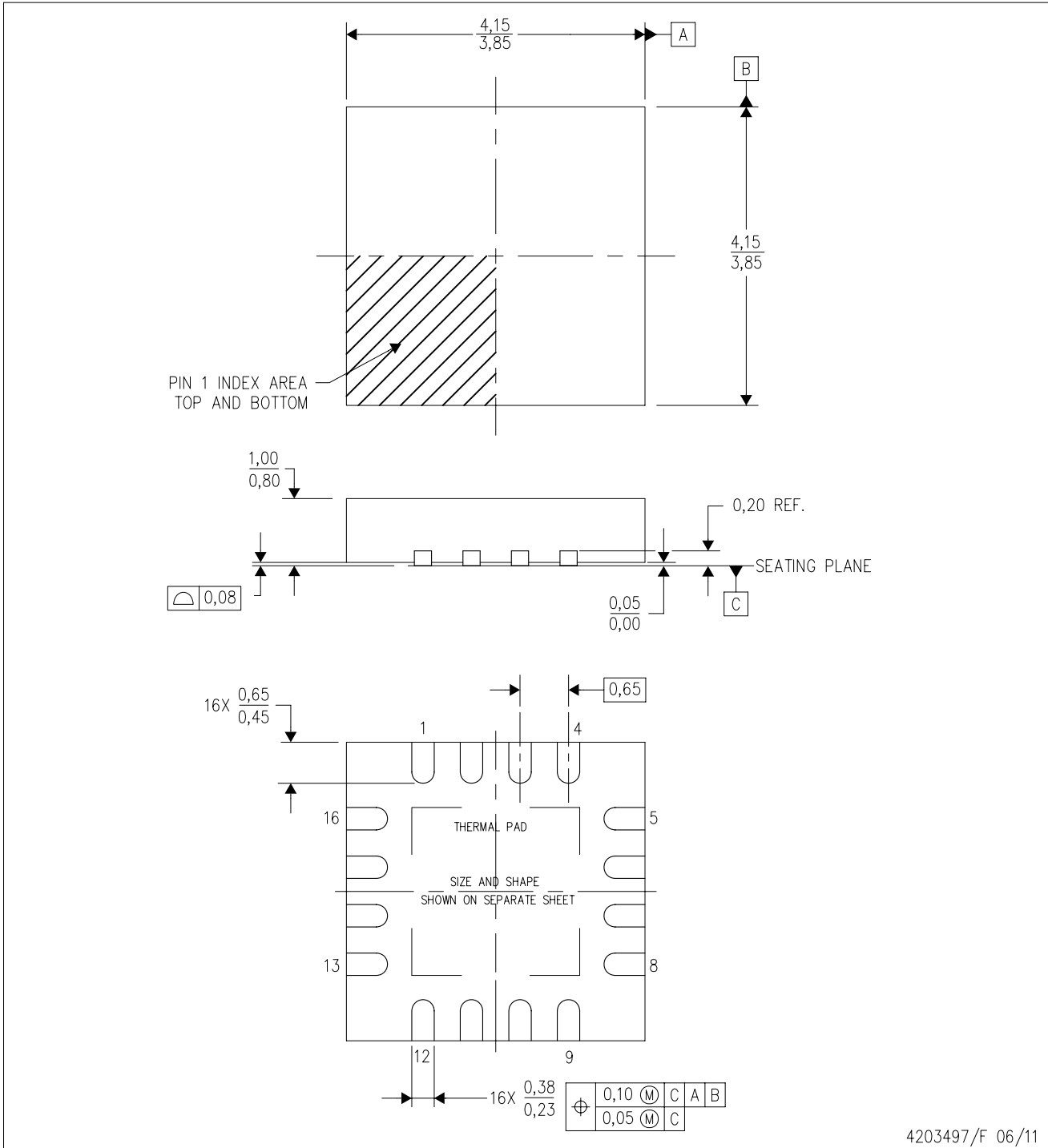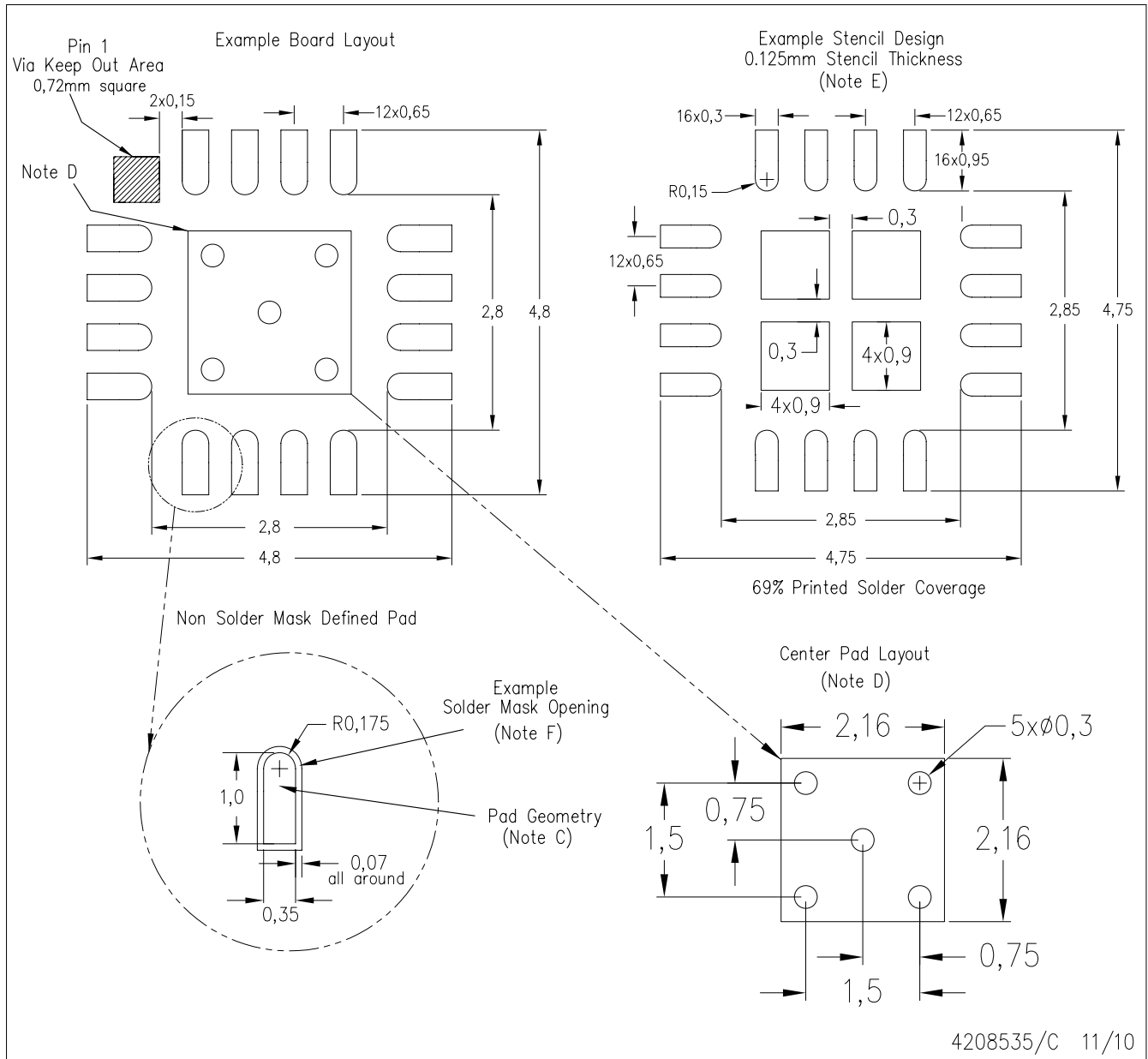
Example Board Layout

Pin 1
Via Keep Out Area
0,72mm square

2x0,15

12x0,65

Note D

2,8   4,8

2,8

4,8

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

R0,175

Pad Geometry
(Note C)

1,0

0,07
all around

0,35

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

16x0,3

12x0,65

16x0,95

R0,15

0,3

12x0,65

2,85   4,75

0,3

4x0,9

4x0,9

2,85

4,75

69% Printed Solder Coverage

Center Pad Layout
(Note D)

2,16

5xØ0,3

1,5

0,75

2,16

0,75

1,5

4208535/C 11/10

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Publication IPC−7351 is recommended for alternate designs.
       D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN
           Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
           for specific thermal information, via requirements, and recommended board layout. These documents are available at
           www.ti.com <http://www.ti.com>.
       E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
           contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
       F. Customers should contact their board fabrication site for solder mask tolerances.

DW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

Pin 1
Index Area

1   8

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−2/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
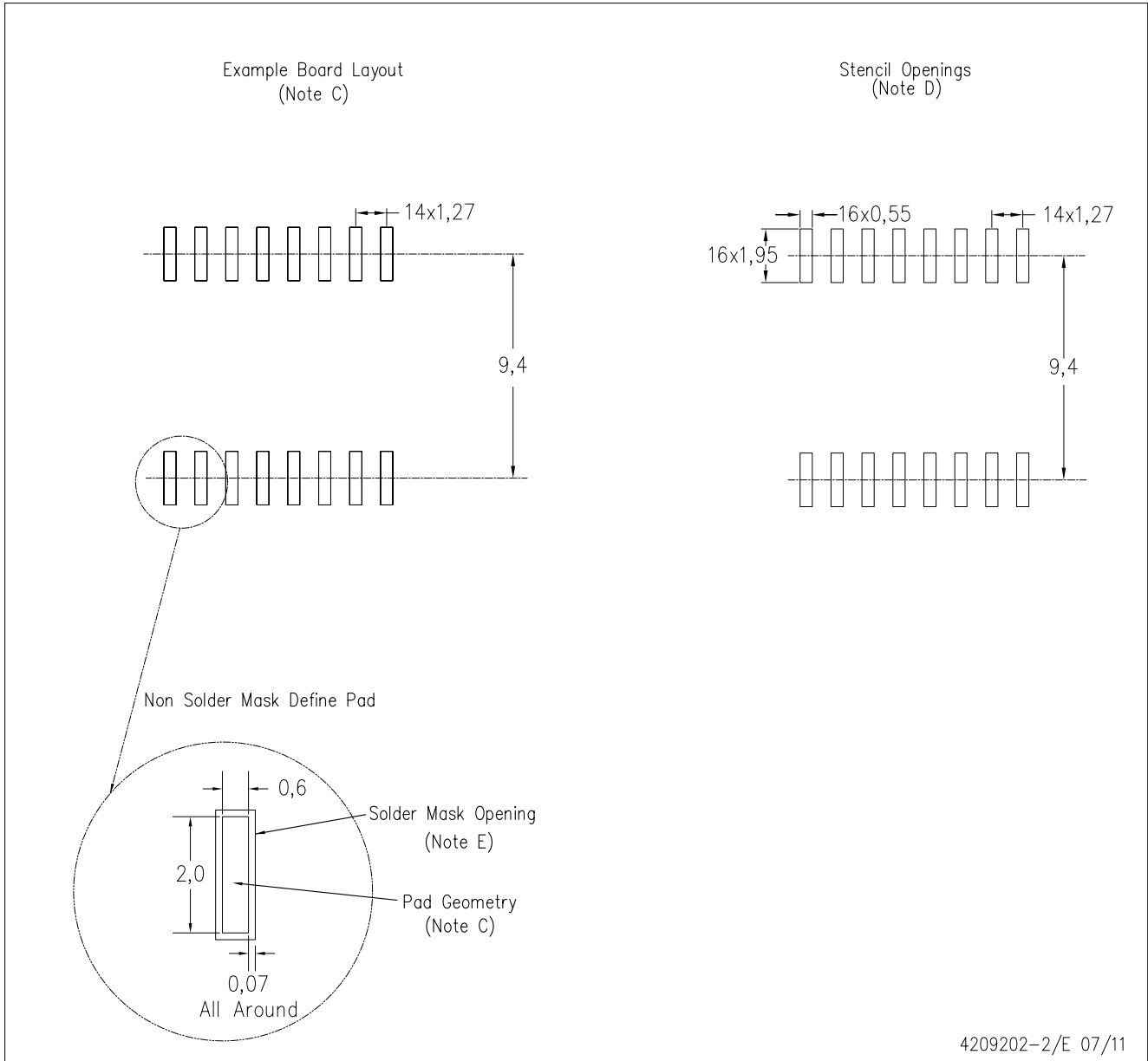   B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AA.

DW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55   14x1,27

16x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−2/E 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Refer to IPC7351 for alternate board design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
       D. Falls within JEDEC MO-150

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