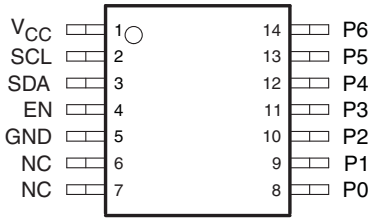
TCA6507
LOW-VOLTAGE 7-BIT I²C AND SMBus LED DRIVER WITH INTENSITY CONTROL AND SHUTDOWN

SCPS164B – MAY 2007 – REVISED NOVEMBER 2007

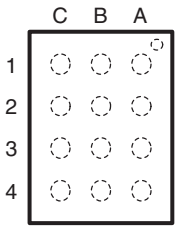
FEATURES

- **Seven LED Driver Outputs: On, Off, Blinking, Fading at Programmable Rates**
- **Open-Drain Outputs Directly Drive LEDs to 40 mA Max**
- **Can Be Configured Into Two Independent Banks of LED Drivers**
- **Widely Programmable Blink Rates, Fade-On and Fade-Off Rates and Maximum Intensity**
- **LED Intensity Set Using Pulse Width Modulation (PWM)**
- **Outputs Not Used as LED Drivers Can Be Used as Regular General-Purpose Open-Drain Outputs**
- **16 Steps of Maximum Intensity Control from Fully-Off to Fully-On States**
- **256 Intensity Levels During Fade-On or Fade-Off for Smooth Perceived Transition**
- **Operating Power-Supply Voltage Range of 1.65 V to 3.6 V**
- **EVM Available**
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Inputs**
  - **V_{hys} = 0.18 V Typ at 1.8 V**
  - **V_{hys} = 0.25 V Typ at 2.5 V**
  - **V_{hys} = 0.33 V Typ at 3.3 V**
- **5.5-V Tolerant Open-Drain Outputs**
- **Low Standby Current with Shutdown Capability for Additional Power Savings**
- **Internal Power-On Reset**
- **Internal Oscillator Requires No External Components**
- **Programmed Through I²C Bus Interface Logic Compatible With SMBus**
- **400-kHz Fast I²C Bus**
- **Noise Filter on SCL/SDA Inputs**
- **No Glitch on Power Up**
- **Supports Hot Insertion**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

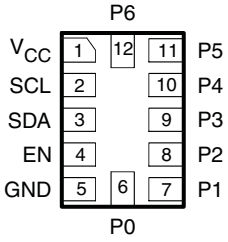
PW PACKAGE (TOP VIEW)



ZXU PACKAGE (TOP VIEW)



RUE PACKAGE (TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

This 7-bit LED dimmer for the two-line bidirectional bus (I²C) is designed to control (or dim) LEDs via the I²C interface [serial clock (SCL), serial data (SDA)]. Without this device, the microprocessor or microcontroller must be actively involved in turning on and off the LEDs (per the required dimming rate), which uses valuable processor time and the overloads I²C bus. The TCA6507 alleviates this issue by limiting the number of operations required by the processor in blinking LEDs and, thus, helps to create a more efficient system.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	BGA – ZXU (Pb-free)	Reel of 2500	TCA6507ZXUR	PH507
	QFN – RUE	Reel of 3000	TCA6507RUER	2M
	TSSOP – PW	Reel of 2000	TCA6507PWR	PH507

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

This device can be used for driving LEDs and for general-purpose parallel output expansion. The TCA6507 has three Select registers (Select0, Select1 and Select2), which can be used to configure each LED output into one of seven different operating modes. At power on, the outputs are in high impedance.

When used to drive LEDs, the seven outputs can be configured into two banks of outputs (BANK0 and BANK1). Each bank of outputs can be independently controlled for dimming rate and intensity through the I²C bus. The dimming and blink rates are fully programmable. The intensity of each bank of LEDs is controlled by dynamically varying the duty cycle of the signal, which has a period of approximately 8 ms and a pulse rate of 125 times per second, driving the outputs. The TCA6507 has two independent dimming/blinking modules—PWM0 and PWM1—driven by a single internal oscillator that supports these features. PWM0 determines the characteristics of BANK0 and PWM1 determines the characteristics of BANK1.

The TCA6507 has a master intensity level known as the ambient light detection (ALD) value. The associated pulse width modulation (PWM) signal for this value is PWMALD. The TCA6507 can be programmed such that PWMALD overrides PWM0 or PWM1 so selected LEDs are on steadily at the master intensity level. Further, the TCA6507 can be programmed such that the ALD value can override the maximum intensity values for PWM0 and PWM1. Thus, the ALD value can control the brightness of all LEDs whether they are on steadily or controlled by one of the dimming modules. The ALD value is stored in the lower four bits of the One-Shot / Master Intensity register.

When the I²C bus is idle, and intensity control is not used, the TCA6507 can be put into shutdown mode by setting the enable (EN) pin low. This mode provides additional power savings, as it is a low-power mode where the LEDs are off. A low signal on the EN pin also resets the registers and I²C/SMBus state machine in the TCA6507 to their default state.

An initial setup command must be sent from the I²C master to the TCA6507 to program the dimming rate and intensity (and intensity ramp if needed) for each bank of outputs. From then on, only one command from the bus master is required to turn each individual output ON, OFF, or to cycle at the programmed dimming rate. The default value for all time parameters is 256 ms so the default blink rate is approximately one per second.

The TCA6507 is optimized for 1.65 V to 3.6 V on the SDA/SCL side, but the LEDs can be driven by any voltage up to 5.5 V. This allows the TCA6507 to interface with next-generation microprocessors and microcontrollers, where supply levels are dropping down to conserve power.

This LED dimmer supports hot insertion.

ZXU PACKAGE TERMINAL ASSIGNMENTS

	C	B	A
1	P1	P2	GND
2	P3	EN	SDA
3	P4	P0	SCL
4	P5	P6	V_{CC}

TERMINAL FUNCTIONS

BALL POSITION	PIN NO.		NAME	DESCRIPTION
BGA (ZXU)	QFN (RUE)	TSSOP (PW)		
A1	5	5	GND	Ground
A2	3	3	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
A3	2	2	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
A4	1	1	V_{CC}	Supply voltage of I^2C registers, oscillator and control logic. Connect directly to V_{CC} of the external I^2C master. Provides voltage-level translation.
B3	6	8	P0	P-port output 0. Open-drain design structure.
C1	7	9	P1	P-port output 1. Open-drain design structure.
B1	8	10	P2	P-port output 2. Open-drain design structure.
C2	9	11	P3	P-port output 3. Open-drain design structure.
C3	10	12	P4	P-port output 4. Open-drain design structure.
C4	11	13	P5	P-port output 5. Open-drain design structure.
B4	12	14	P6	P-port output 6. Open-drain design structure.
B2	4	4	EN	Enable input. If set to low, it puts the TCA6507 in shutdown mode and resets the internal registers and I^2C/SMBus state machine to their default states

FUNCTIONAL BLOCK DIAGRAM

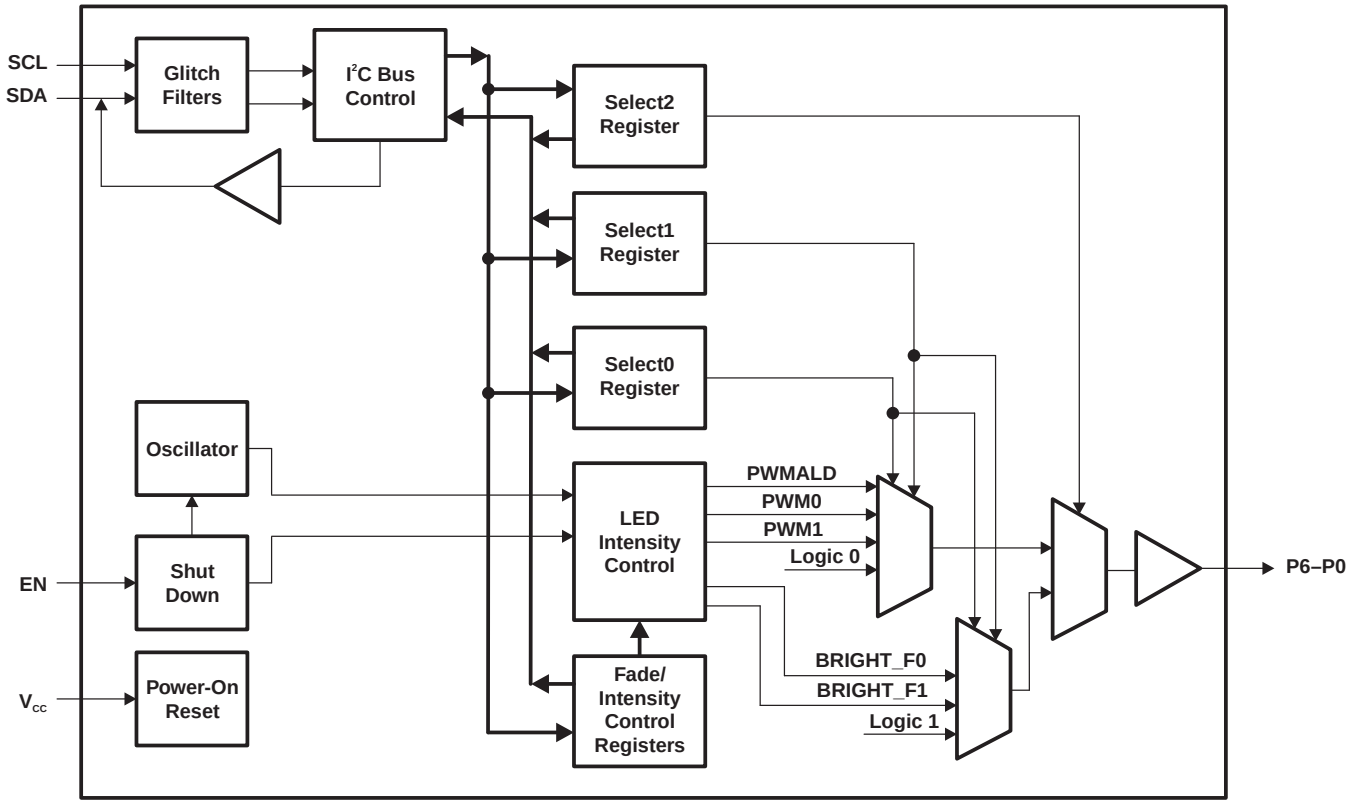
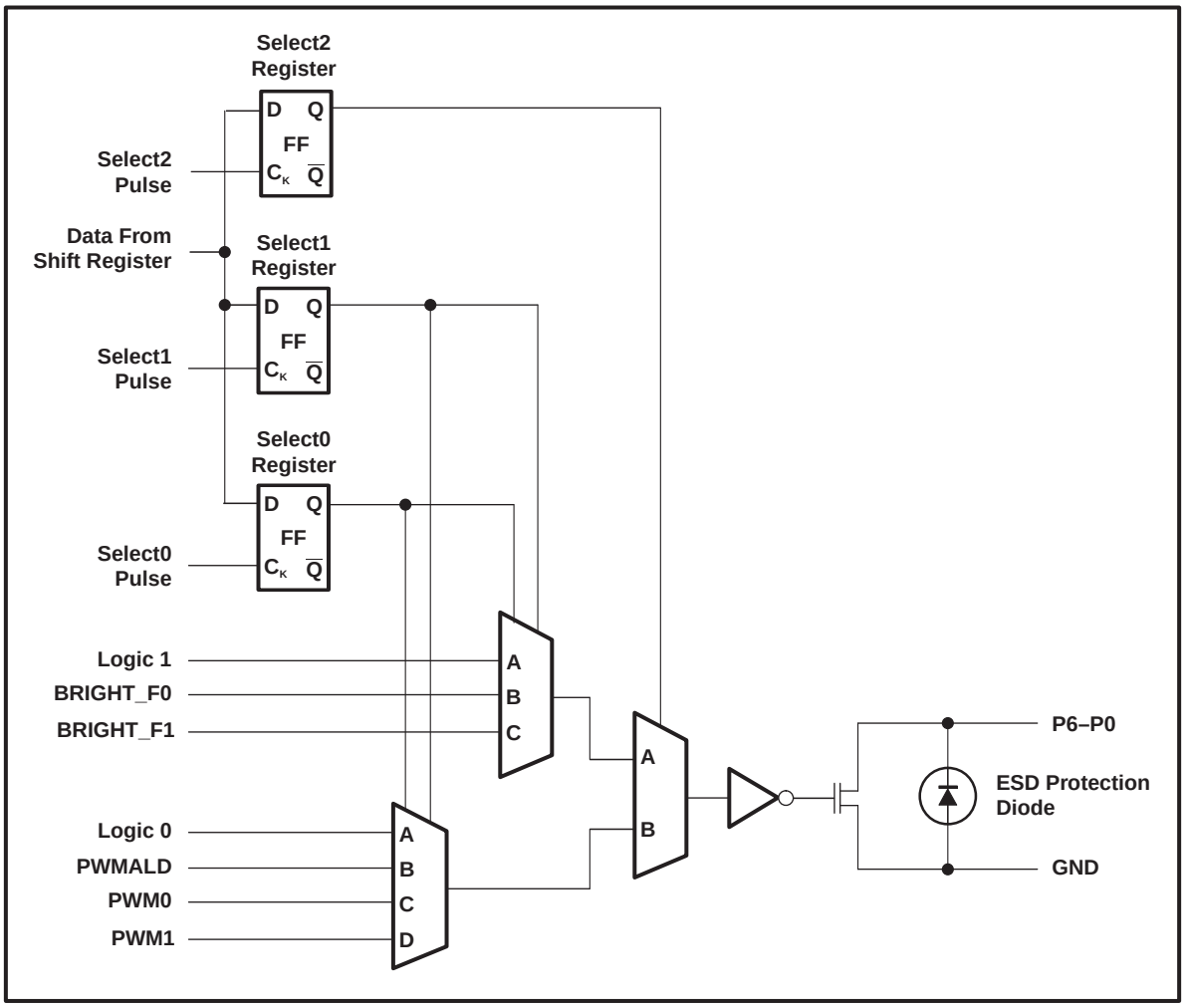


Figure 1. TCA6507 Functional Block Diagram

OUTPUT PORT SIMPLIFIED SCHEMATIC



I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 2). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK)–a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 3).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 2).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 4). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

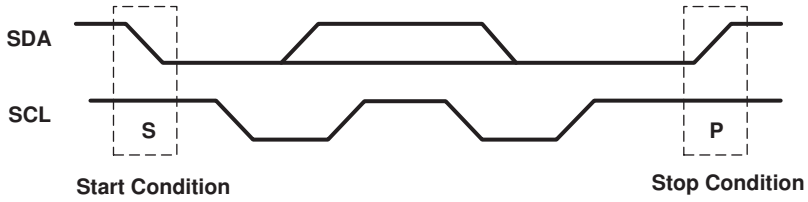


Figure 2. Definition of Start and Stop Conditions

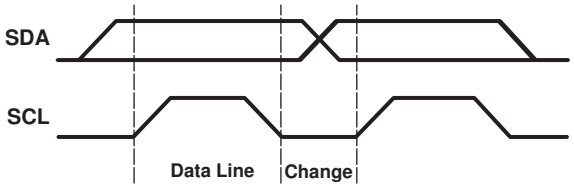


Figure 3. Bit Transfer

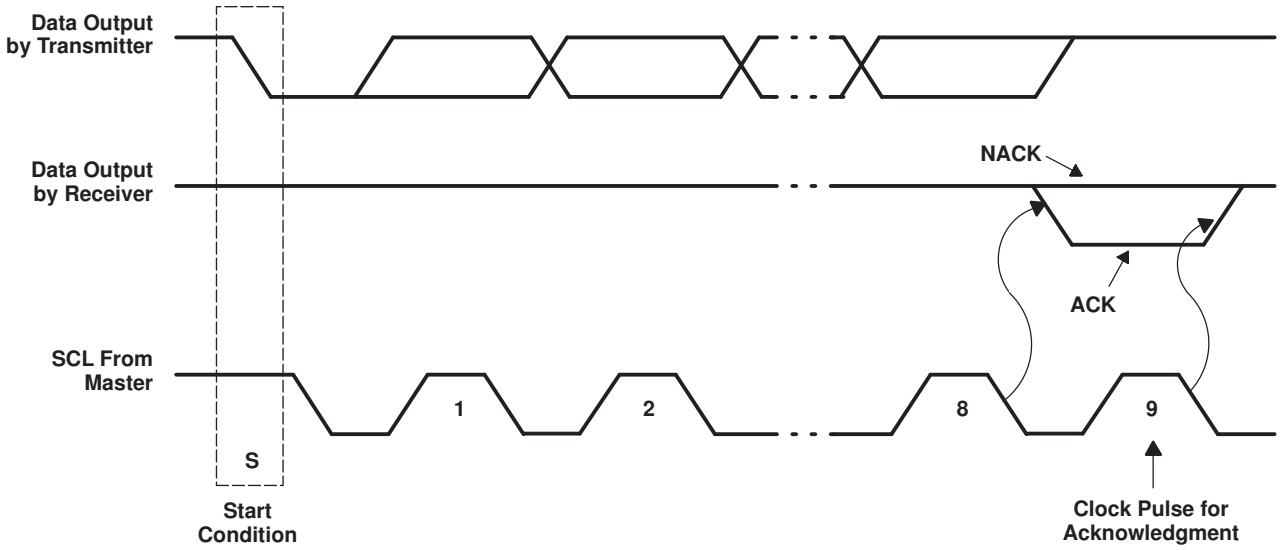


Figure 4. Acknowledgment on the I²C Bus

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	1	0	0	0	1	0	1	R/$\overline{W}$
Px I/O data bus	X(1)	P6	P5	P4	P3	P2	P1	P0

(1) X = Don't care

Device Address

The address of the TCA6507 is shown in Figure 5.

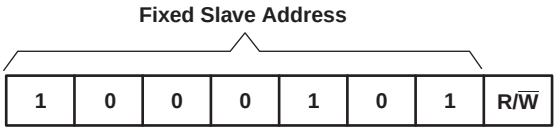


Figure 5. TCA6507 Address

The last bit of the slave address defines the operation (read or write) to be performed. High (1) selects a read operation, and low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register. The last four bits (B0, B1, B2 and B3) of this command byte determine the internal registers (Select0, Select1, Select2, Fade-On Time, Fully-On Time, Fade-Off Time, First Fully-Off Time, Second Fully-Off Time, Maximum Intensity and Initialization) that are affected. The command byte is sent only during a write transmission.

After the command byte is received, the I²C master starts sending data bytes. The first data byte goes into the internal register defined by the command byte. Bit B4 in the command byte is used to determine the programming mode. If B4 is low, all data bytes are written to the register defined by B0, B1, B2, and B3. If B4 is high, the last four bits of the command byte are automatically incremented after the byte is written, and the next data byte is stored in the corresponding register. Registers are written in the sequence shown in Table 3. Once the Initialization register (register 10) is written to, the command byte returns to 0 (Select0 register). Registers 11 to 15 are reserved, and a command byte that references these registers is not acknowledged by the TCA6507.

The upper three bits (B7–B5) of the command byte must be programmed as zeroes for proper operation.

If a Stop condition occurs after the command byte is received, the TCA6507 stores the command byte and then remains idle until the I²C master sends the next operation.

B7	B6	B5	B4	B3	B2	B1	B0

Figure 6. Control Register Bits

Table 2. Command Byte

BIT	FUNCTION
B7	Reserved. Must be programmed as 0.
B6	Reserved. Must be programmed as 0.
B5	Reserved. Must be programmed as 0.
B4	Auto increment
B3	Register address 3
B2	Register address 2
B1	Register address 1
B0	Register address 0

Table 3. Control Register Description

CONTROL REGISTER BITS				COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B3	B2	B1	B0				
0	0	0	0	0x00	Select0	Read/write byte	0000 0000
0	0	0	1	0x01	Select1	Read/write byte	0000 0000
0	0	1	0	0x02	Select2	Read/write byte	0000 0000
0	0	1	1	0x03	Fade-On Time	Read/write byte	0100 0100
0	1	0	0	0x04	Fully-On Time	Read/write byte	0100 0100
0	1	0	1	0x05	Fade-Off Time	Read/write byte	0100 0100
0	1	1	0	0x06	First Fully-Off Time	Read/write byte	0100 0100
0	1	1	1	0x07	Second Fully-Off Time	Read/write byte	0100 0100
1	0	0	0	0x08	Maximum Intensity	Read/write byte	1111 1111
1	0	0	1	0x09	One Shot / Master Intensity	Read/write byte	0000 1111
1	0	1	0	0x10	Initialization	Write byte	N/A
1	0	1	1	0x11	Reserved	N/A	N/A
1	1	0	0	0x12	Reserved	N/A	N/A
1	1	0	1	0x13	Reserved	N/A	N/A
1	1	1	0	0x14	Reserved	N/A	N/A
1	1	1	1	0x15	Reserved	N/A	N/A

Register Descriptions

The Select0 register (register 0), Select1 (register 1), and Select2 register (register 2) configure the state of each of the outputs (see Table 4) .

Table 4. Select2, Select1, and Select0 Register States

SELECT2	SELECT1	SELECT0	STATE
0	0	0	LED off (high impedance)
0	0	1	LED off (high impedance)
0	1	0	LED on steadily with maximum intensity value of PWM0 (ALD value or BRIGHT_F0 value)
0	1	1	LED on steadily with maximum intensity value of PWM1 (ALD value or BRIGHT_F1 value)
1	0	0	LED fully on (output low). Can be used as general-purpose output
1	0	1	LED on at brightness set by One Shot / Master Intensity register
1	1	0	LED blinking with intensity characteristics of BANK0 (PWM0)
1	1	1	LED blinking with intensity characteristics of BANK1 (PWM1)

Table 5. Register 0 (Select0 Register)

BIT	S0-7	S0-6	S0-5	S0-4	S0-3	S0-2	S0-1	S0-0
DEFAULT	X(1)	0	0	0	0	0	0	0

(1) X = Don't care

Table 6. Register 1 (Select1 Register)

BIT	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1	S1-0
DEFAULT	X(1)	0	0	0	0	0	0	0

(1) X = Don't care

Table 7. Register 2 (Select2 Register)

BIT	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1	S1-0
DEFAULT	X(1)	0	0	0	0	0	0	0

(1) X = Don't care

To use a P port as a general-purpose output, Select1 and Select0 registers must be set low (or 0), then the inverse of the data written to the Select2 bit appears on the open-drain output.

The intensity of each bank of LEDs can be customized by programming six registers: Fade-On Time, Fully-On Time, Fade-Off Time, First Fully-Off Time, Second Fully-Off Time, and Maximum Intensity registers. Each bank is designed to produce two identical intensity pulses per blink cycle. Both pulses have the same fade-on, fully-on and fade-off times, but independent fully-off times to achieve a double-blink effect when desired.

The Fade-On Time register (register 3) defines the time from the fully-off state to the fully-on state for the LED per region A in Figure 7. The first four bits (C7–C4) in this register set the fade-on time for BANK1, and the next four bits (C3–C0) set the fade-on time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the least significant bit (LSB) is bit C4. For BANK0, the MSB is bit C3 while the LSB is bit C0. See Table 13 for more information.

Table 8. Register 3 (Fade-On Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The Fully-On Time register (register 4) defines the time spent at maximum intensity between the fade-on state and fade-off state for the LED per region B in Figure 7. The first four bits (C7–C4) in this register set the fully-on time for BANK1, and the next four bits (C3–C0) set the fully-on time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the most significant bit (MSB) is bit C3, while the LSB is bit C0. See Table 13 for more information.

Table 9. Register 4 (Fully-On Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The Fade-Off Time register (register 5) defines the time from the fully-on state to the fully-off state for the LED per region C in Figure 7. The first four bits (C7–C4) in this register set the fade-off time for BANK1, and the next four bits (C3–C0) set the fade-off time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the MSB is bit C3, while the least significant bit (LSB) is bit C0. See Table 13 for more information.

Table 10. Register 5 (Fade-Off Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

The first and second Fully-Off Time registers (registers 6 and 7) define the time spent at zero intensity (in the fully-off state of the LED) per region D and E, respectively, in Figure 7. The first four bits (C7–C4) in this register set the fully-off time for BANK1, and the next four bits (C3–C0) set the fully-off time for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the MSB is bit C3, while the LSB is bit C0. See Table 13 for more information.

Table 11. Register 6 (First Fully-Off Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

Table 12. Register 7 (Second Fully-Off Time Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	0	1	0	0	0	1	0	0

Table 13. Time Parameters

CODE	TIME (ms)
0	0
1	64
2	128
3	192
4 (default)	256
5	384
6	512
7	768
8	1024
9	1536
10	2048
11	3072
12	4096
13	5760
14	8128
15	16320

The Maximum Intensity register (register 8) defines the duty cycle of the waveform driving the LED in its fully-on state per region F in Figure 7. The first four bits (C7–C4) in this register set the duty cycle for BANK1 and the next four bits (C3–C0) set the duty cycle for BANK0. The data for each bank is a binary number between 0 and 15. For BANK1, the MSB is bit C7, while the LSB is bit C4. For BANK0, the MSB is bit C3, while the LSB is bit C0. The values in this register also define the LED intensity indicated by the BRIGHT_F0 or BRIGHT_F1 modes. The intensity of each LED is updated 125 times per second (every 8 ms with a 32-kHz clock).

Table 14. Register 8 (Maximum Intensity Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

Table 15. Intensity Parameters (see Figure 7)

REGION	PARAMETER NAME	PARAMETER RANGE	REGISTER RANGE	REGISTER NAME	REGISTER
A1, A2	Fade-on time	0 to 16320 ms (exponential trend)	0 to 15	Fade-On Time	2
B1, B2	Fully-on time	0 to 16320 ms (exponential trend)	0 to 15	Fully-On Time	3
C1, C2	Fade-off time	0 to 16320 ms (exponential trend)	0 to 15	Fade-Off Time	4
D	First fully-off time	0 to 16320 ms (exponential trend)	0 to 15	First Fully-Off Time	5
E	Second fully-off time	0 to 16320 ms (exponential trend)	0 to 15	Second Fully-Off Time	6
F	Maximum intensity	0 to 100%	0 to 15	Maximum Intensity	7

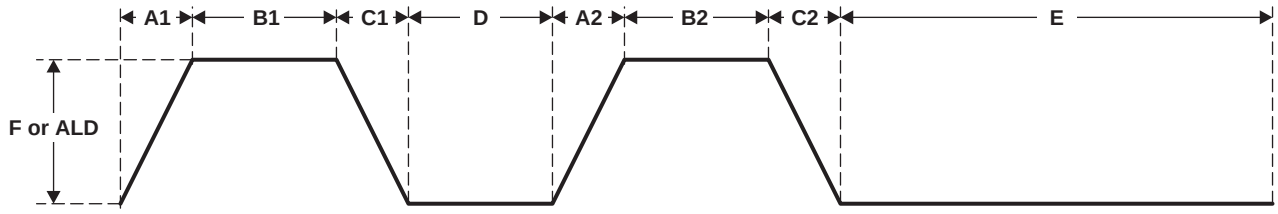


Figure 7. LED Intensity Per Bank

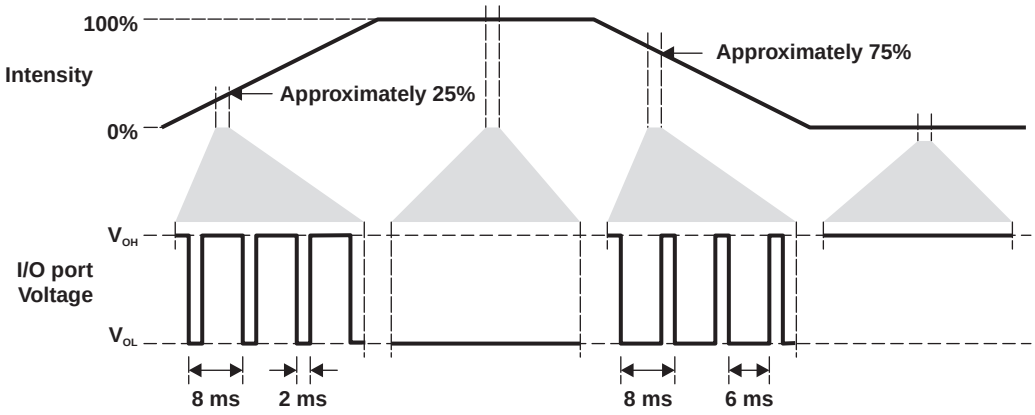


Figure 8. Output Port Voltage vs LED Intensity, Maximum Intensity = 100%

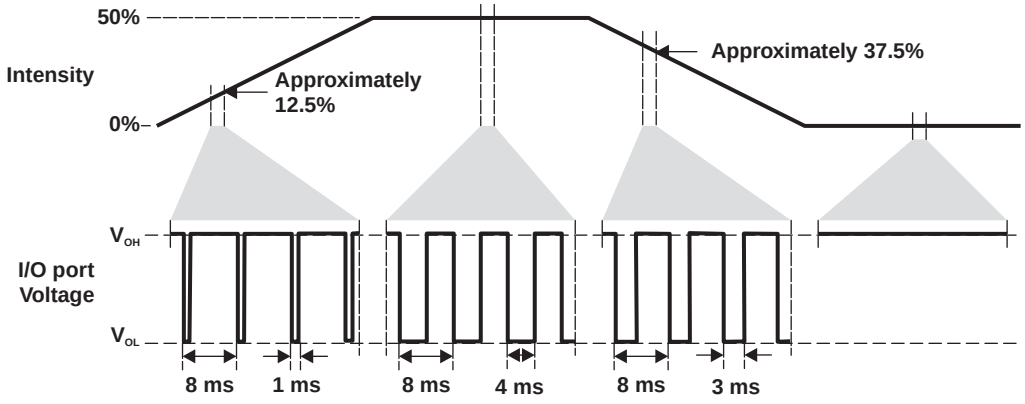


Figure 9. Output Port Voltage vs LED Intensity, Maximum Intensity = 50%

The One-Shot / Master Intensity register (register 9) (see Table 16) is an 8-bit register with three functions.

Bits 0–3 set the master intensity value (ALD). It is a binary number between 0 and 15.

Bits 4–5 determine whether the maximum intensity of PWM0 and PWM1 is set by the programmed F value (BRIGHT_F0 or BRIGHT_F1) or the master ALD value. The default value for these bits is 0. Bit 4 supports PWM0 and bit 5 is for PWM1. If bit 4 (or bit 5) is 0, the maximum intensity value for PWM0 (or PWM1) is set by the F value. If bit 4 (or bit 5) is 1, the maximum intensity value for PWM0 (or PWM1) is set by the master ALD value. This allows the user to vary the brightness of all LEDs by changing a single register.

Bits 6–7 determine whether each PWM operates in normal or one-shot mode. Bit 6 supports PWM0 and bit 7 is for PWM1. If bit 6 (or bit 7) is 0, PWM0 (or PWM1) operates in the normal mode where the LEDs goes through the full intensity cycle defined by Table 15 and Figure 7. If bit 6 (or bit 7) is 1, PWM0 (or PWM1) operate in the one-shot mode. In this mode, the LEDs can be used to create a single-shot lighting effect where the LED intensity is valid for a particular segment of the cycle shown in Table 15 and Figure 7.

Table 16. One-Shot / Master Intensity Register

BIT	DESCRIPTION
0–3	Master intensity (ALD) value. Valid values are 0 to 15.
4	Determines whether maximum intensity of PWM0 is set by the programmed F value or the master ALD value 0 = F value 1 = ALD value
5	Determines whether maximum intensity of PWM1 is set by the programmed F value or the master ALD value 0 = F value 1 = ALD value
6	Determines if PWM0 operates in normal or one-shot mode 0 = Normal mode 1 = One-shot mode
7	Determines if PWM1 operates in normal or one-shot mode 0 = Normal mode 1 = One-shot mode

The Initialization register (register 10) determines whether to initialize each PWM and, if so, provides the starting point of the LED intensity cycle for each bank. Bits 0–3 (C0–C3) are for BANK0 and bits 4–7 (C4–C7) are for BANK1.

Bits 0–2 provide the starting point for PWM0. If bit 3 is high (or 1), it initializes PWM0.

Bits 4–6 provide the starting point for PWM1. If bit 7 is high (or 1), it initialized PWM1.

In the one-shot mode for BANK0, the LEDs start at the beginning of the region defined by C2, C1, and C0 in the Initialization register and, when it reaches the end of that region, the LED stays at that intensity level defined at the end of the region. When the stop point is reached, all P ports attached to PWM0 disconnect from PWM0 and stay at either the maximum intensity level for PWM0 (BRIGHT_F0 or ALD value) or the OFF state. The bits in the Select2 and Select1 registers change to reflect the final state of the LED at that time. PWM0 continues running and is free to be used by other LEDs. The one-shot mode works similarly for BANK1.

Upon writing to this register, each bank is initialized to the state listed in Table 18 and Table 19.

Table 17. Register 10 (Initialization Register)

BANK	BANK1				BANK0			
BIT	C7	C6	C5	C4	C3	C2	C1	C0

Table 18. BANK1

C6	C5	C4	INTENSITY CYCLE
0	0	0	Beginning at region A1 in Table 15 and Figure 6
0	0	1	Beginning at region B1 in Table 15 and Figure 6
0	1	0	Beginning at region C1 in Table 15 and Figure 6
0	1	1	Beginning at region D in Table 15 and Figure 6
1	0	0	Beginning at region A2 in Table 15 and Figure 6
1	0	1	Beginning at region B2 in Table 15 and Figure 6
1	1	0	Beginning at region C2 in Table 15 and Figure 6
1	1	1	Beginning at region E in Table 15 and Figure 6

Table 19. BANK0

C2	C1	C0	STARTING POINT OF INTENSITY CYCLE
0	0	0	Beginning at region A1 in Table 15 and Figure 6
0	0	1	Beginning at region B1 in Table 15 and Figure 6
0	1	0	Beginning at region C1 in Table 15 and Figure 6
0	1	1	Beginning at region D in Table 15 and Figure 6
1	0	0	Beginning at region A2 in Table 15 and Figure 6
1	0	1	Beginning at region B2 in Table 15 and Figure 6
1	1	0	Beginning at region C2 in Table 15 and Figure 6
1	1	1	Beginning at region E in Table 15 and Figure 6

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA6507 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released, and the TCA6507 registers and I^2C/SMBus state machine initialize to their default states.

After the initial power-up phase, V_{CCI} must be lowered to below 0.2 V and then back up to the operating voltage (V_{CCI}) for a power-reset cycle.

Enable and Reset

If the enable (EN) input is set to low, the TCA6507 is put in the standby or shutdown mode. In this mode, the oscillator is turned off, the registers are returned to their default state, and the the I^2C/SMBus state machine is initialized. This mode is useful for low power consumption. An internal filtering circuit prevents negative glitches from accidentally shutting down the device. EN must be low for a minimum of approximately 60 μs to ensure a shutdown state.

The system master can reset the TCA6507 in the event of a timeout or other improper operation by setting EN low for a minimum of approximately 60 μs. This has the same effect as a power-on reset without depowering the TCA6507.

The oscillator start up time (t_{OSC}) is measured from the point when EN is set high.

Bus Transactions

Data is exchanged between the master and TCA6507 through read and write commands.

Reads

The bus master first must send the TCA6507 address with the LSB set to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA6507 (see Figure 10). Data is clocked into the register on the rising edge of the ACK clock pulse.

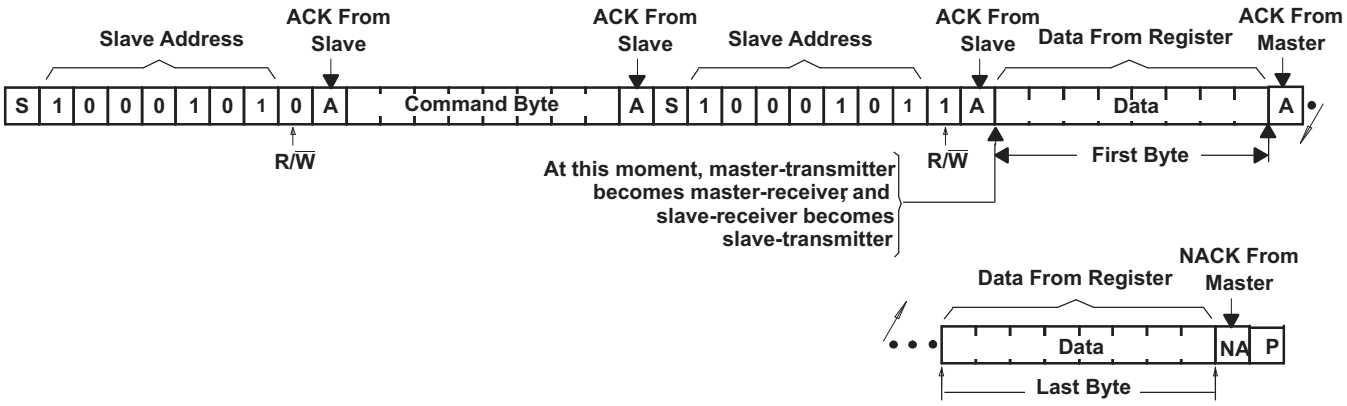


Figure 10. Read From Register

Writes

Data is transmitted to the TCA6507 by sending the device address and setting the LSB to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 11 through Figure 13).

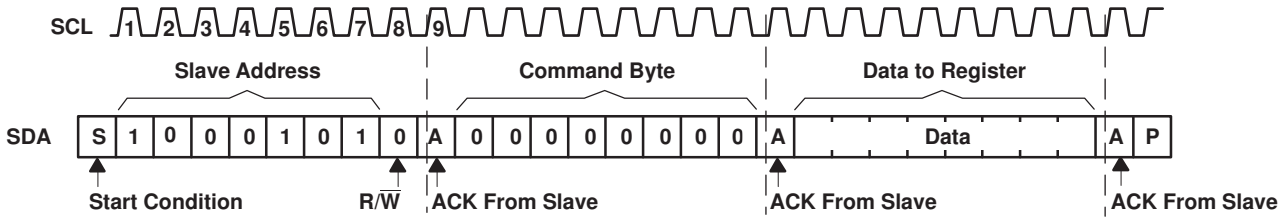


Figure 11. Write to Select0 Register

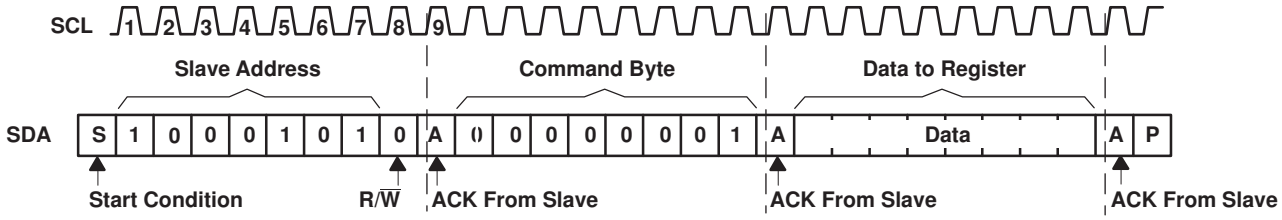


Figure 12. Write to Select1 Register

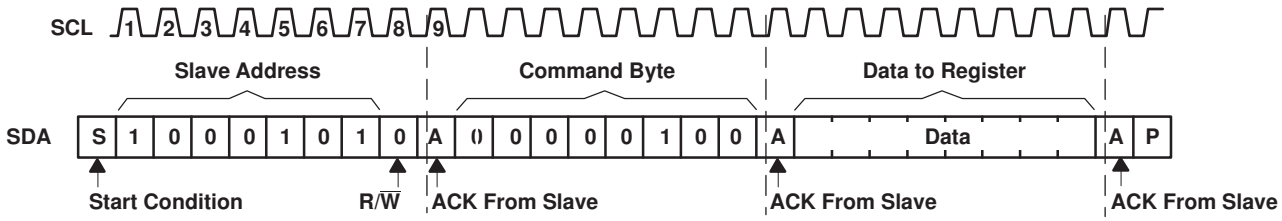


Figure 13. Write to Fully-On Time Register

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage range			–0.5	4.6	V
V_I	Input voltage range(2)			–0.5	6.5	V
V_O	Output voltage(2)				6.5	V
I_{IK}	Input clamp current	$V_I < 0$	SCL, EN		±20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	P port, SDA		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}	P port		50	mA
			SDA		25	
I_{CC}	Continuous current through GND				250	mA
	Continuous current through V_{CC}				20	
θ_{JA}	Package thermal impedance(3)		PW package		112.6	°C/W
			RUE package		128	
			ZXU package		TBD	
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage of I²C registers, oscillator, and control logic			1.65	3.6	V
V_{IH}	High-level input voltage	SCL, SDA, EN	1.65 V ≤ V_{CC} ≤ 1.95 V	1.3	3.6	V
			1.96 V ≤ V_{CC} ≤ 3.6 V	0.7 × V_{CC}	3.6	
V_{IL}	Low-level input voltage	SCL, SDA, EN	1.65 V ≤ V_{CC} ≤ 1.95 V	–0.5	0.3	V
			1.96 V ≤ V_{CC} ≤ 3.6 V	–0.5	0.3 × V_{CC}	
V_O	Output voltage			0	5.5	V
I_{OL}	Low-level output current (1)				40	mA
T_A	Operating free-air temperature			–40	85	°C

(1) The total current sourced by the P port must be limited to 200 mA.

Electrical Characteristics

GND = 0 V, T_A = –40°C to 85°

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
f_{INT}	Intensity control clock frequency	Operating mode	1.65 V to 3.6 V	23	32	43	kHz
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 3.6 V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, I_O = 0	1.65 V to 3.6 V		1.4		V
V_{OL}	SDA	I_{OL} = 6 mA	1.65 V to 3.6 V		0.2	0.6	V
I_{OL}	SDA		1.65 V to 3.6 V	3	13.2		mA
	P port(2)	V_{OL} = 0.5 V	1.65 V	25	59.7		
		V_{OL} = 0.6 V	1.8 V to 3.6 V	40	68		
I_I	SCL, SDA, EN	$V_I = V_{CC}$ or GND	1.65 V to 3.6 V			±0.1	µA
I_{CC}	Standby current	EN disabled, P port idle, Intensity control disabled, SCL = V_{CC}, SDA = V_{CC}, I_O = 0, f_{SCL} = 0	1.65 V to 1.95 V		2	12	µA
			1.96 V to 3.6 V		3	15	
	Operating mode	P port running, Intensity control enabled, SCL = V_{CC}, SDA = V_{CC}, I_O = 0, f_{SCL} = 0	1.65 V to 1.95 V		9.7	17	
			1.96 V to 3.6 V		10.4	20	
		P port running, Intensity control enabled, SDA = V_{CC}, I_O = 0, f_{SCL} = 400 kHz	1.65 V to 1.95 V		10.2	18	
			1.96 V to 3.6 V		11.4	25	
C_i	SCL		1.65 V to 3.6 V			7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	1.65 V to 3.6 V			8	pF
C_o	P port	$V_O = V_{CC}$ or GND	1.65 V to 3.6 V			10	pF

(1) All typical values are at T_A = 25°C.
(2) The total current sourced by the P port must be limited to 200 mA.

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 14)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	250	ns
t_{buf}	I²C bus free time between Stop and Start conditions		4.7		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		4.7		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		4		0.6		µs
t_{sps}	I²C Stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid-data time	SCL low to SDA output valid		1		1	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1		1	µs
C_b	I²C bus capacitive load		0	400	0	400	pF

(1) C_b = total capacitance of one bus line in pF

Oscillator Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_{OSC}	Oscillator start-up time from powerdown or shutdown mode to fully on at 32 kHz	5		5		ms

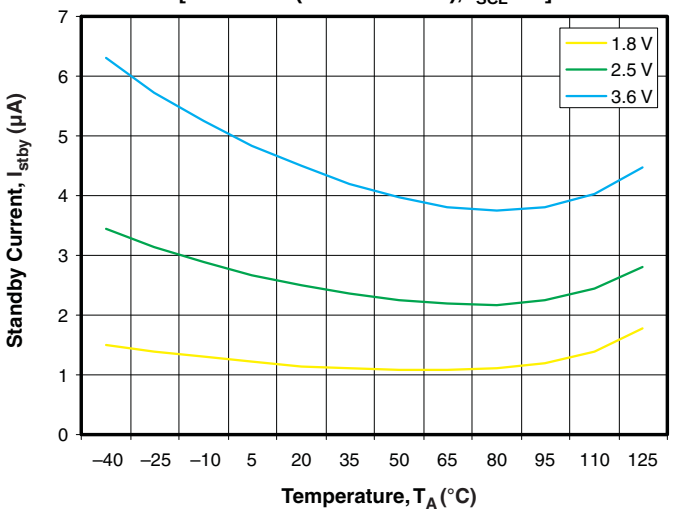
Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted)

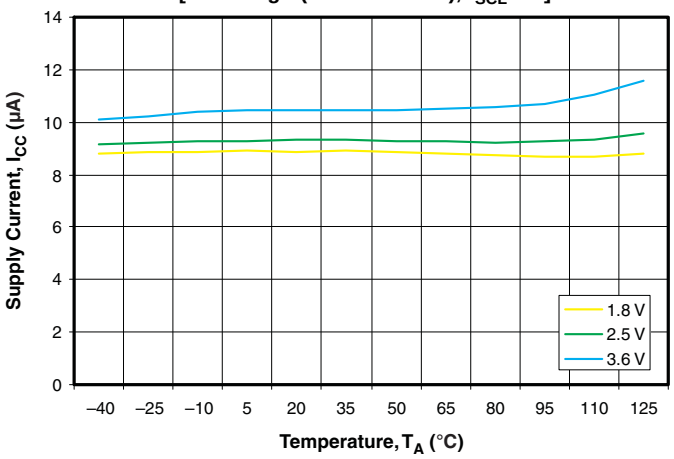
PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{pv}	Output data valid (in general-purpose output mode)	SCL	P port		400		400	ns
t_{ps}	Shutdown data valid	EN (low)	P port (high)		60		60	µs
t_w	EN pulse duration			60		60		µs

TYPICAL CHARACTERISTICS

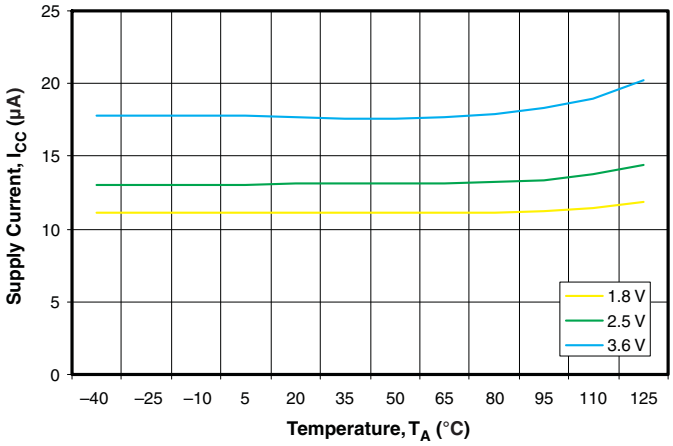
STANDBY CURRENT vs TEMPERATURE [EN is Low (PWM Disabled), f_{SCL} = 0]



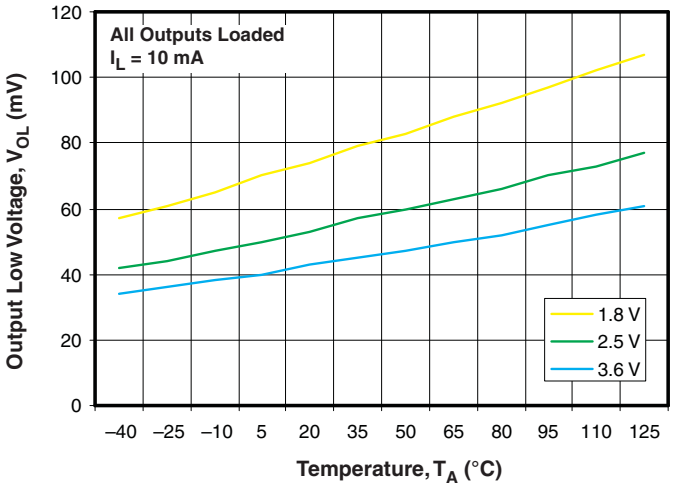
SUPPLY CURRENT vs TEMPERATURE [EN is High (PWM Enabled), f_{SCL} = 0]



SUPPLY CURRENT vs TEMPERATURE [EN is High (PWM Enabled), f_{SCL} = 400 kHz]

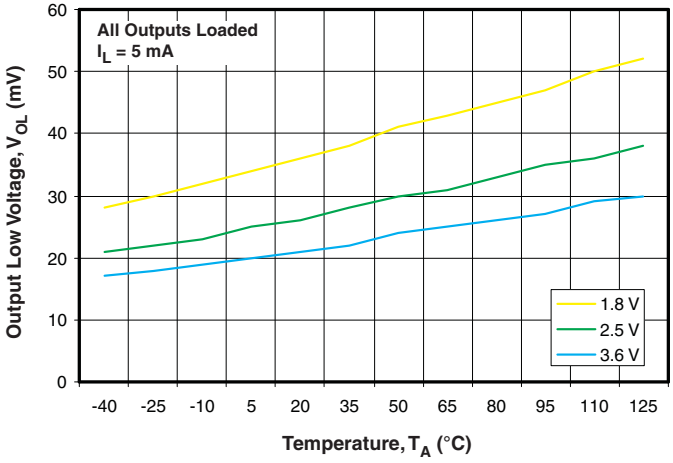


PORT OUTPUT LOW VOLTAGE vs TEMPERATURE

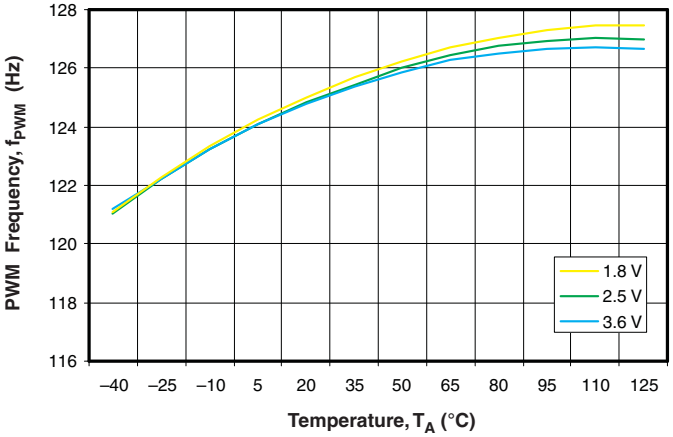


TYPICAL CHARACTERISTICS (continued)

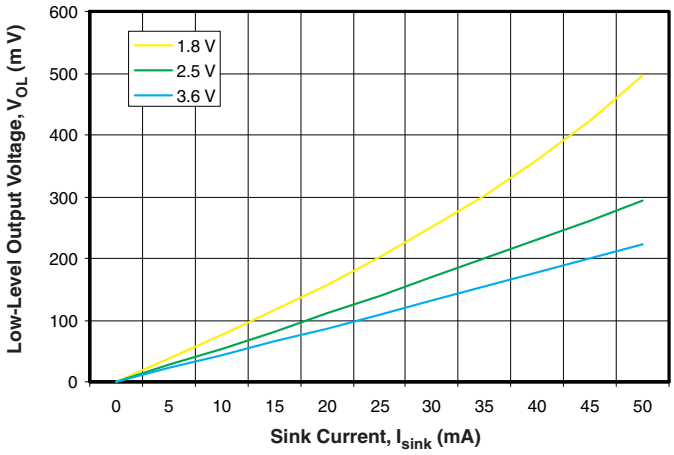
PORT OUTPUT LOW VOLTAGE vs TEMPERATURE



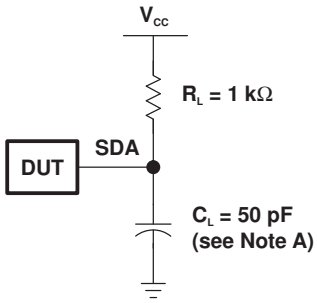
PWM FREQUENCY vs TEMPERATURE



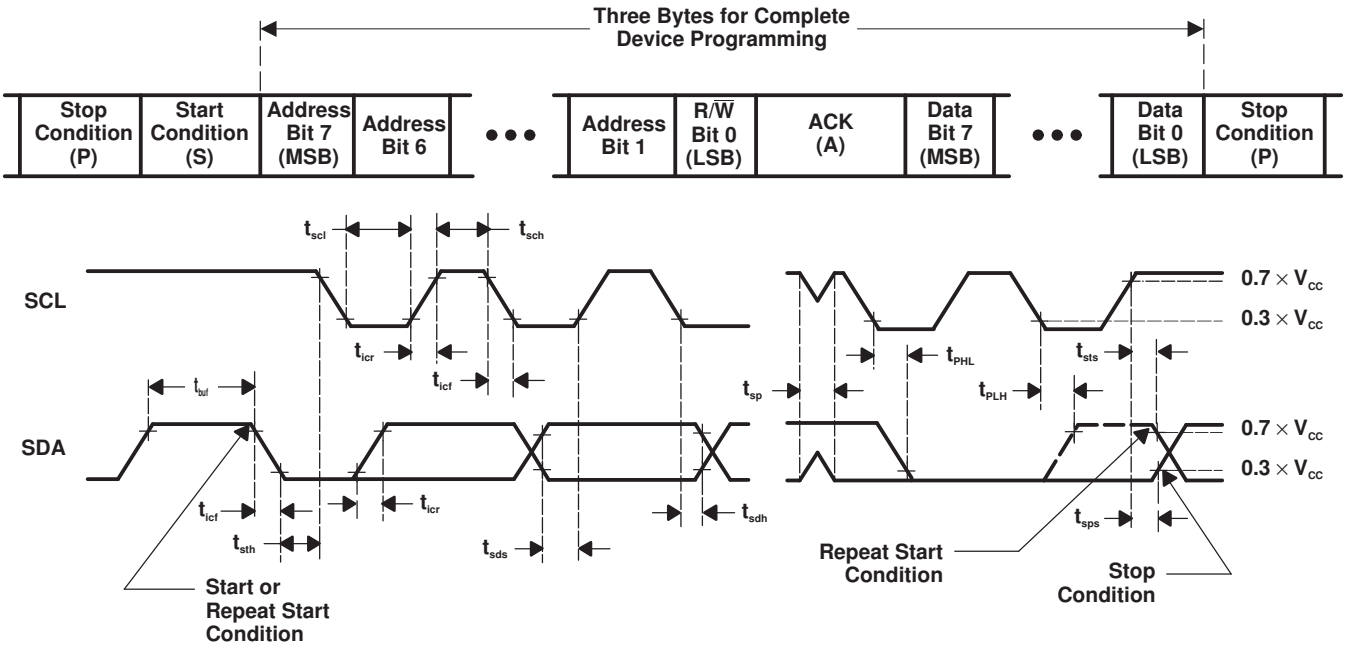
OUTPUT LOW VOLTAGE vs SINK CURRENT



PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2	Command
3	P-port data

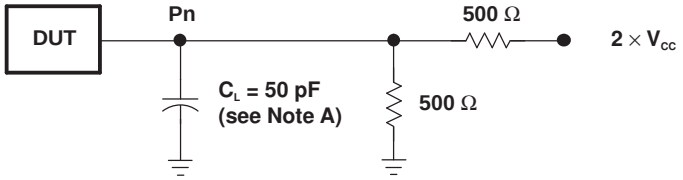
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

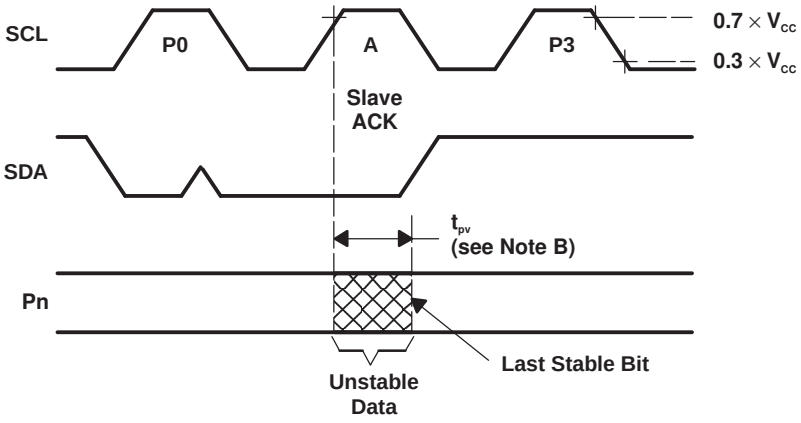
C. All parameters and waveforms are not applicable to all devices.

Figure 14. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. All parameters and waveforms are not applicable to all devices.

Figure 15. P-Port Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 16 shows a general application in which the TCA6507 can be used. Each LED output is driving one LED. Figure 16 highlights another application where the TPS61052 boost converter and high-power LED driver and TCA6507 7-bit LED driver can be used in combination for applications requiring flashlight functionality and/or high-brightness indicator/backlight LEDs.

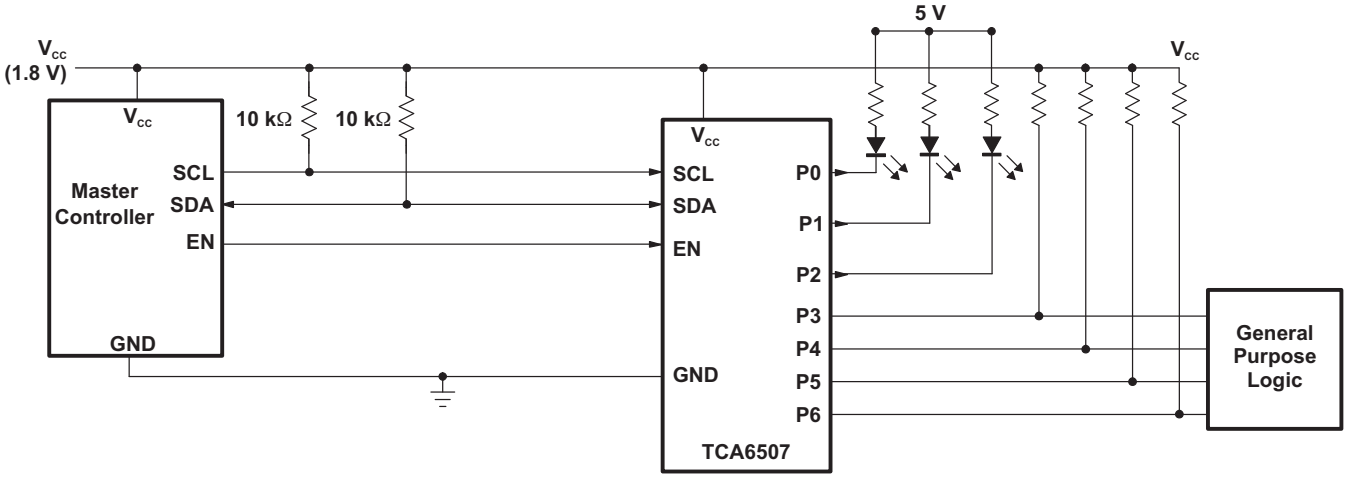


Figure 16. Typical Application

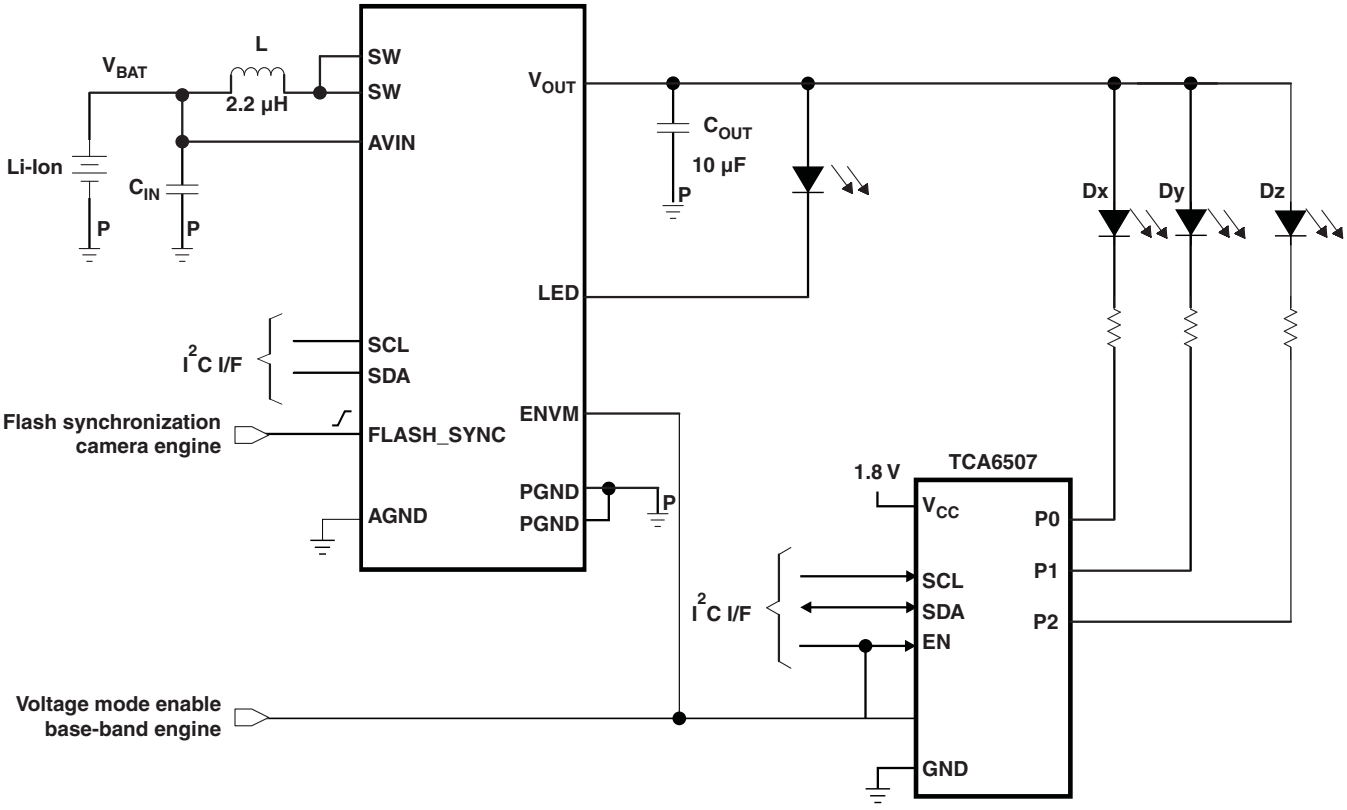


Figure 17. White LED Flashlight Driver and High-Brightness LED Indicator/Backlight Power Supply

SOFTWARE CONSIDERATIONS FOR USING THE TCA6507

Operation

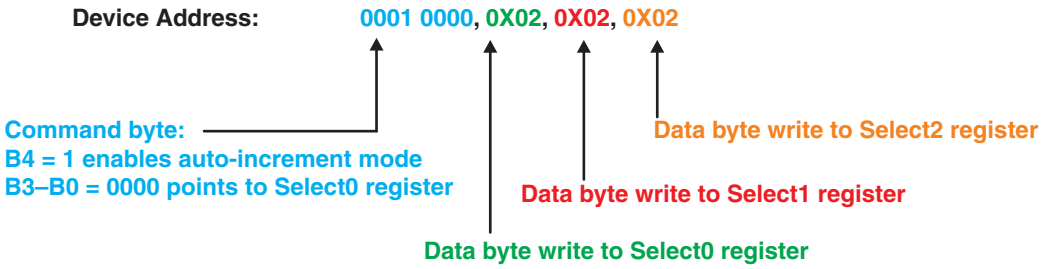
The TCA6507 includes 11 registers that control the LED function and intensity. In general, the TCA6507 needs to be operated/written this way to run LEDs (see Figure 11).

1. Master sends a START condition.
2. Master sends the slave address with a write operation (1000 1010).
3. Master sends a command byte that points 1 of the 11 registers in this device.
4. Master sends data to the TCA6507 register(s).

If auto-increment mode is used, the master can write to all 11 registers with 1 command byte being sent initially. After all registers are written to (if needed), LEDs operate after the TCA6507 acknowledges the master's command.

Auto-Increment Mode

In auto-increment mode, the last four bits of the command byte are automatically incremented after the byte is written and the next data byte is stored in the corresponding register.



The registers are written to in the order shown in Table 3.

LED Operation

For LED states, see Figure 1 and Table 4.

It is the combination of Select2, Select1, and Select0 registers that gives the state of the LED or Px.

Bit 0 from the Select0 register, bit = 0 from Select1 register and bit=0 from the Select2 register provide the state for P0 or the first LED. Similarly, bit = 1 from the Select0 register, bit 1 from Select1 register and bit = 1 from the Select2 register provide the state for P1 or the second LED (see Table 20).

Table 20. LED Operation

	MSB							LSB
Select0	X	0	0	0	0	0	0	0
Select1	X	0	0	0	0	0	0	0
Select2	X	0	0	0	0	0	0	0
Output or LED affected	X X	P6 7th LED	P5 6th LED	P4 5th LED	P3 4th LED	P2 3rd LED	P1 2nd LED	P0 1st LED

Example of LED Operation

Starting with a powerup/reset and all seven LEDs off, the following is an example of LED operationg(using auto-increment):

<start>, ...,	<slave addr>,	<command with auto-increment>,	<data>,	<data>,	<data>,	<stop>
Start,	1000 1010,	0001 0000,	0X02,	0X02,	0X02,	Stop

A command byte of 0001 0000 writes first to the Select0 register. Data written is 0000 0010. Since auto-increment is enabled, the next data byte goes into Select1 and Select2 registers, respectively (see Table 21).

Table 21. LED Operation Example

	MSB							LSB
Select0	X	0	0	0	0	0	1	0
Select1	X	0	0	0	0	0	1	0
Select2	X	0	0	0	0	0	1	0
Output or LED affected	X X	P6 7th LED	P5 6th LED	P4 5th LED	P3 4th LED	P2 3rd LED	P1 2nd LED	P0 1st LED

For P1 or the second LED, the combination of 1 for the Select0 register (Bit 1), 1 for the Select1 register bit (bit 1), and 1 for the Select2 register bit (bit 1) puts the LED in a state where it blinks with intensity characteristic of BANK1 (PWM1) (see Table 4).

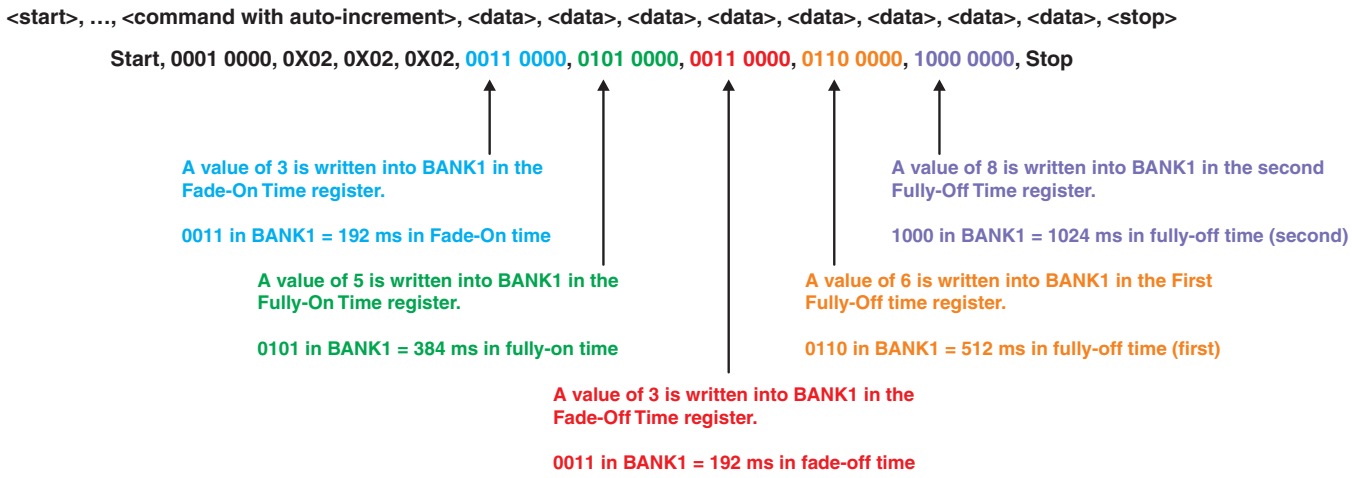
Blink Control

The Fade-On time, Fully-On time, Fade-Off time, First Fully-Off time, and Second Fully-Off time registers must be written to for basic blink control. Each of these registers has eight bits – top four bits for BANK1 (or PWM1) and bottom four bits for BANK0 (or PWM0) (see Table 17).

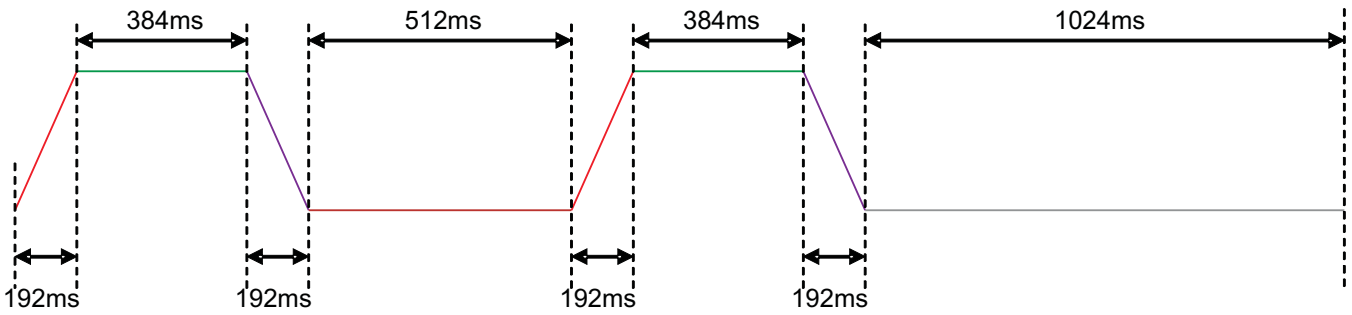
Each BANK or PWM has a default value of 4 (0100), which translates to a time of 256 ms. The largest value for each BANK or PWM is 15 (1111), which translates to a time of 16320 ms (see Figure 7 and Table 15).

Example of Blink Control

Starting with a powerup/reset and all seven LEDs off, here is an example (using auto-increment):



This sets the blink cycle as such for PWM1 or BANK1:



Intensity Control

The Maximum Intensity registers must be written to for setting the intensity of the LED. This register has eight bits – top four bits for BANK1 (or PWM1) and bottom four bits for BANK0 (or PWM0). This register can be written to after sending data to the Second Fully-Off Time register (see Table 17).

The Maximum Intensity register has a default value of 15 (1111), which translates to 100% brightness (see Figure 7 and Table 15).

Examples of Intensity Control

The intensity of the LED can be modified by changing the duty cycle of the output port voltage. The period is 8 ms. In Figure 8, 1111 0000 was written into the Maximum Intensity register to put a 100% intensity level in PWM1 or BANK1.

The user can vary the duty cycle of the output voltage for intensity changes:

- For 25% brightness, the voltage level at the output/LED should be LOW for 25% of the time (2 ms) and HIGH for 75% of the time (6 ms).
- For 75% brightness, the voltage level at the output/LED should be LOW for 75% of the time (6 ms) and HIGH for 25% of the time (2 ms).

In Figure 8, 0111 0000 was written into the Maximum Intensity register to put a 50% intensity level in PWM1 or BANK1. The period is 8 ms.

The user can vary the duty cycle of the output voltage for intensity changes:

- For 12.5% brightness, the voltage level at the output/LED should be LOW for 12.5% of the time (1 ms) and HIGH for 87.5% of the time (7 ms).
- For 37.5% brightness, the voltage level at the output/LED should be LOW for 37.5% of the time (3 ms) and HIGH for 62.5% of the time (5 ms)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA6507PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples
TCA6507RUER	ACTIVE	X2QFN	RUE	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2M	Samples
TCA6507ZXUR	ACTIVE	BGA MICROSTAR JUNIOR	ZXU	12	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	PH507	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

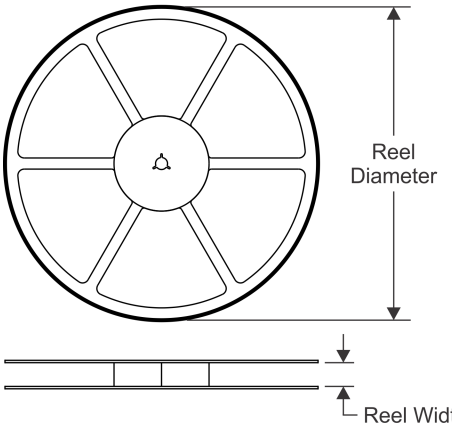
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

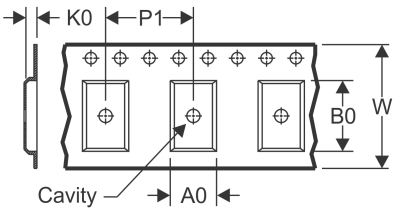
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

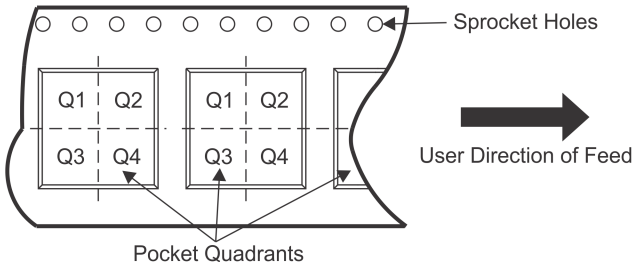


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

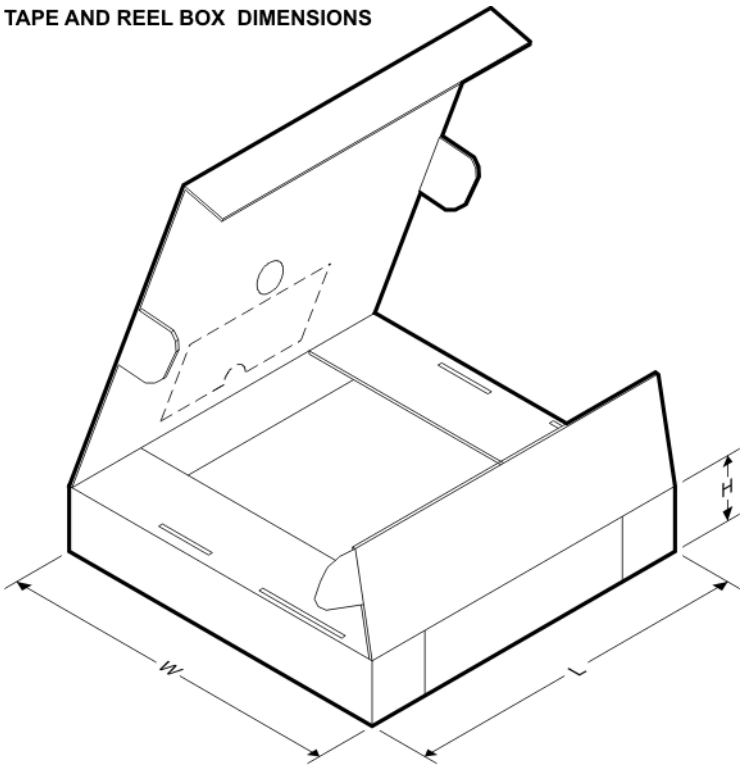
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA6507PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TCA6507RUER	X2QFN	RUE	12	3000	179.0	8.4	1.6	2.2	0.55	4.0	8.0	Q1
TCA6507ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2

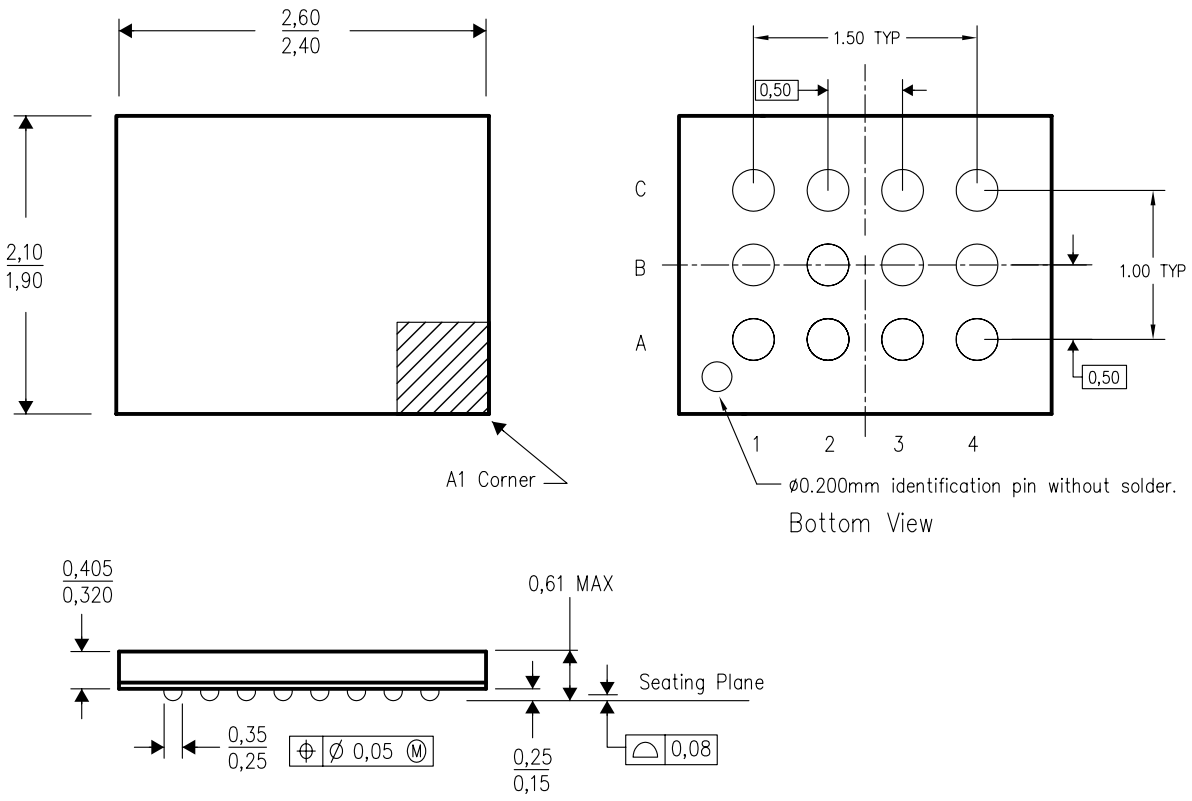
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA6507PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TCA6507RUER	X2QFN	RUE	12	3000	203.0	203.0	35.0
TCA6507ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	338.1	338.1	20.6

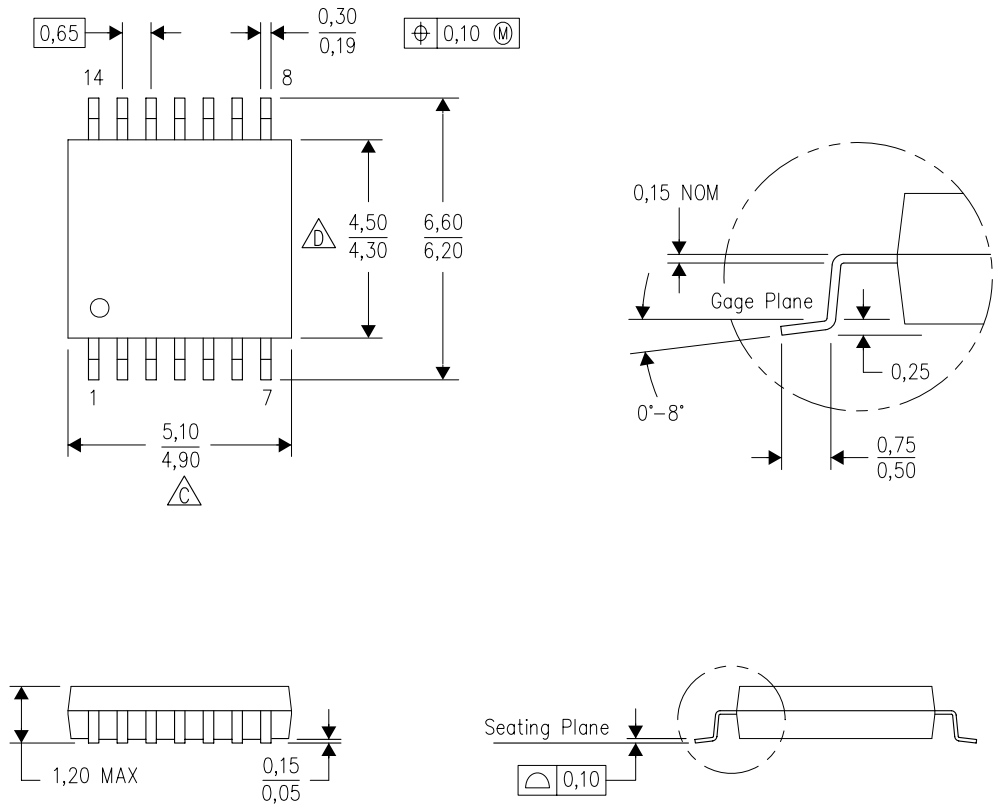
ZXU (S–PBGA–N12) PLASTIC BALL GRID ARRAY



4207009/B 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is a lead–free solder ball design.

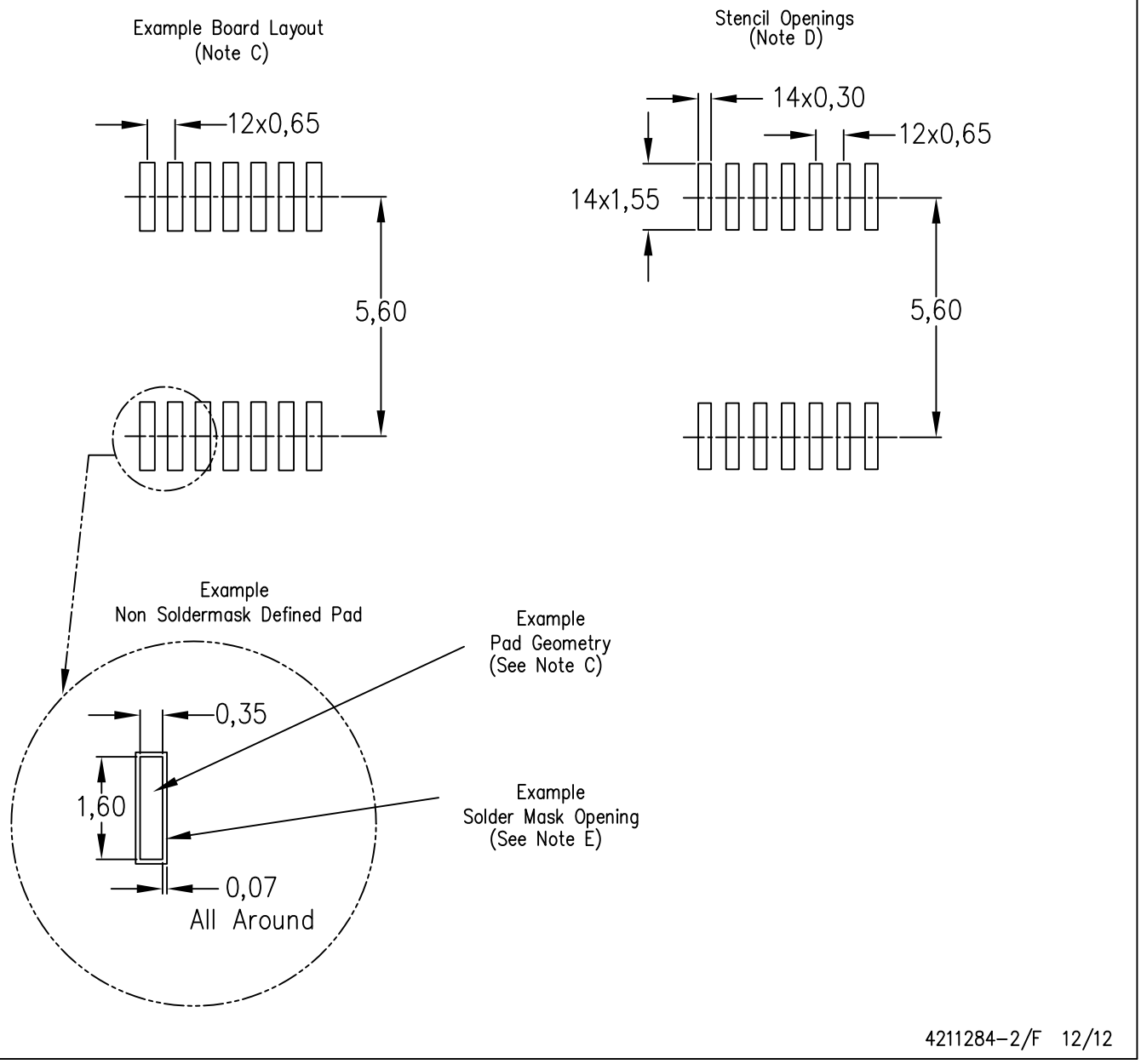
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

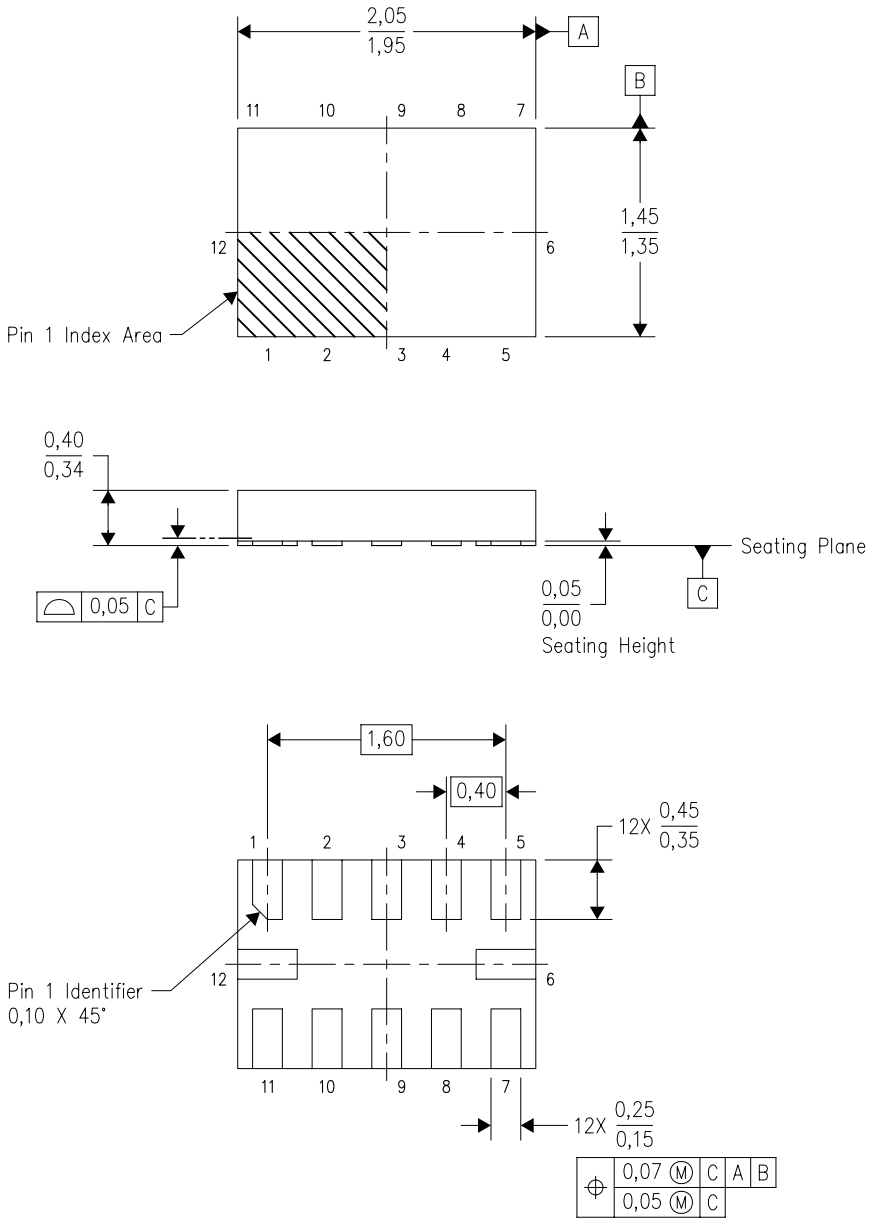
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUE (R–PX2QFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



4208463/C 07/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2DFE.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265