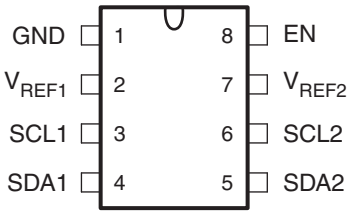
DUAL BIDIRECTIONAL I^2C BUS AND SMBus VOLTAGE-LEVEL TRANSLATOR

Check for Samples: PCA9306-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 2: –40°C to 105°C**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I^2C Applications**
- **I^2C and SMBus Compatible**
- **Less Than 1.5-ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I^2C Devices and Multiple Masters**
- **Allows Voltage-Level Translation Between**
  - **1.2-V V_{REF1} and 1.8-V, 2.5-V, 3.3-V, or 5-V V_{REF2}**
  - **1.8-V V_{REF1} and 2.5-V, 3.3-V or 5-V V_{REF2}**
  - **2.5-V V_{REF1} and 3.3-V or 5-V V_{REF2}**
  - **3.3-V V_{REF1} and 5-V V_{REF2}**
- **Provides Bidirectional Voltage Translation With No Direction Pin**
- **Low 3.5-Ω ON-State Connection Between Input and Output Ports Provides Less Signal Distortion**
- **Open-Drain I^2C I/O Ports (SCL1, SDA1, SCL2, and SDA2)**
- **5-V Tolerant I^2C I/O Ports to Support Mixed-Mode Signal Operation**
- **High-Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = Low**
- **Lock-Up-Free Operation for Isolation When EN = Low**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCU PACKAGE
(TOP VIEW)



PIN	SYMBOL	FUNCTION
1	GND	Ground, 0 V
2	V_{REF1}	Low-voltage-side reference supply voltage for SCL1 and SDA1
3	SCL1	Serial clock, low-voltage side. Connect to V_{REF1} through a pullup resistor.
4	SDA1	Serial data, low-voltage side. Connect to V_{REF1} through a pullup resistor.
5	SDA2	Serial data, high-voltage side. Connect to V_{REF2} through a pullup resistor.
6	SCL2	Serial clock, high-voltage side. Connect to V_{REF2} through a pullup resistor.
7	V_{REF2}	High-voltage-side reference supply voltage for SCL2 and SDA2
8	EN	Switch enable input. Connected to V_{REF2} and pulled up through a high resistor.

DESCRIPTION

This dual bidirectional I^2C and SMBus voltage-level translator, with an enable (EN) input, is operational from 1.2-V to 3.3-V V_{REF1} and 1.8-V to 5.5-V V_{REF2}.

The PCA9306 allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin. The low ON-state resistance (r_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In I^2C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9306 enables the system designer to isolate two halves of a bus; thus, more I^2C devices or longer trace length can be accommodated.

The PCA9306 also can be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

As with the standard I^2C system, pullup resistors are required to provide the logic high levels on the translator's bus. The PCA9306 has a standard open-collector configuration of the I^2C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I^2C devices, in addition to SMBus devices. Standard-mode I^2C devices only specify 3 mA in a generic I^2C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the drain pullup supply voltage (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less ESD-resistant devices.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

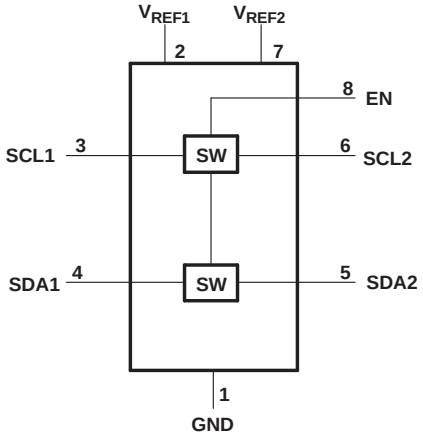
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTION TABLE

INPUT EN(1)	TRANSLATOR FUNCTION
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

(1) EN is controlled by the V_{REF2} logic levels and should be at least 1 V higher than V_{REF1} for best translator operation.

Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{REF1}	DC reference voltage range		–0.5	7	V
V_{REF2}	DC reference bias voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
$V_{I/O}$	Input/output voltage range(2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	V_I < 0		–50	mA
θ_{JA}	Package thermal impedance(3)			227	°C/W
T_{stg}	Storage temperature range		–65	150	°C
ESD	Electrostatic discharge rating	Human-body model H2		2	kV
		Charged-device model C4B		750	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	SCL1, SDA1, SCL2, SDA2	0	5	V
V_{REF1}	Reference voltage		0	5	V

Recommended Operating Conditions (continued)

		MIN	MAX	UNIT
V_{REF2}	Reference voltage	0	5	V
EN	Enable input voltage	0	5	V
I_{PASS}	Pass switch current		64	mA
T_A	Operating free-air temperature	–40	105	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA,	EN = 0 V				–1.2	V
I_{IH}	Input leakage current		V_I = 5 V,	EN = 0 V				5	µA
C_i(EN)	Input capacitance		V_I = 3 V or 0				11		pF
$C_{io(off)}$	Off capacitance	SCLn, SDAn	V_O = 3 V or 0,	EN = 0 V			4	6	pF
$C_{io(on)}$	On capacitance	SCLn, SDAn	V_O = 3 V or 0,	EN = 3 V			10.5	12.5	pF
r_{on} (2)	ON-state resistance	SCLn, SDAn	V_I = 0,	I_O = 64 mA	EN = 4.5 V		3.5	5.5	Ω
					EN = 3 V		4.7	7	
					EN = 2.3 V		6.3	9.5	
					EN = 1.5 V		25.5	32	
			V_I = 2.4 V,	I_O = 15 mA	EN = 4.5 V	1	6	15	
					EN = 3 V	20	60	140	
			V_I = 1.7 V,	I_O = 15 mA	EN = 2.3 V	20	60	140	

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two terminals.

AC PERFORMANCE (TRANSLATING DOWN)

Switching Characteristics

over recommended operating free-air temperature range, EN = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1		0.8		0.6		0.3	ns
t_{PHL}				1.2		1		0.5	

Switching Characteristics

over recommended operating free-air temperature range, EN = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1		1		0.7		0.4	ns
t_{PHL}				1.3		1		0.6	

AC PERFORMANCE (TRANSLATING UP)

Switching Characteristics

over recommended operating free-air temperature range, EN = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 2)

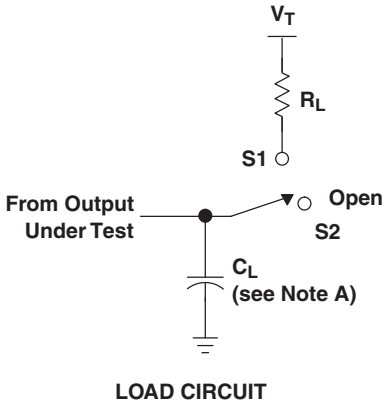
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2		0.9		0.6		0.4	ns
t_{PHL}				1.4		1.1		0.7	

Switching Characteristics

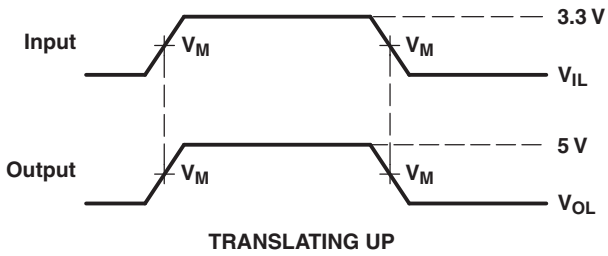
over recommended operating free-air temperature range, EN = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 2)

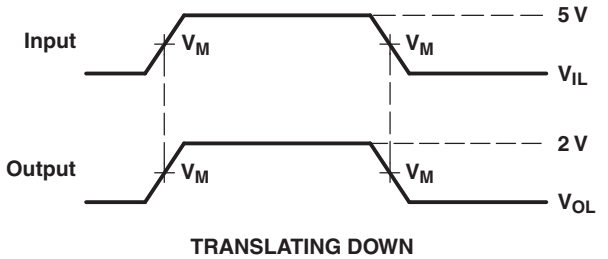
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2		1		0.6		0.4	ns
t_{PHL}				1.3		1.3		0.8	

PARAMETER MEASUREMENT INFORMATION



USAGE	SWITCH
Translating up	S1
Translating down	S2





NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit for Outputs

APPLICATION INFORMATION

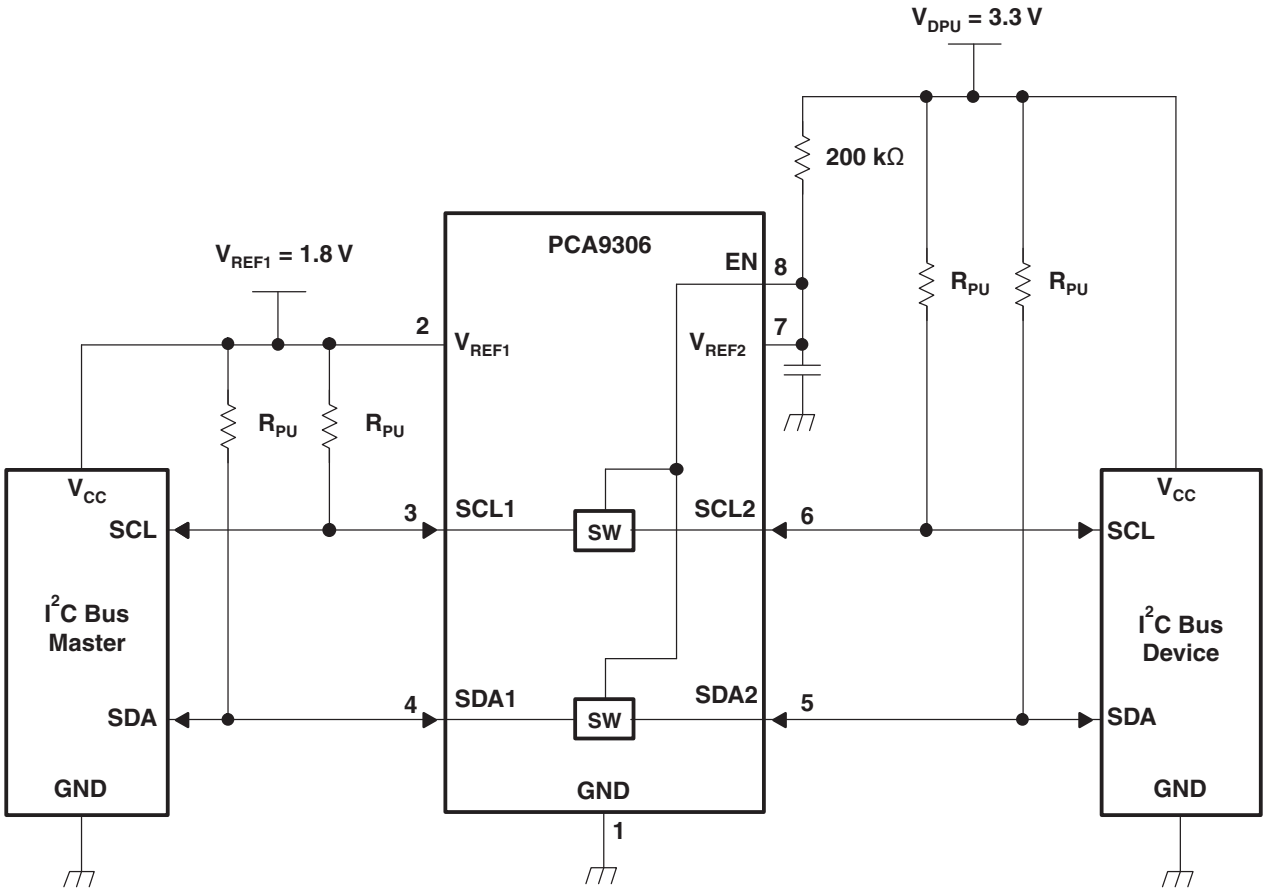


Figure 3. Typical Application Circuit (Switch Always Enabled)

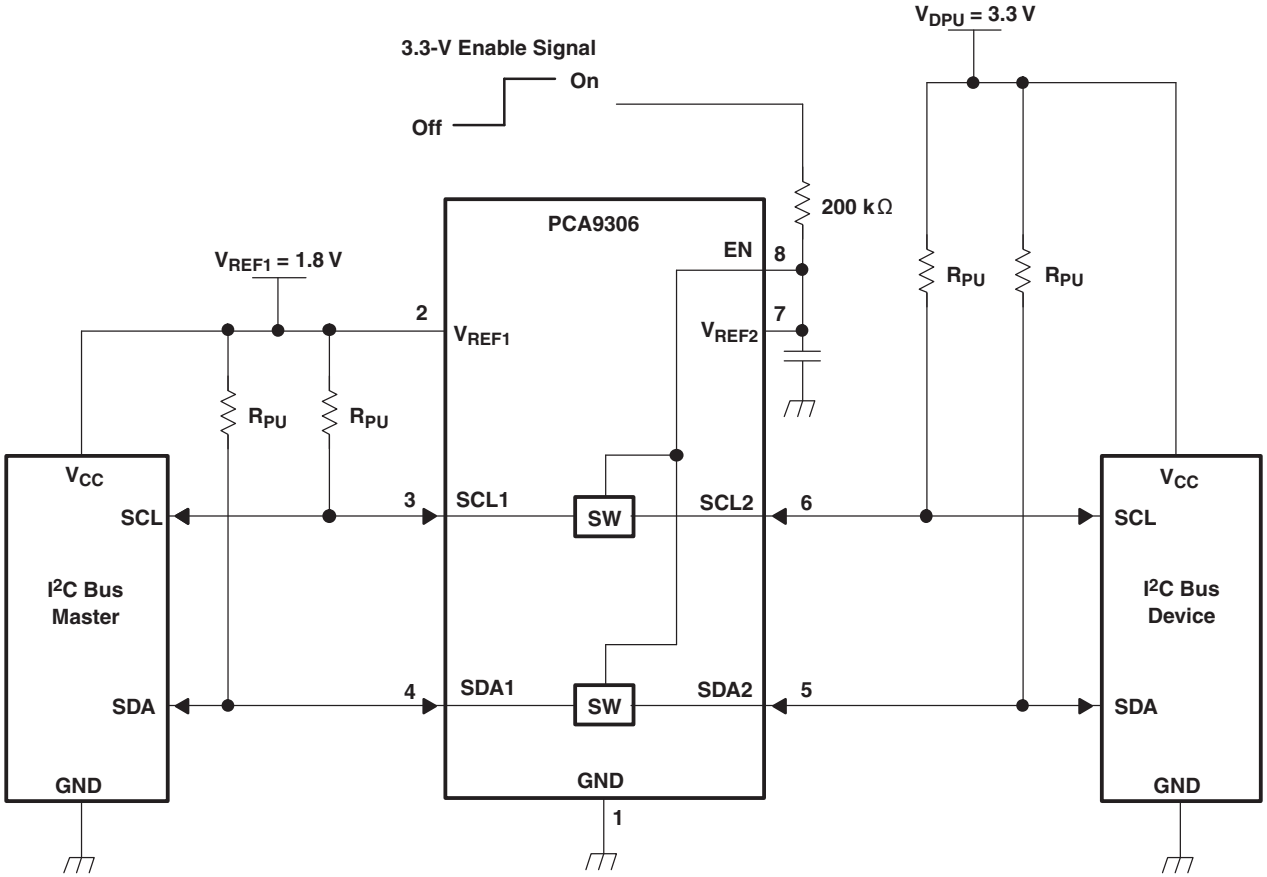


Figure 4. Typical Application Circuit (Switch Enable Control)

Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A filter capacitor on V_{REF2} is recommended. The I^2C bus master output can be totem pole or open drain (pullup resistors may be required) and the I^2C bus device output can be totem pole or open drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open drain, no direction control is needed.

The reference supply voltage (V_{REF1}) is connected to the processor core power-supply voltage.

Application Operating Conditions

see Figure 3

		MIN	TYP(1)	MAX	UNIT
V_{REF2}	Reference voltage	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	0	1.5	4.4	V
I_{PASS}	Pass switch current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	–40		105	°C

(1) All typical values are at T_A = 25°C.

Sizing Pullup Resistor

The pullup resistor value needs to limit the current through the pass transistor, when it is in the on state, to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35\ V}{0.015\ A}$$

The following table summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306 device at 0.175 V, although the 15 mA applies only to current flowing through the PCA9306 device.

PULLUP RESISTOR VALUES (1) (2)

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL	+10%(3)	NOMINAL	+10%(3)	NOMINAL	+10%(3)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCA9306IDCURQ1	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCUS	Samples
PCA9306TDCURQ1	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	YAAS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF PCA9306-Q1 :

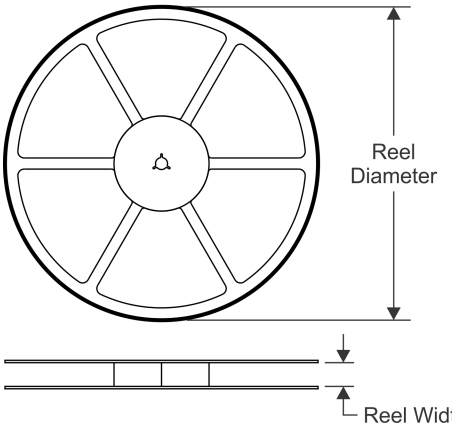
- Catalog: PCA9306

NOTE: Qualified Version Definitions:

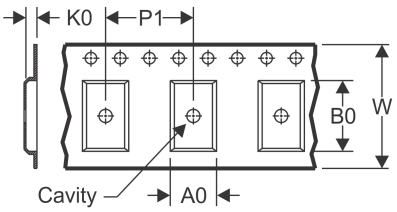
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

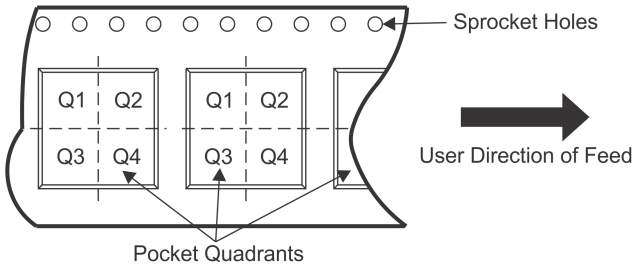


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

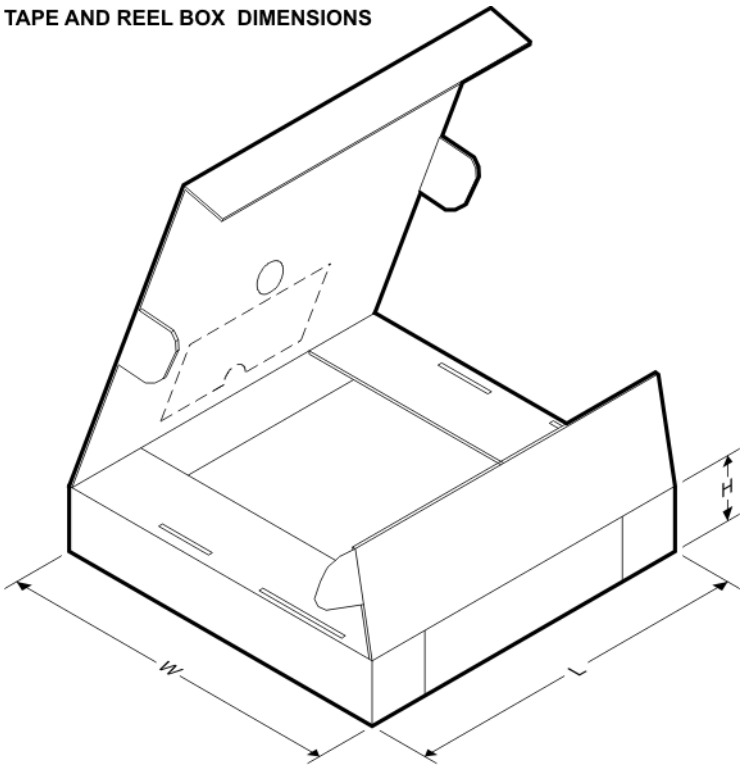
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9306IDCURQ1	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306TDCURQ1	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

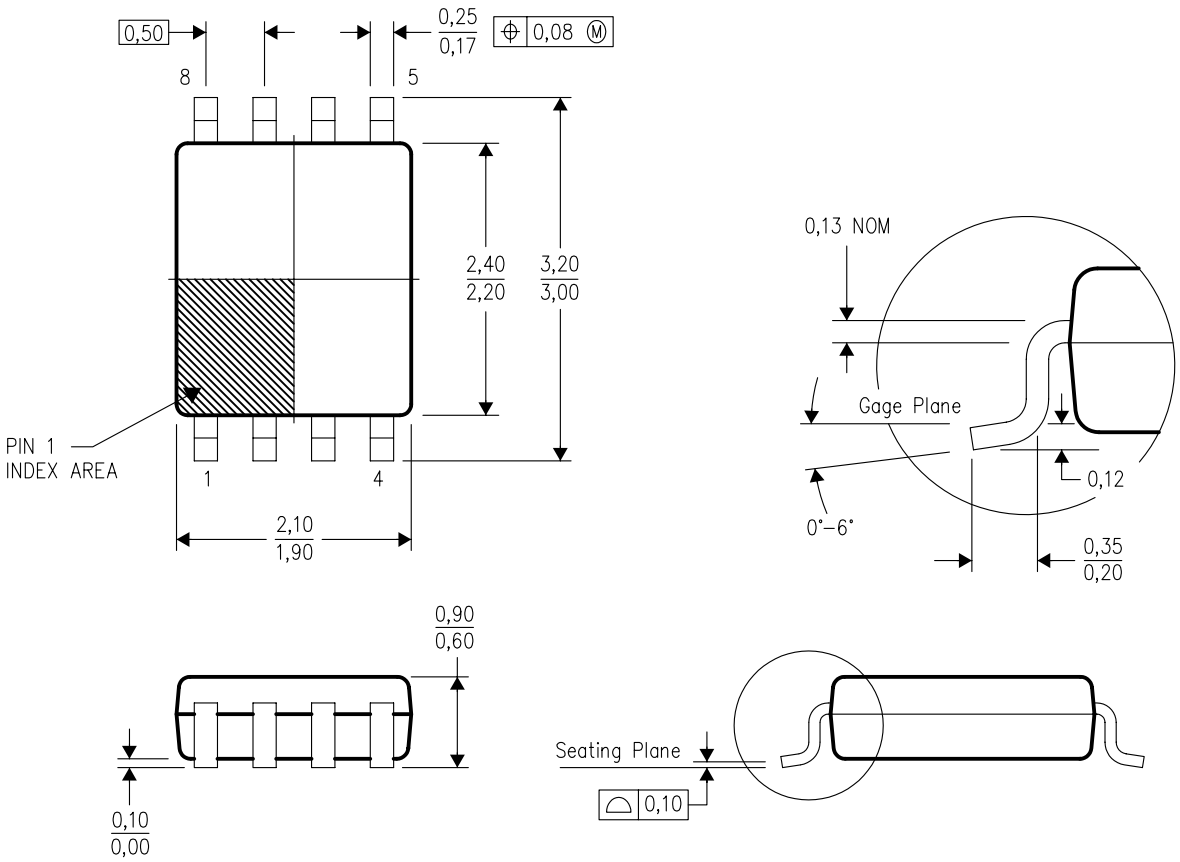
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9306IDCURQ1	US8	DCU	8	3000	202.0	201.0	28.0
PCA9306TDCURQ1	US8	DCU	8	3000	202.0	201.0	28.0

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



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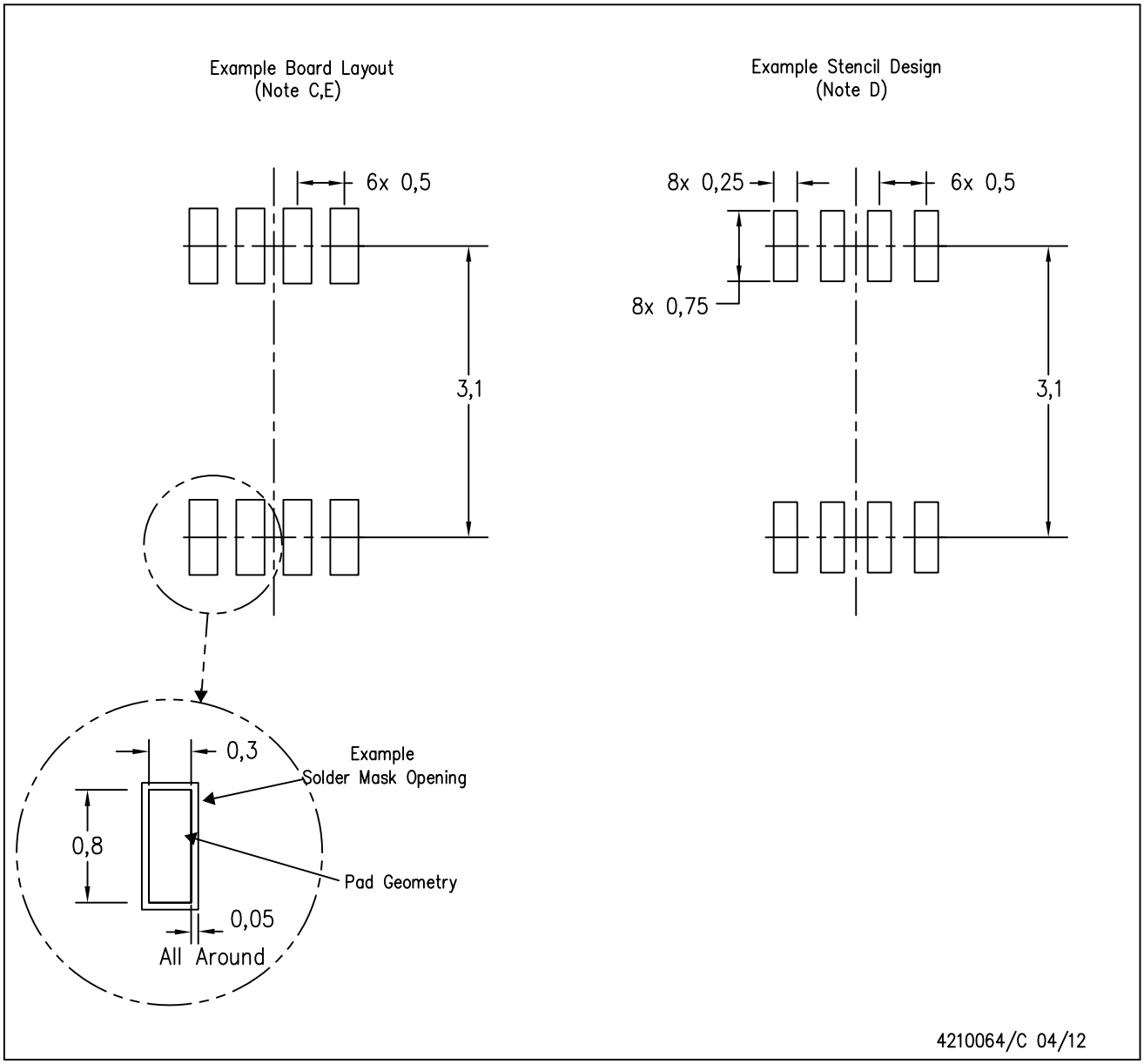
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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