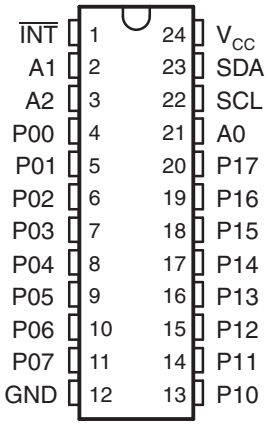
LOW VOLTAGE 16-BIT I²C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS

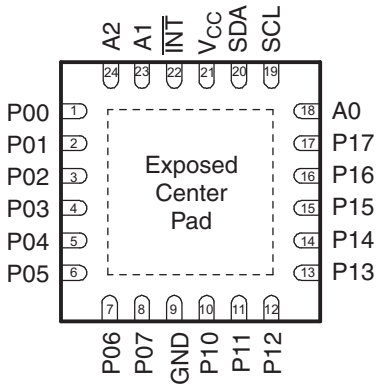
FEATURES

- **Low Standby-Current Consumption of 3 μA Max**
- **I²C to Parallel Port Expander**
- **Open-Drain Active-Low Interrupt Output**
- **5-V Tolerant I/O Ports**
- **Compatible With Most Microcontrollers**
- **400-kHz Fast I²C Bus**
- **Address by Three Hardware Address Pins for Use of up to Eight Devices**
- **Polarity Inversion Register**
- **Latched Outputs With High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

PW PACKAGE
(TOP VIEW)



RTW PACKAGE
(TOP VIEW)



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

DESCRIPTION/ORDERING INFORMATION

This 16-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The TCA9555 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low operation) registers. At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the TCA9555 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I²C/SMBus state machine.

The TCA9555 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA9555 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs.

Although pin-to-pin and I^2C-address is compatible with the PCF8575, software changes are required due to the enhancements.

The TCA9555 is identical to the TCA9535, except for the inclusion of the internal I/O pullup resistor, which pulls the I/O to a default high when configured as an input and undriven.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address and allow up to eight devices to share the same I^2C bus or SMBus. The fixed I^2C address of the TCA9555 is the same as the PCF8575, PCF8575C, and PCF8574, allowing up to eight of these devices in any combination to share the same I^2C bus or SMBus.

ORDERING INFORMATION(1)

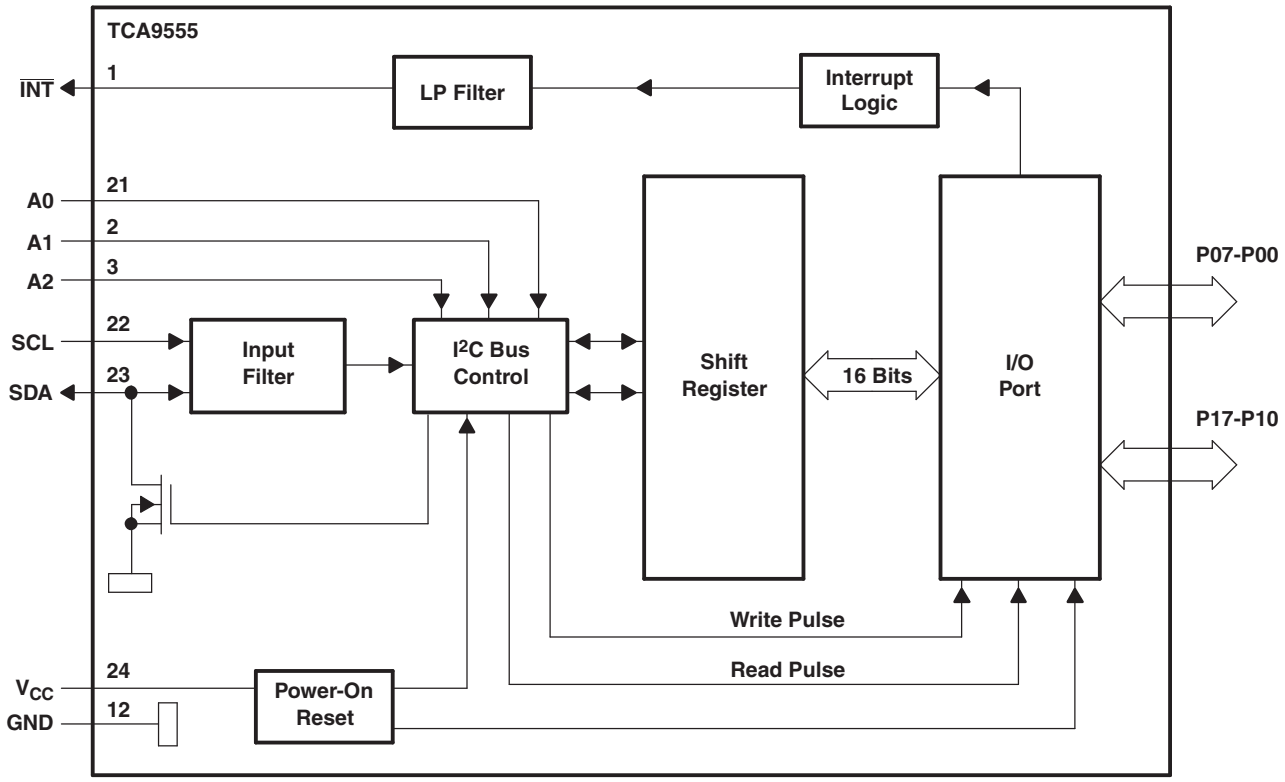
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Reel of 2000	TCA9555PWR	PW555
	QFN – RTW	Reel of 3000	TCA9555RTWR	PW555

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TERMINAL FUNCTIONS

NO.		NAME	DESCRIPTION
TSSOP (PW)	QFN (RTW)		
1	22	$\overline{INT}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
2	23	A1	Address input 1. Connect directly to V_{CC} or ground.
3	24	A2	Address input 2. Connect directly to V_{CC} or ground.
4	1	P00	P-port input/output. Push-pull design structure. At power on, P00 is configured as an input.
5	2	P01	P-port input/output. Push-pull design structure. At power on, P01 is configured as an input.
6	3	P02	P-port input/output. Push-pull design structure. At power on, P02 is configured as an input.
7	4	P03	P-port input/output. Push-pull design structure. At power on, P03 is configured as an input.
8	5	P04	P-port input/output. Push-pull design structure. At power on, P04 is configured as an input.
9	6	P05	P-port input/output. Push-pull design structure. At power on, P05 is configured as an input.
10	7	P06	P-port input/output. Push-pull design structure. At power on, P06 is configured as an input.
11	8	P07	P-port input/output. Push-pull design structure. At power on, P07 is configured as an input.
12	9	GND	Ground
13	10	P10	P-port input/output. Push-pull design structure. At power on, P10 is configured as an input.
14	11	P11	P-port input/output. Push-pull design structure. At power on, P11 is configured as an input.
15	12	P12	P-port input/output. Push-pull design structure. At power on, P12 is configured as an input.
16	13	P13	P-port input/output. Push-pull design structure. At power on, P13 is configured as an input.
17	14	P14	P-port input/output. Push-pull design structure. At power on, P14 is configured as an input.
18	15	P15	P-port input/output. Push-pull design structure. At power on, P15 is configured as an input.
19	16	P16	P-port input/output. Push-pull design structure. At power on, P16 is configured as an input.
20	17	P17	P-port input/output. Push-pull design structure. At power on, P17 is configured as an input.
21	18	A0	Address input 0. Connect directly to V_{CC} or ground.
22	19	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
23	20	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
24	21	V_{CC}	Supply voltage

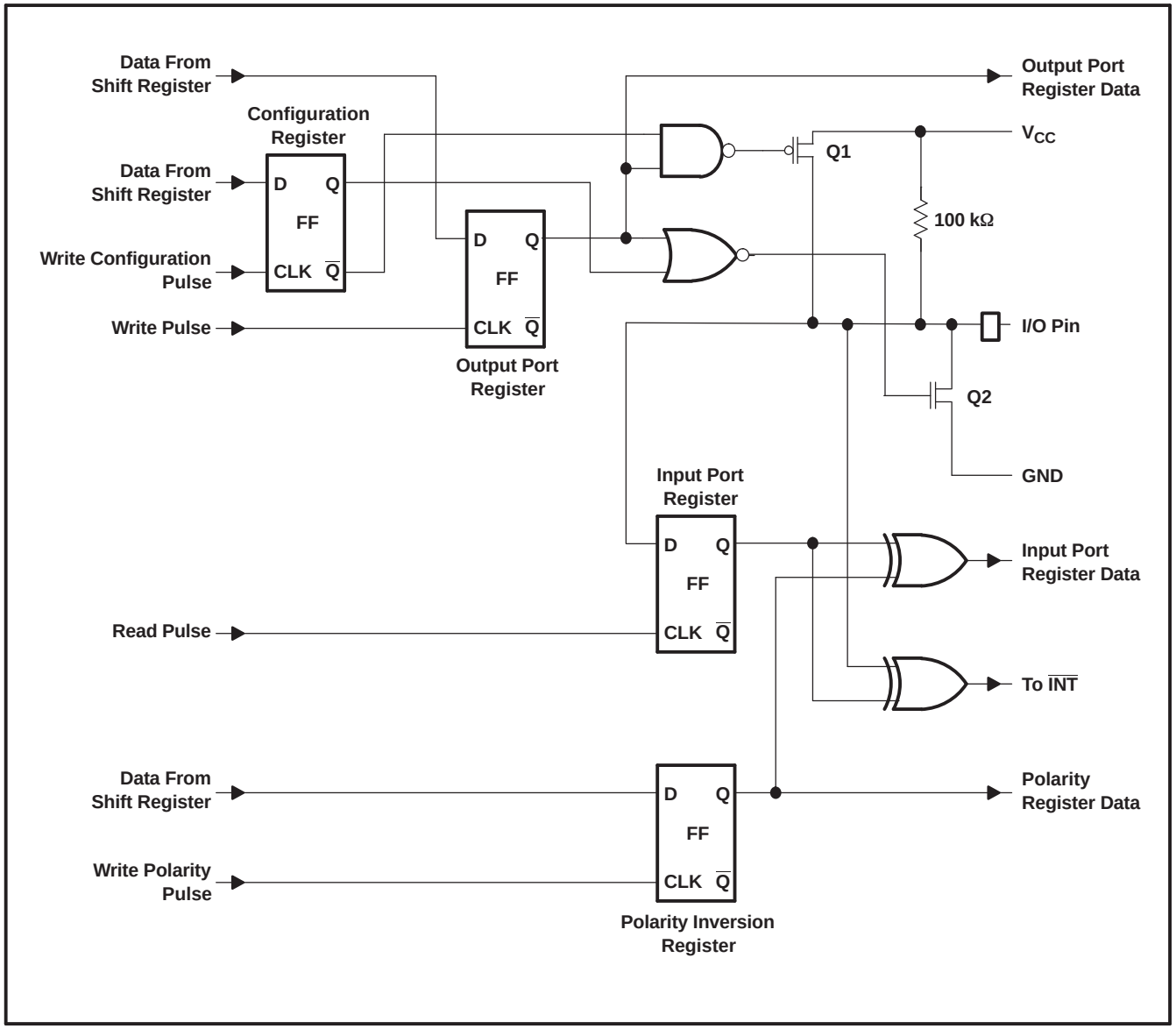
LOGIC DIAGRAM (POSITIVE LOGIC)



A. Pin numbers shown are for the PW package.

B. All I/Os are set to inputs at reset.

SIMPLIFIED SCHEMATIC OF P-PORT I/Os



I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

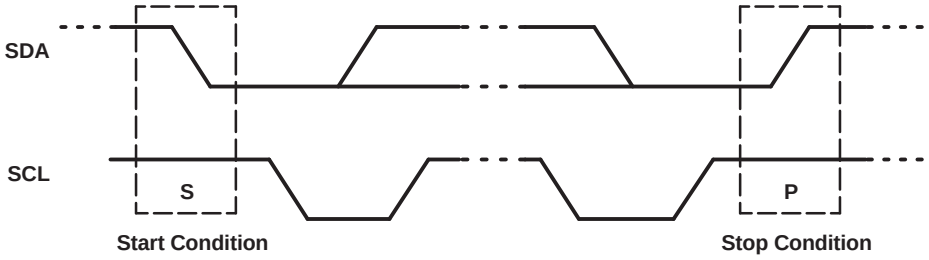


Figure 1. Definition of Start and Stop Conditions

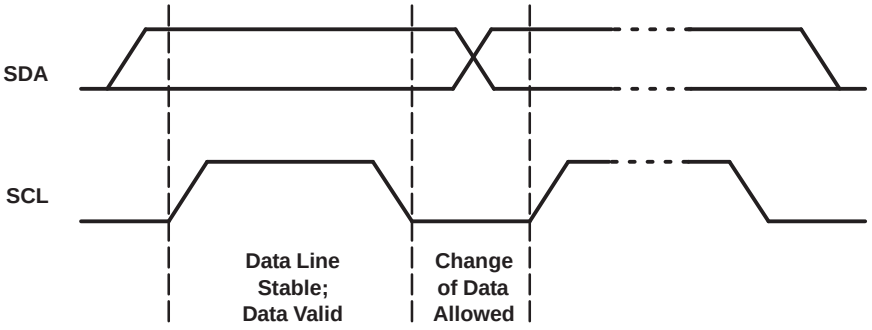


Figure 2. Bit Transfer

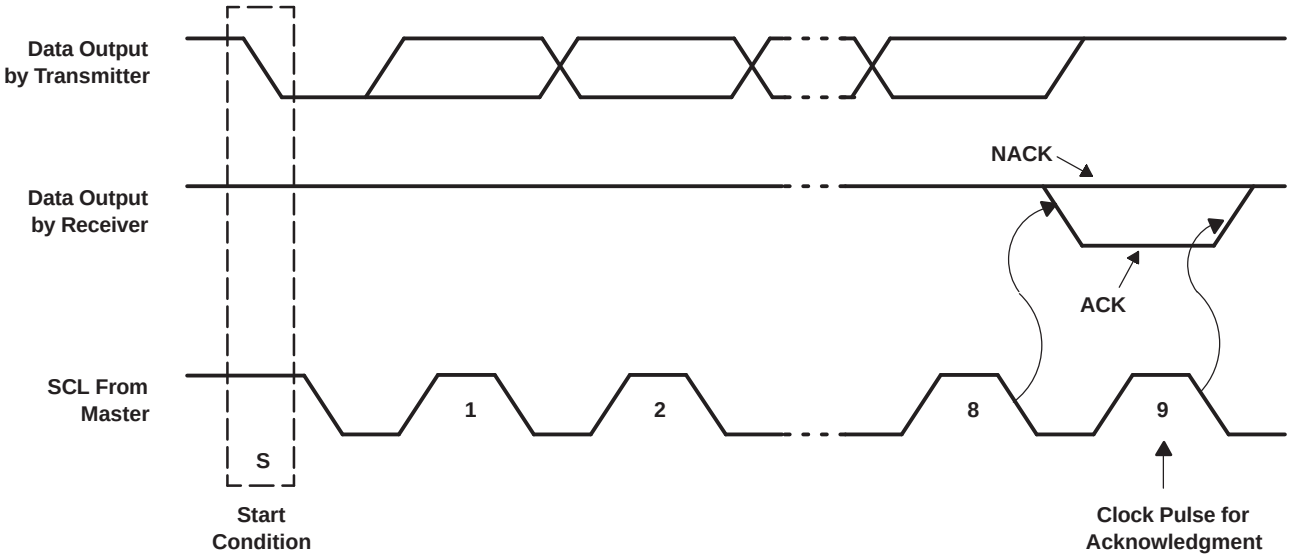


Figure 3. Acknowledgment on I²C Bus

Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

Device Address

Figure 4 shows the address byte of the TCA9555.

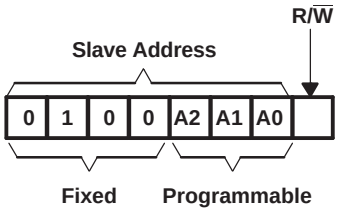


Figure 4. TCA9555 Address

Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9555. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

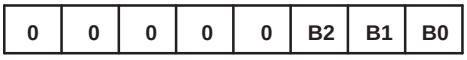


Figure 5. Control Register Bits

Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register will be accessed next.

Registers 0 and 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Registers 2 and 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Registers 4 and 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Registers 6 and 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA9555 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the TCA9555 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt or in a Stop event. Resetting occurs in the read mode at the acknowledge (ACK) bit or not acknowledge (NACK) bit after the falling edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{INT}$ has an open-drain structure and requires a pullup resistor to V_{CC}.

Bus Transactions

Data is exchanged between the master and the TCA9555 through write and read commands.

Writes

Data is transmitted to the TCA9555 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the TCA9555 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion ports, and configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 6 and Figure 7). For example, if the first byte is sent to output port (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

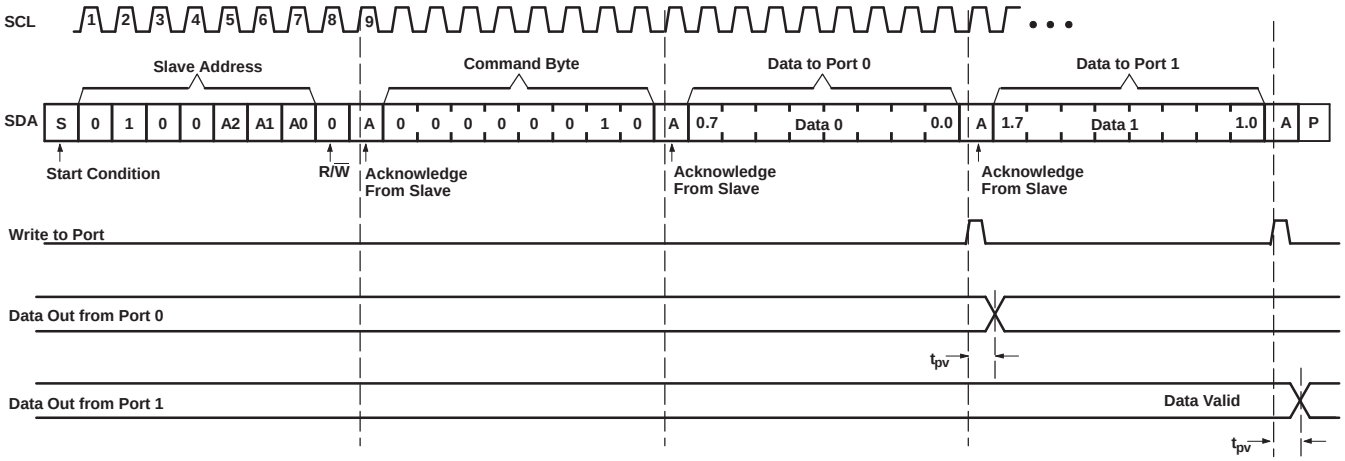


Figure 6. Write to Output Port Registers

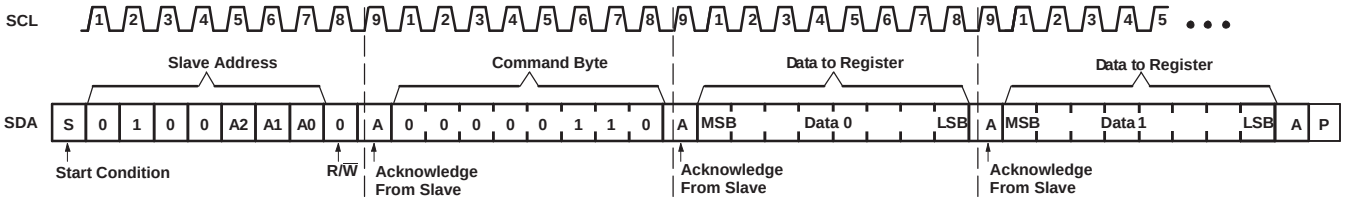


Figure 7. Write to Configuration Registers

Reads

The bus master first must send the TCA9555 address with the least-significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA9555 (see Figure 8 through Figure 10).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

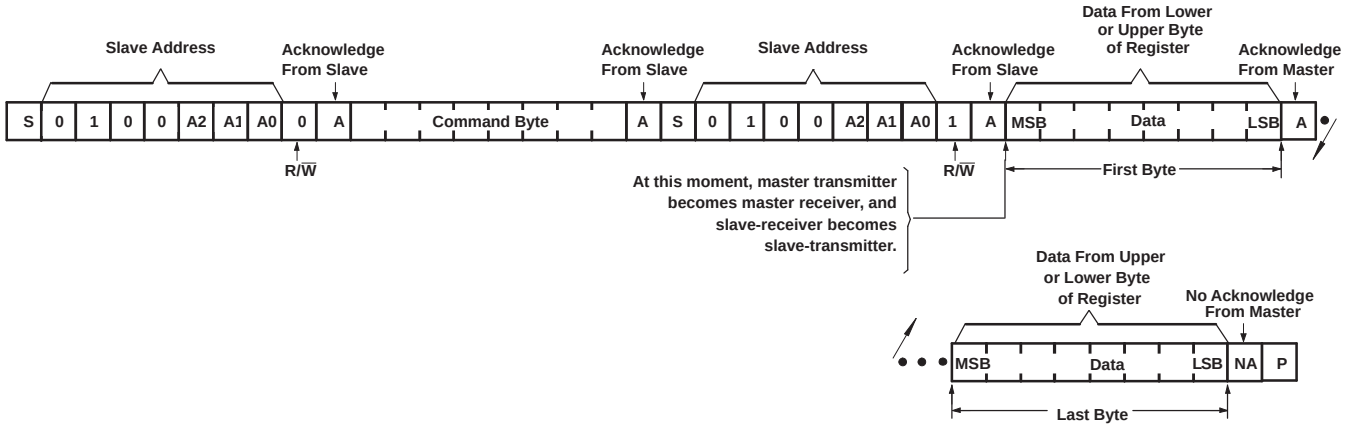
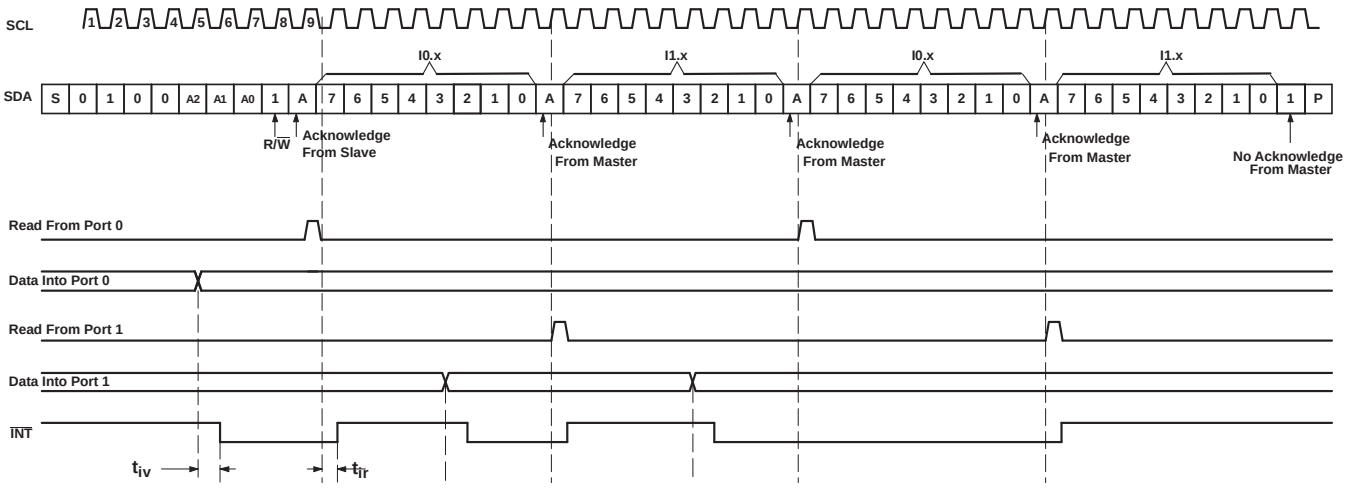


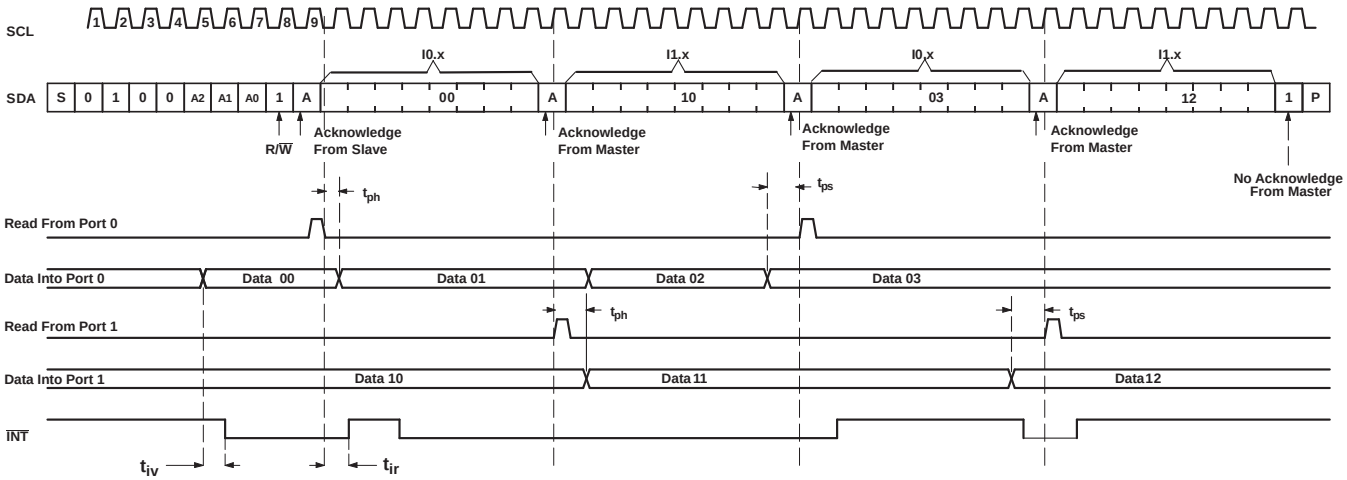
Figure 8. Read From Register



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 8 for these details).

Figure 9. Read Input Port Register, Scenario 1



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 8 for these details).

Figure 10. Read Input Port Register, Scenario 2

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance, junction to free air(3)	PW package		88	°C/W
		RTW package		66	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P07–P00, P17–P10	$0.7 \times V_{CC}$	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		A2–A0, P07–P00, P17–P10	–0.5	$0.3 \times V_{CC}$	
I_{OH}	High-level output current	P07–P00, P17–P10		–10	mA
I_{OL}	Low-level output current	P07–P00, P17–P10		25	mA
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage		$V_I = V_{CC}$ or GND, I_O = 0	1.65 V to 5.5 V		1.5	1.65	V
V_{OH}	P-port high-level output voltage(2)		I_{OH} = –8 mA	1.65 V	1.2			V
				2.3 V	1.8			
				3 V	2.6			
				4.75 V	4.1			
			I_{OH} = –10 mA	1.65 V	1.8			
				2.3 V	1.7			
				3 V	2.5			
				4.75 V	4			
I_{OL}	SDA		V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
	P port(3)		V_{OL} = 0.5 V		8	20		
			V_{OL} = 0.7 V		10	24		
	$\overline{INT}$		V_{OL} = 0.4 V		3			
I_I	SCL, SDA		$V_I = V_{CC}$ or GND	1.65 V to 5.5 V			±1	µA
	A2–A0						±1	
I_{IH}	P port		$V_I = V_{CC}$	1.65 V to 5.5 V			1	µA
I_{IL}	P port		V_I = GND	1.65 V to 5.5 V			–100	µA
I_{CC}	Operating mode		$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz, No load	5.5 V		100	200	µA
				3.6 V		30	75	
				2.7 V		20	50	
				1.95 V		10	45	
	Standby mode	Low inputs	V_I = GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.1	1.5	mA
				3.6 V		0.7	1.3	
				2.7 V		0.5	1	
				1.95 V		0.3	0.9	
		High inputs	$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		2.5	3	µA
				3.6 V		2	2.6	
				2.7 V		1.5	2.5	
				1.95 V		1.2	2.3	
ΔI_{CC}	Additional current in standby mode		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	1.65 V to 5.5 V			1.5	mA
C_I	SCL		$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		3	7	pF
C_{io}	SDA		$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		3	7	pF
	P port					3.7	9.5	

(1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 11)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	$20 + 0.1C_b$	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(Data)}$	Valid-data time	SCL low to SDA output valid	50		ns
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	µs
C_b	I²C bus capacitive load			400	pF

SWITCHING CHARACTERISTICS

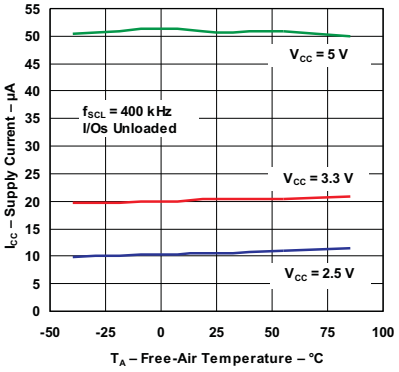
over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 12 and Figure 13)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P port		200	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

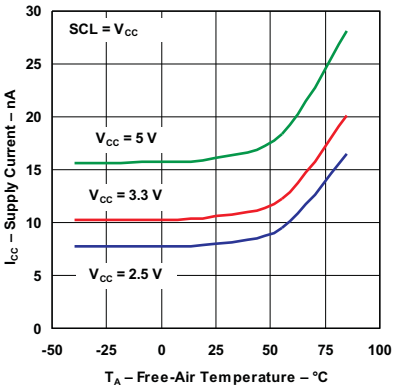
TYPICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

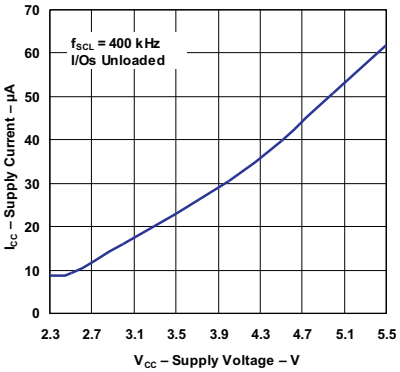
SUPPLY CURRENT VS TEMPERATURE



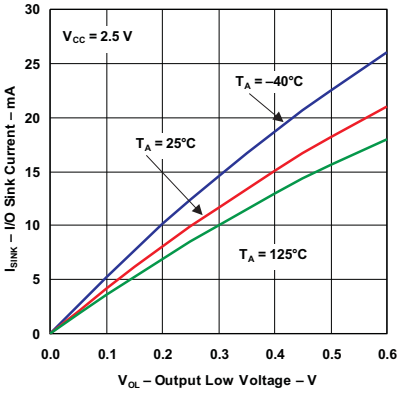
STANDBY SUPPLY CURRENT VS TEMPERATURE



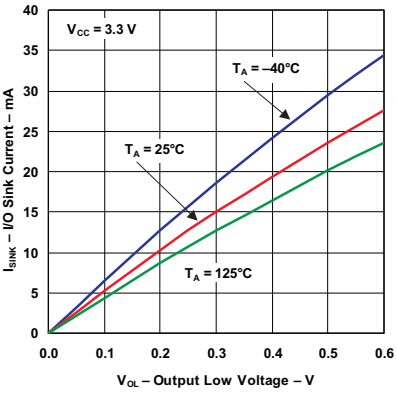
SUPPLY CURRENT VS SUPPLY VOLTAGE



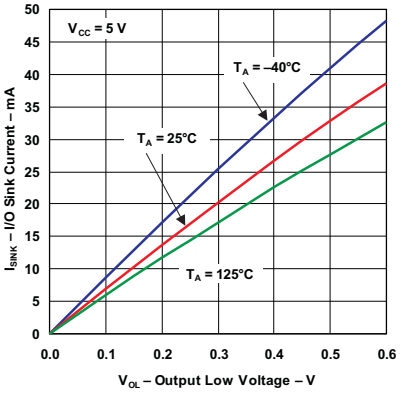
I/O SINK CURRENT VS OUTPUT LOW VOLTAGE



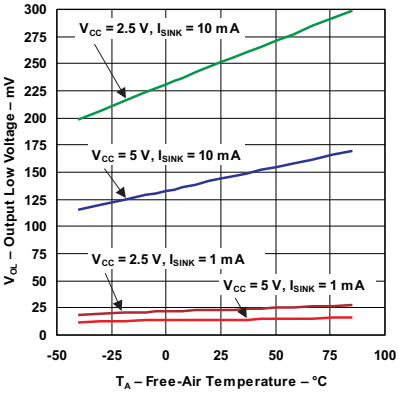
I/O SINK CURRENT VS OUTPUT LOW VOLTAGE



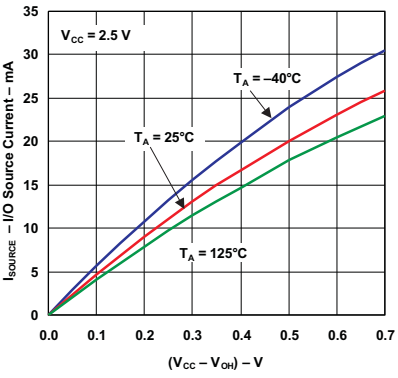
I/O SINK CURRENT VS OUTPUT LOW VOLTAGE



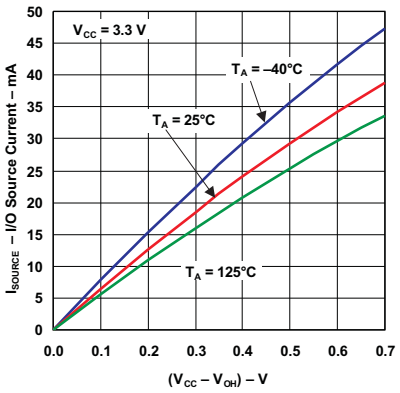
I/O OUTPUT LOW VOLTAGE VS TEMPERATURE



I/O SOURCE CURRENT VS OUTPUT HIGH VOLTAGE



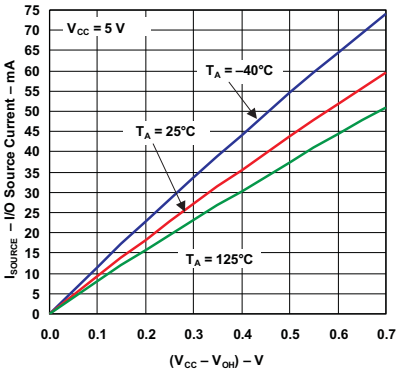
I/O SOURCE CURRENT VS OUTPUT HIGH VOLTAGE



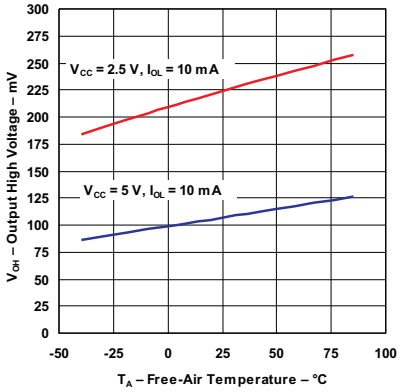
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

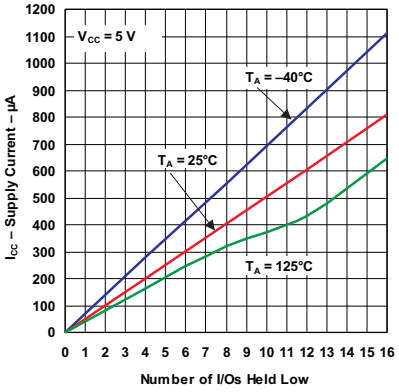
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



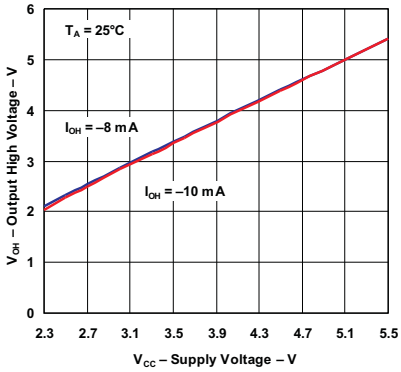
I/O HIGH VOLTAGE vs TEMPERATURE



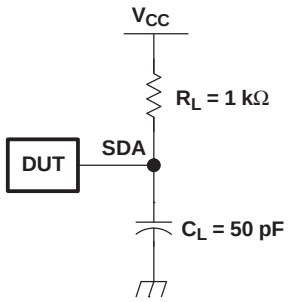
SUPPLY CURRENT vs NUMBER OF I/Os HELD LOW



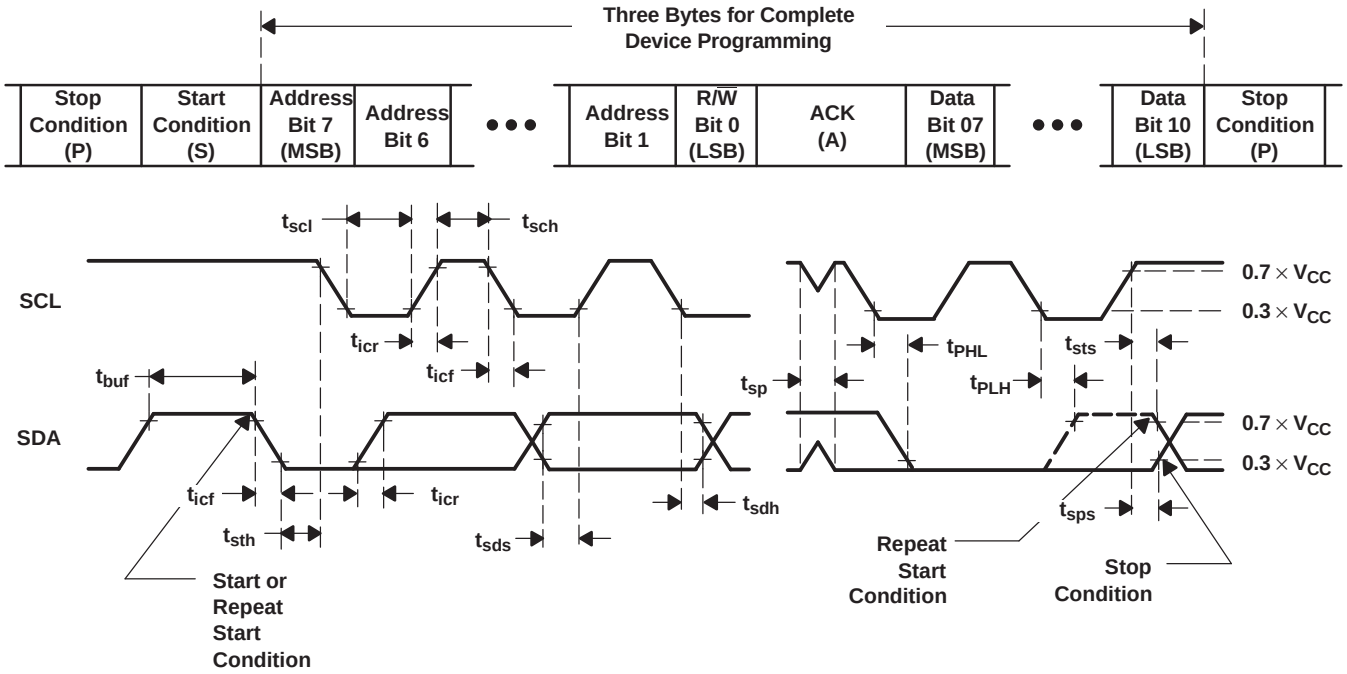
OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE



PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

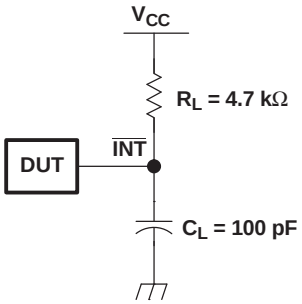
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

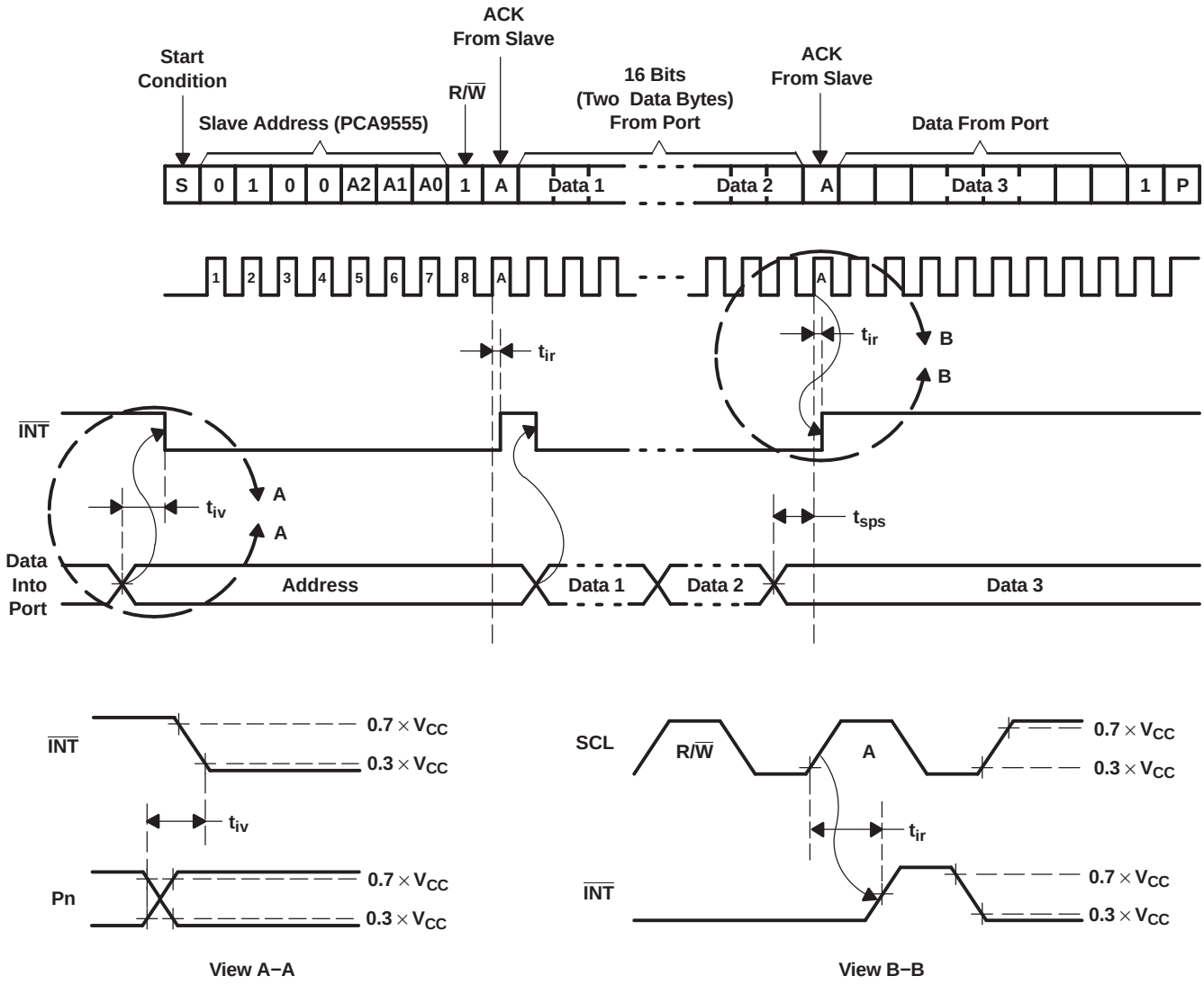
C. All parameters and waveforms are not applicable to all devices.

Figure 11. I^2C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



INTERRUPT LOAD CONFIGURATION



View A–A **View B–B**

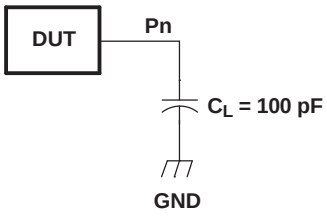
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

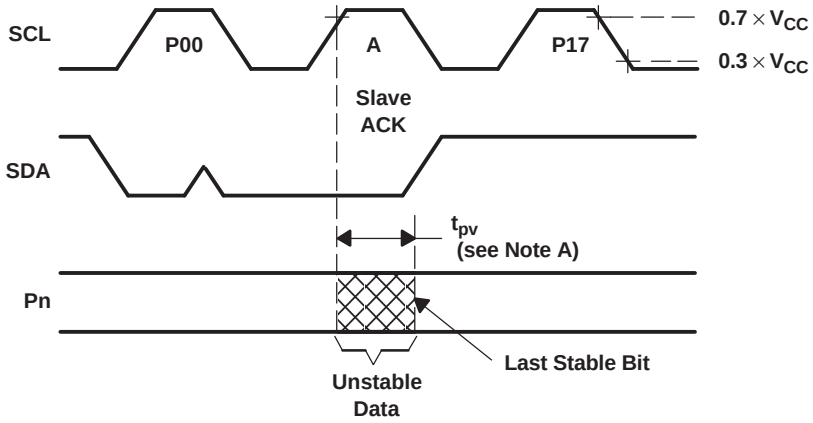
C. All parameters and waveforms are not applicable to all devices.

Figure 12. Interrupt Load Circuit and Voltage Waveforms

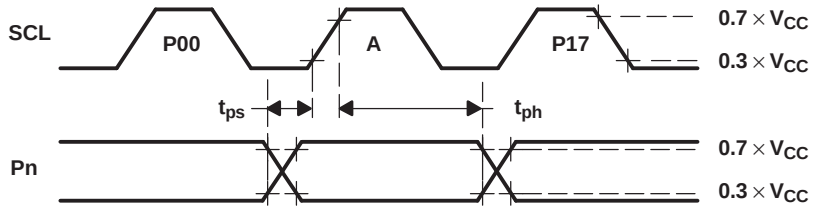
PARAMETER MEASUREMENT INFORMATION (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

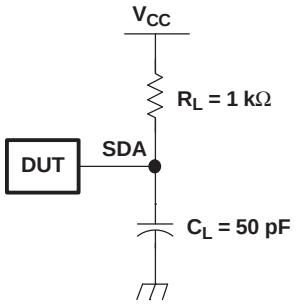
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

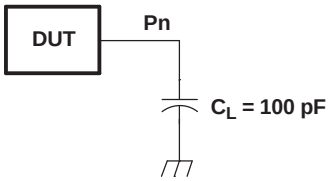
E. All parameters and waveforms are not applicable to all devices.

Figure 13. P-Port Load Circuit and Voltage Waveforms

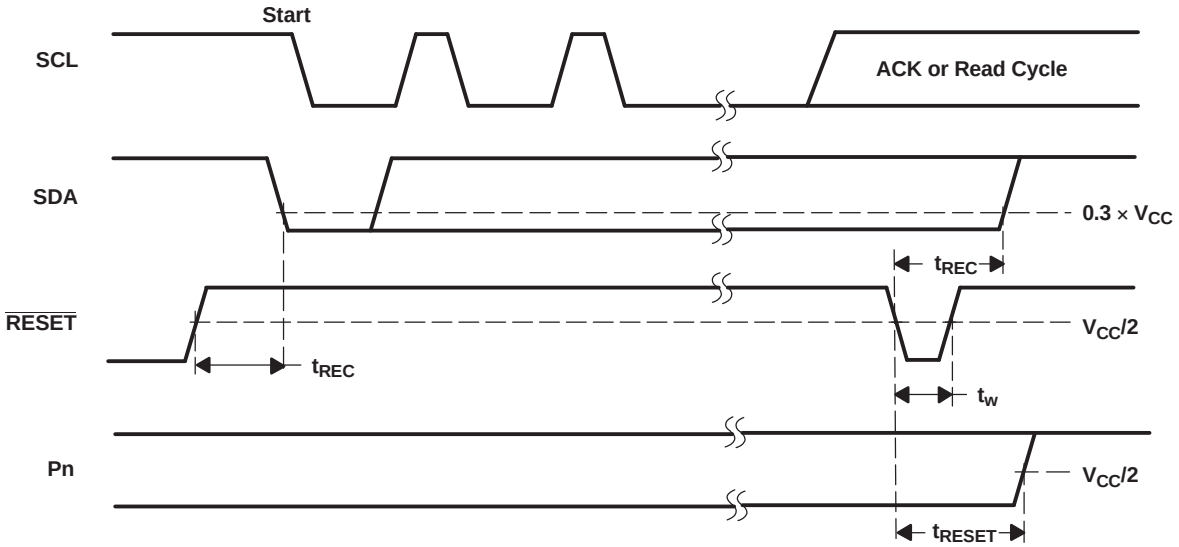
PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION



P-PORT LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

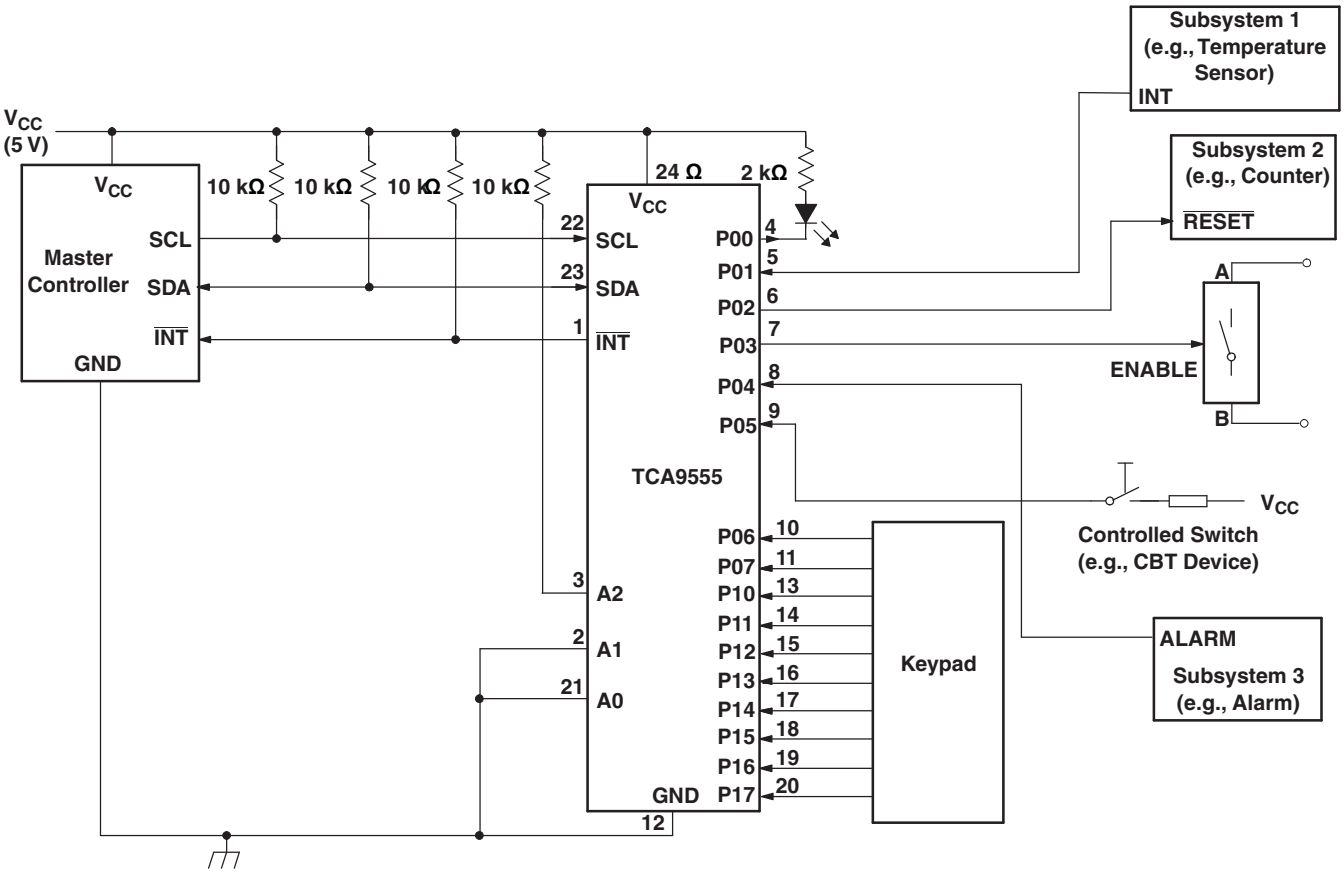
D. I/Os are configured as inputs.

E. All parameters and waveforms are not applicable to all devices.

Figure 14. Reset Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

Figure 15 shows an application in which the TCA9555 can be used.



A. Device address is configured as 0100100 for this example.

B. P00, P02, and P03 are configured as outputs.

C. P01, P04–P07, and P10–P17 are configured as inputs.

D. Pin numbers shown are for the PW package.

Figure 15. Typical Application

Minimizing I_{CC} When I/O Is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 15. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption.

Figure 16 shows a high-value resistor in parallel with the LED. Figure 17 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

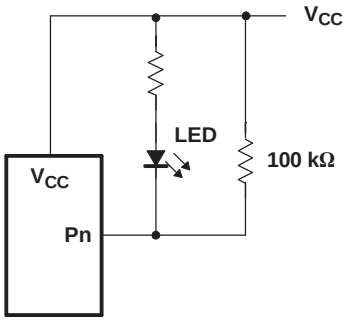


Figure 16. High-Value Resistor in Parallel With LED

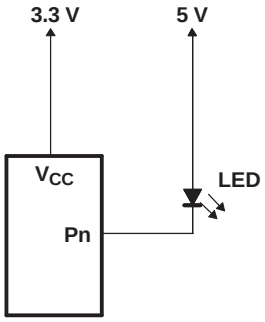


Figure 17. Device Supplied by Lower Voltage

Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9555 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 18 and Figure 19.

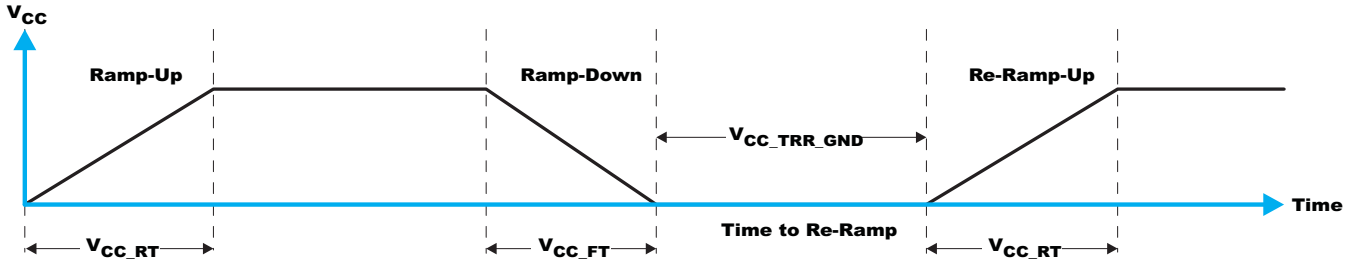


Figure 18. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

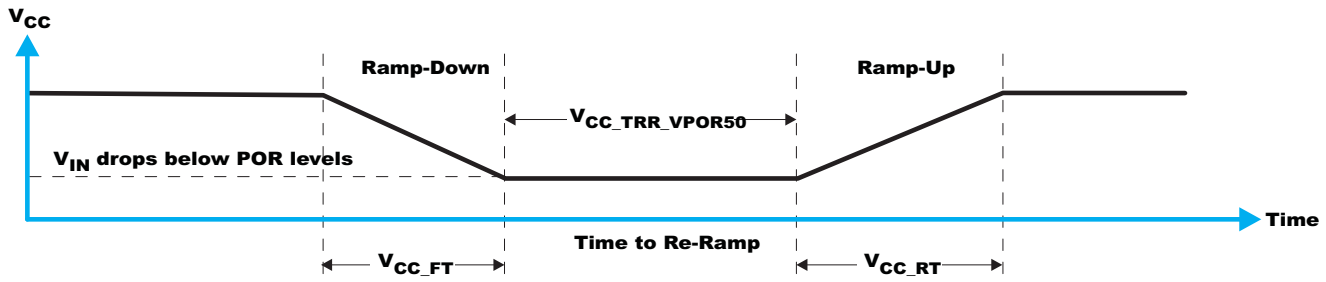


Figure 19. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 1 specifies the performance of the power-on reset feature for TCA9555 for both types of power-on reset.

Table 1. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 18	0.1		2000	ms
V_{CC_RT}	Rise rate	See Figure 18	0.1		2000	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 18	1			µs
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See Figure 19	1			µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See Figure 20			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 20			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.7			V
V_{PORR}	Voltage trip point of POR on rising V_{CC}				1.4	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 20 and Table 1 provide more information on how to measure these specifications.

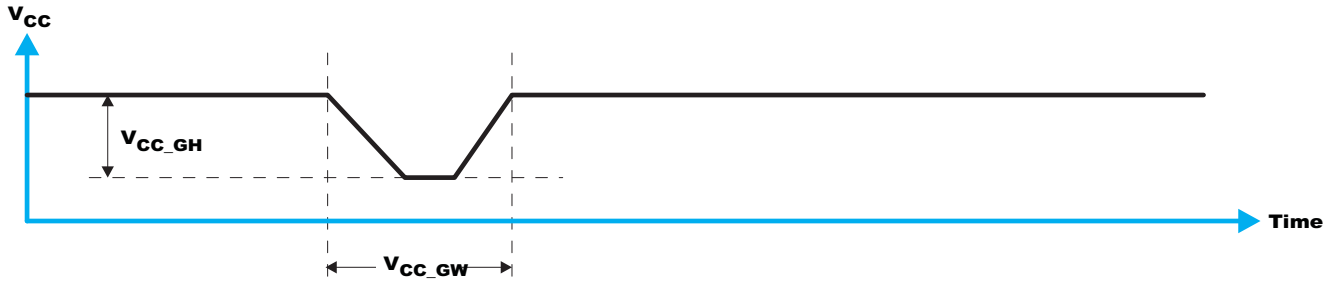


Figure 20. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 21 and Table 1 provide more details on this specification.

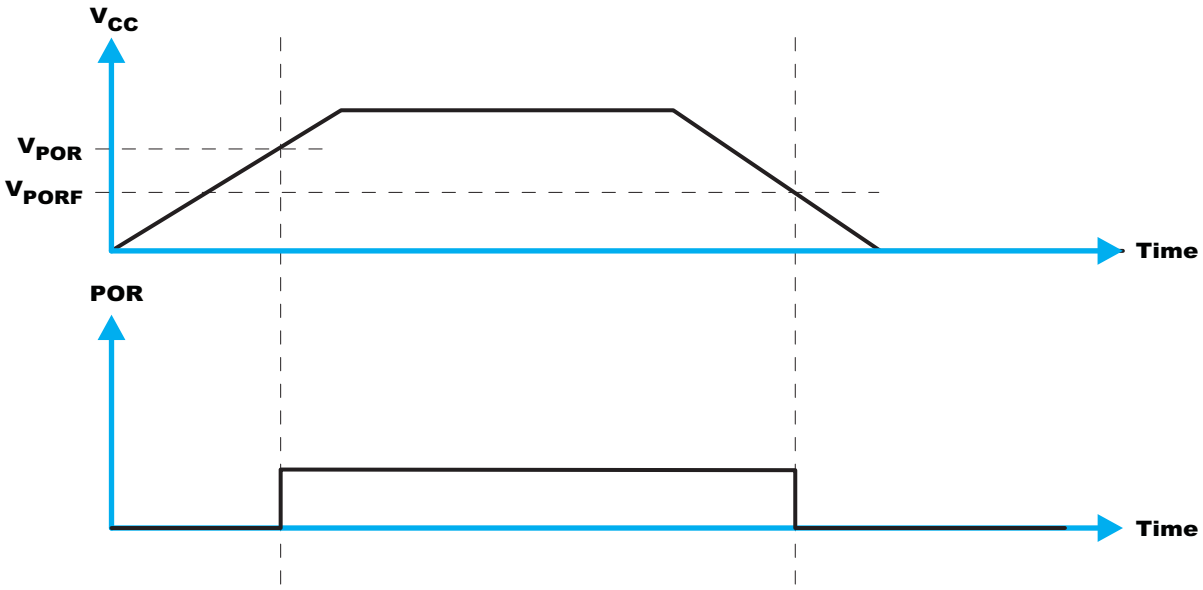


Figure 21. V_{POR}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9555PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW555	Samples
TCA9555RTWR	ACTIVE	WQFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW555	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

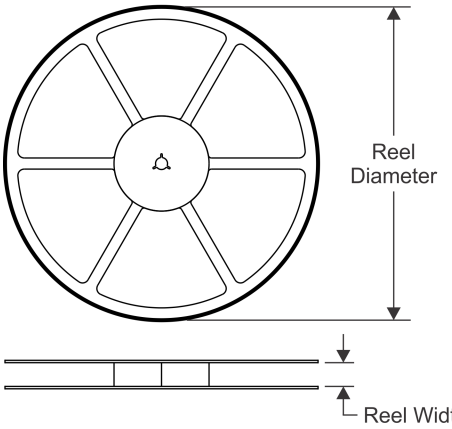
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

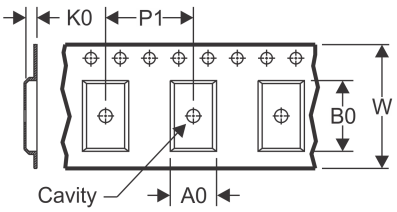
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

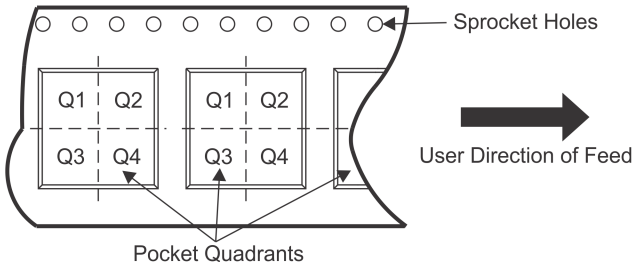


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

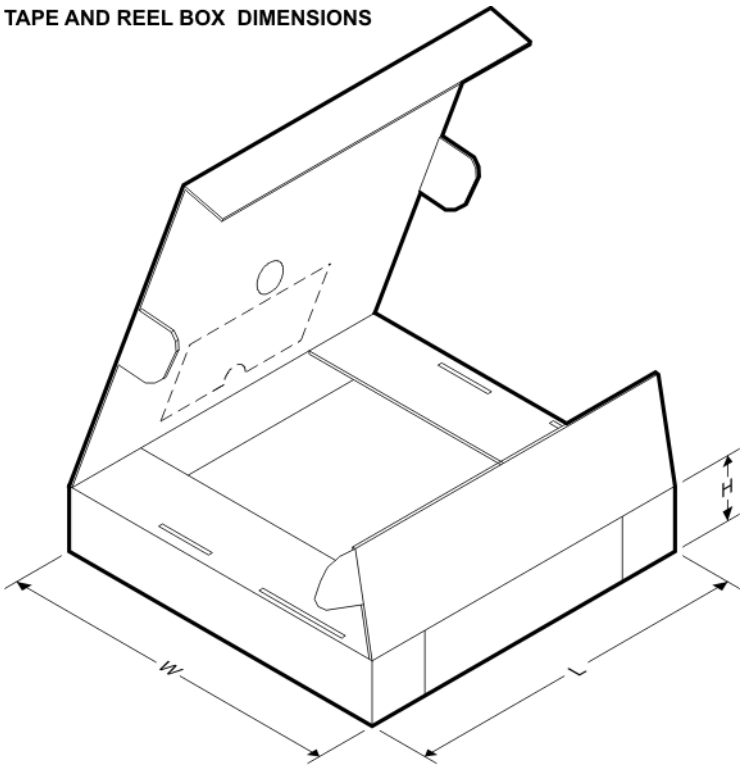
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9555RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

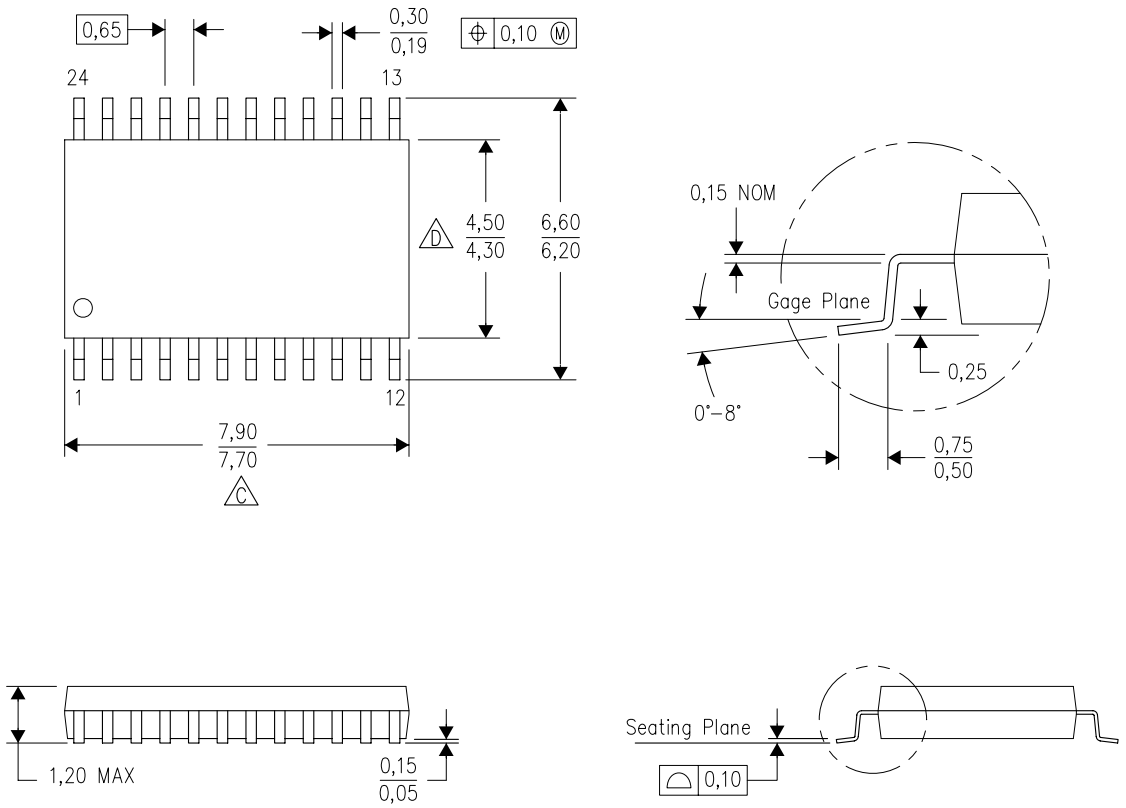
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9555RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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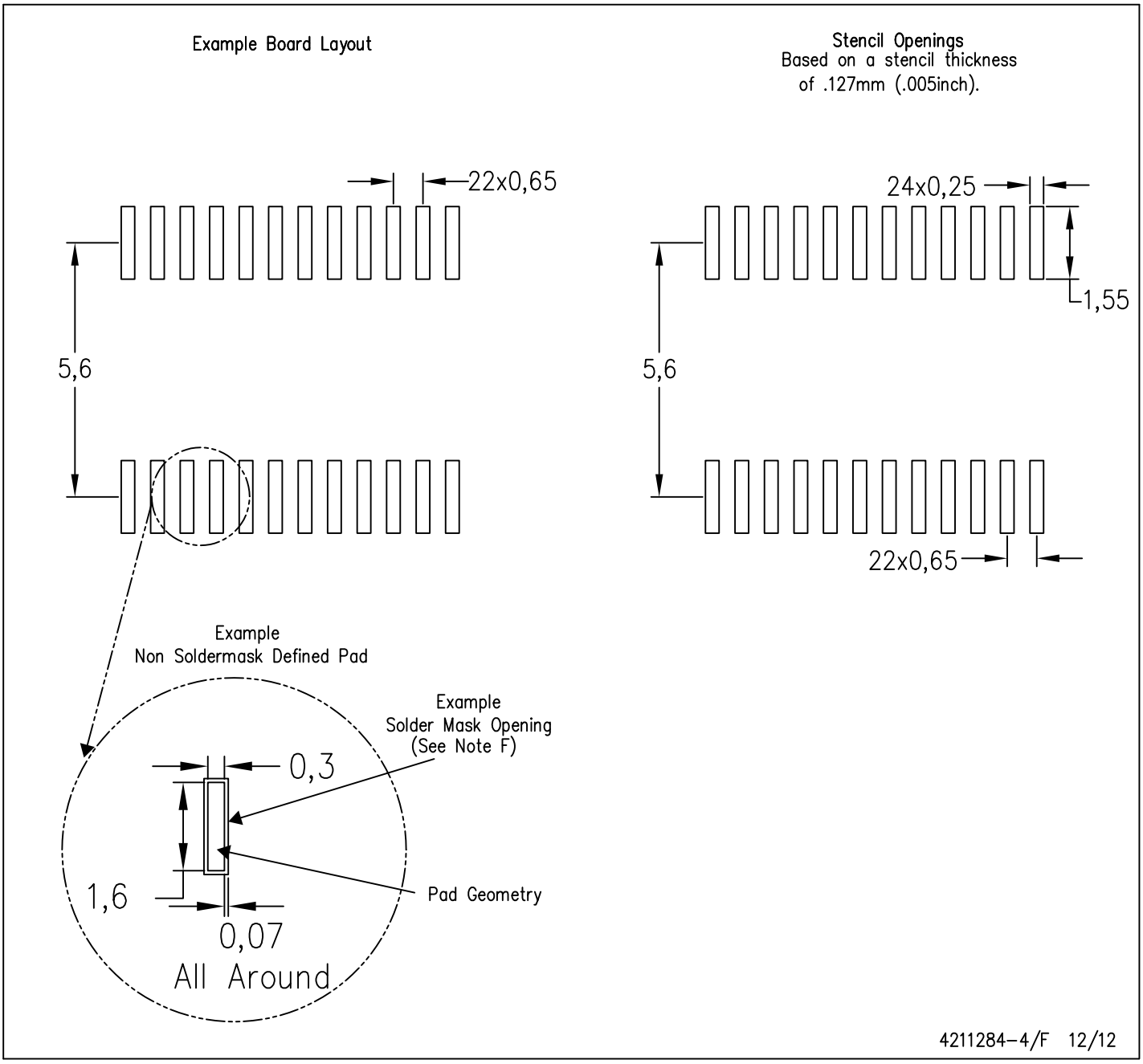
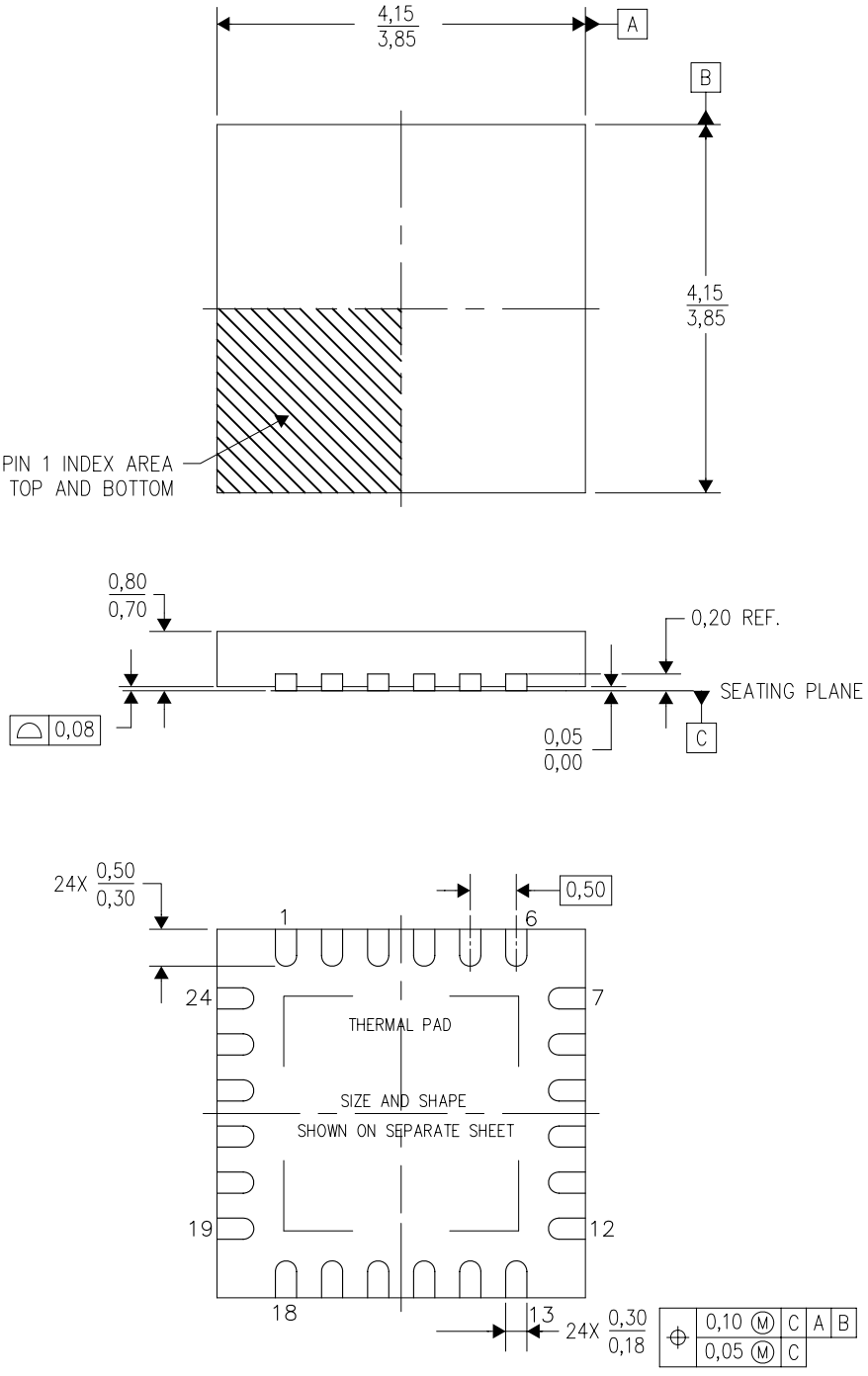
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

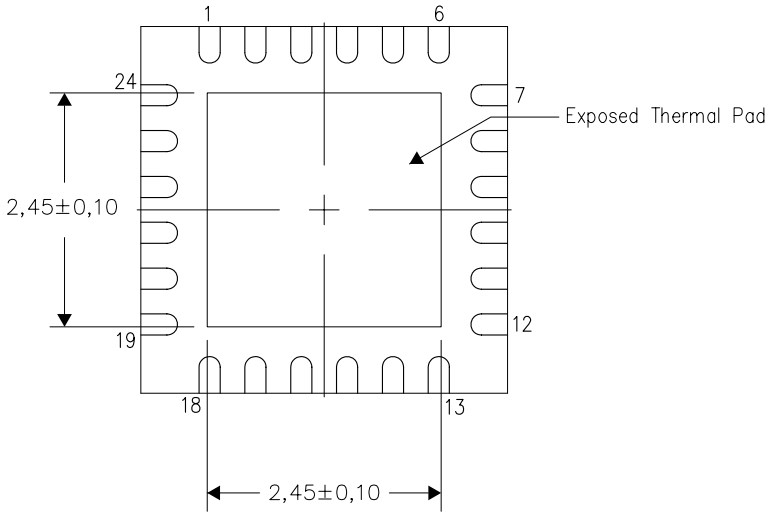
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



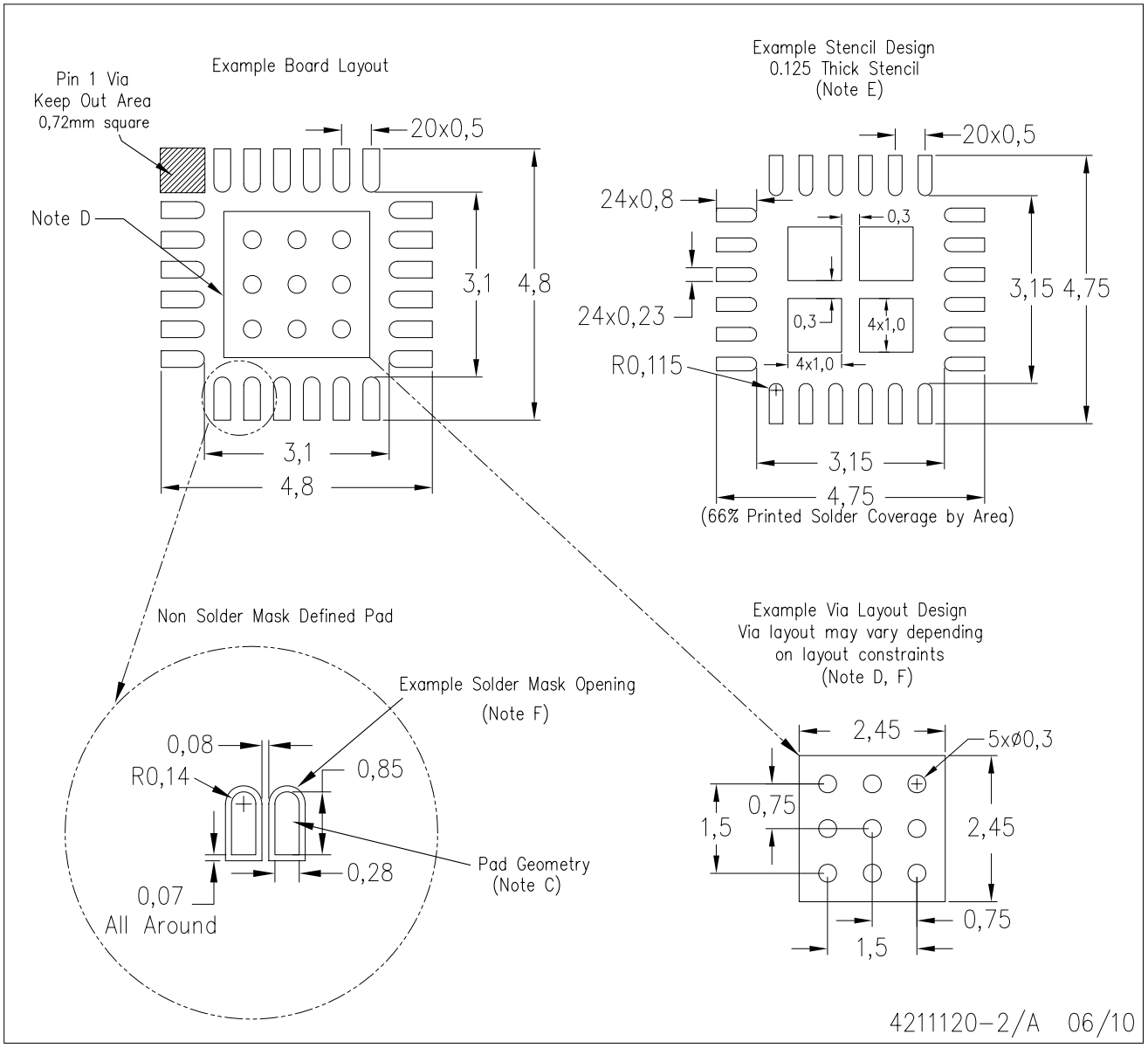
Bottom View

Exposed Thermal Pad Dimensions

4206249–3/L 07/11

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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