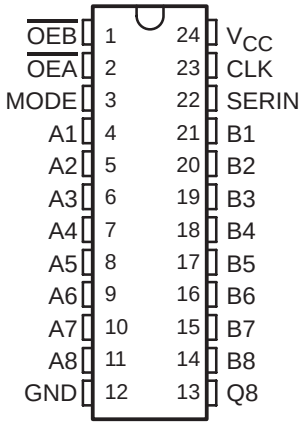
- **Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered 3-State Outputs Drive Bus Lines Directly**
- **Cascadable to n-Bits**
- **Eight Selectable Transceiver/Port Functions:**
  - **− B to A**
  - **− Register to A and/or B**
  - **− Off-Line Shifts (A and B Ports in High-Impedance State)**
  - **− Shifted to A and/or B**
- **Particularly Suitable for Use in Diagnostics Analysis Circuitry**
- **Serial Register Provides:**
  - **− Parallel Storage of Either A or B input Data**
  - **− Serial Transmission of Data from Either A or B Port**
  - **− Readback Mode B to A**
- **Dependable Texas Instruments Quality and Reliability**

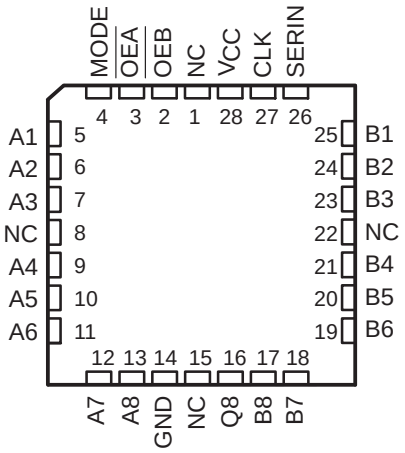
SN54AS856 . . . JT PACKAGE
SN74AS856 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS856 . . . FK PACKAGE
SN74AS856 . . . FN PACKAGE

(TOP VIEW)



NC − No internal connection

description

The ’AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines $\overline{\text{OEA}}$, $\overline{\text{OEB}}$, and MODE. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state). Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The ’AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

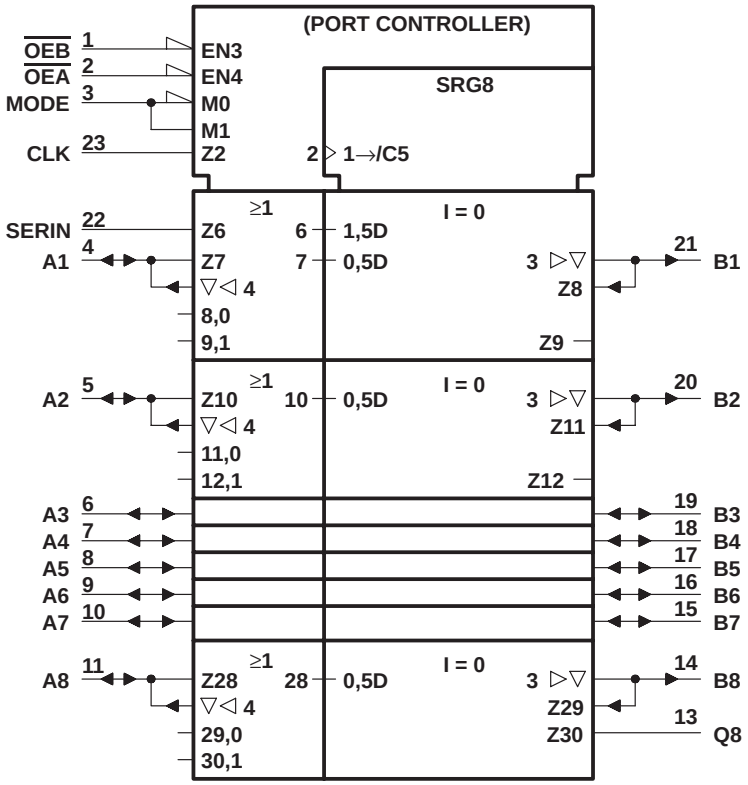
The SN54AS856 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS856 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

MODE	MODE $\overline{OEA}$	MODE $\overline{OEB}$	CLOCK	SERIN	A1	Q1	B1	A2	Q2	B2	A3	Q3	B3	A4	Q4	B4	A5	Q5	B5	A6	Q6	B6	A7	Q7	B7	A8	Q8	B8	FUNCTION
L	L	L	H or L	X	Q1	Q1	H	Q2	Q2	Q2	Q3	Q3	Q3	Q4	Q4	Q4	Q5	Q5	Q5	Q6	Q6	Q6	Q7	Q7	Q7	Q8	Q8	Q8	Feedback
L	L	L	↑	X	Q1	Q1	H	Q2	Q2	Q2	Q3	Q3	Q3	Q4	Q4	Q4	Q5	Q5	Q5	Q6	Q6	Q6	Q7	Q7	Q7	Q8	Q8	Q8	
L	L	H	H or L	X	B1	Q1	H	B2	Q2	Z	B3	Q3	Z	B4	Q4	Z	B5	Q5	Z	B6	Q6	Z	B7	Q7	Z	B8	Q8	Z	B to A
L	L	H	↑	X	B1	B1	L	B2	B2	Z	B3	B3	Z	B4	B4	Z	B5	B5	Z	B6	B6	Z	B7	B7	Z	B8	B8	Z	A to Q
L	H	L	H or L	X	Z	Q1	L	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z	Q8	Q8	A to Q
L	H	L	↑	X	Z	A1	L	Z	A2	A2	Z	A3	A3	Z	A4	A4	Z	A5	A5	Z	A6	A6	Z	A7	A7	Z	A8	A8	Q to B
L	H	H	H or L	X	Z	Q1	L	Z	Q2	Z	Z	Q3	Z	Z	Q4	Z	Z	Q5	Z	Z	Q6	Z	Z	Q7	Z	Z	Q8	Z	A to Q
L	H	H	↑	X	Z	A1	L	Z	A2	Z	Z	A3	Z	Z	A4	Z	Z	A5	Z	Z	A6	Z	Z	A7	Z	Z	A8	Z	
H	L	L	H or L	X	Q1	Q_n	L	Q2	Q_n	Q2	Q3	Q_n	Q3	Q4	Q_n	Q4	Q5	Q_n	Q5	Q6	Q_n	Q6	Q7	Q_n	Q7	Q8	Q_n	Q8	Shift
H	L	L	↑	H	H	H	L	Q1	Q1	Q1	Q2	Q2	Q2	Q3	Q3	Q3	Q4	Q4	Q4	Q5	Q5	Q5	Q6	Q6	Q6	Q7	Q7	Q7	To
H	L	L	↑	L	L	L	L	Q1	Q1	Q1	Q2	Q2	Q2	Q3	Q3	Q3	Q4	Q4	Q4	Q5	Q5	Q5	Q6	Q6	Q6	Q7	Q7	Q7	A and B
H	L	H	H or L	X	Q1	Q_n	L	Q2	Q_n	Z	Q3	Q_n	Z	Q4	Q_n	Z	Q5	Q_n	Z	Q6	Q_n	Z	Q7	Q_n	Z	Q8	Q_n	Z	Shift
H	L	H	↑	H	H	H	L	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z	To
H	L	H	↑	L	L	L	L	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z	A
H	H	L	H or L	X	Z	Q_n	L	Z	Q_n	Q2	Z	Q_n	Q3	Z	Q_n	Q4	Z	Q_n	Q5	Z	Q_n	Q6	Z	Q_n	Q7	Z	Q_n	Q8	Shift
H	H	L	↑	H	Z	H	L	Z	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	To
H	H	L	↑	L	Z	L	L	Z	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	B
H	H	H	H or L	X	Z	Q_n	L	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Z	Q_n	Z	Shift
H	H	H	↑	H	Z	H	L	Z	Q1	Z	Z	Q2	Z	Z	Q3	Z	Z	Q4	Z	Z	Q5	Z	Z	Q6	Z	Z	Q7	Z	
H	H	H	↑	L	Z	L	L	Z	Q1	Z	Z	Q2	Z	Z	Q3	Z	Z	Q4	Z	Z	Q5	Z	Z	Q6	Z	Z	Q7	Z	

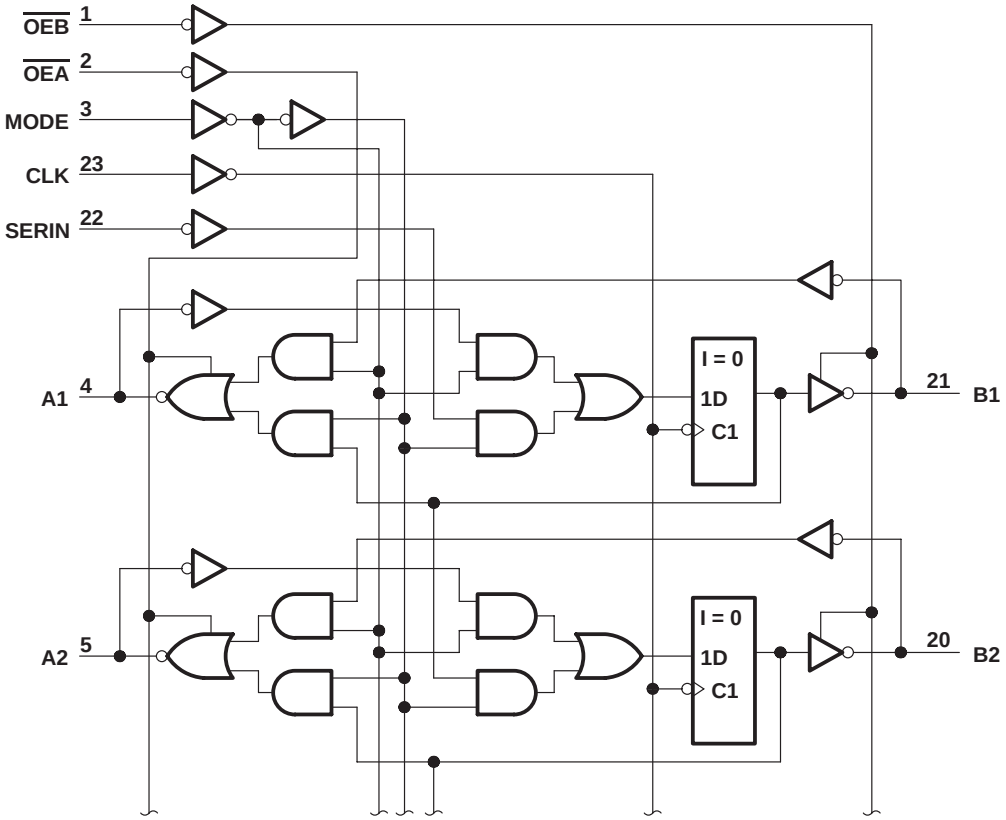
n = level of Q_n(n = 1, 2 . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as the data travels from port to port are ignored in this table.

logic symbol†



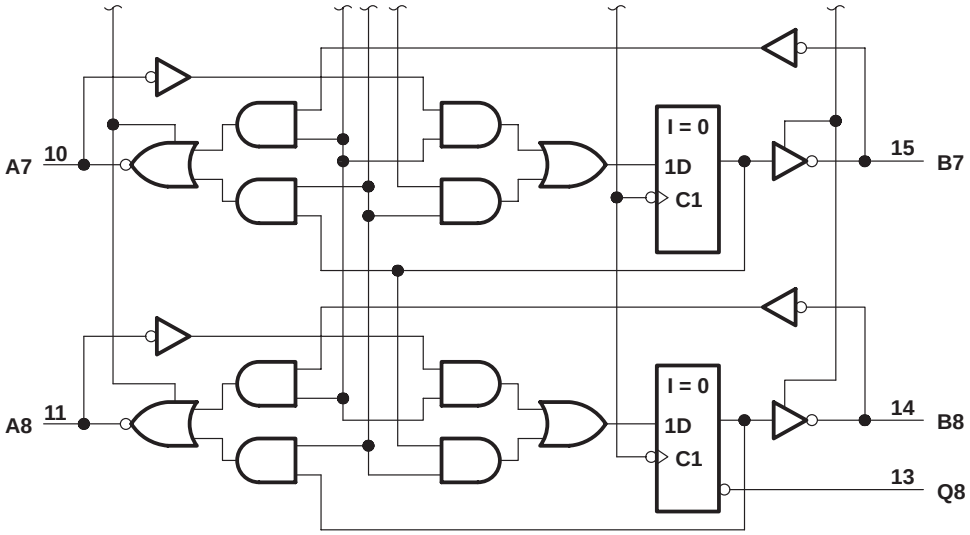
Pin numbers shown are for DW, JT, and NT packages.
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Four Identical Channels Not Shown
Inputs/Outputs Not Shown:

(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS856 . . . . . −55°C to 125°C
SN74AS856 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS856			SN74AS856			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		$\overline{OEB}$, $\overline{OEA}$, MODE	5.5			5.5			
t_h	Hold-time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		$\overline{OEB}$, $\overline{OEA}$, MODE	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS856			SN74AS856			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			
V_{OL}	All outputs	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	except Q8	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.5			0.5	
I_I	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	µA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	$\overline{OEB}$, $\overline{OEA}$, MODE	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.5			−0.5	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			118	200		118	200	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters II_I and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS856		SN74AS856		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any B port	Any A port	2	8	2	7	ns
t_{PHL}			2	10.5	2	9.5	
t_{PLH}	↑MODE	Any A or B port	2	8.5	2	7.5	ns
t_{PHL}			5	20	5	19	
t_{PLH}	↓MODE †	Any A or B port	2	8.5	2	7.5	ns
t_{PHL}			2	9.5	2	8	
t_{PLH}	CLK	Any A or B port	3	12	3	9	ns
t_{PHL}			3	12	3	11	
t_{PLH}	CLK	Q8	2	9	2	7.5	ns
t_{PHL}			2	10	2	9	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	Any A or B port	2	9	2	7	ns
t_{PLZ}			2	12	2	9.5	
t_{PZH}			2	8	2	7	ns
t_{PZL}			2	11	2	10	

† The positive transition of the MODE control will cause low-level data at the A output bus or stored in Q to be invalid for 12 ns.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AS856DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74AS856NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74AS856NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.