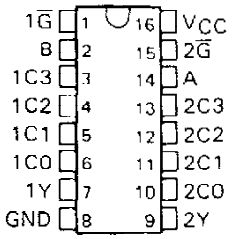
SN54F352, SN74F352
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

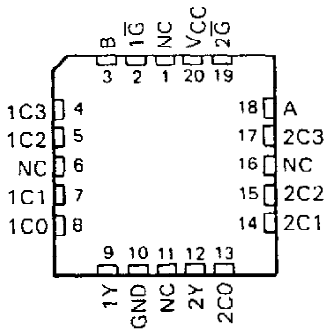
D2932, MARCH 1987–REVISED JANUARY 1989

- Inverting Versions of SN54F153 and SN74F153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54F352 . . . J PACKAGE
SN74F352 . . . D OR N PACKAGE
(TOP VIEW)



SN54F352 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

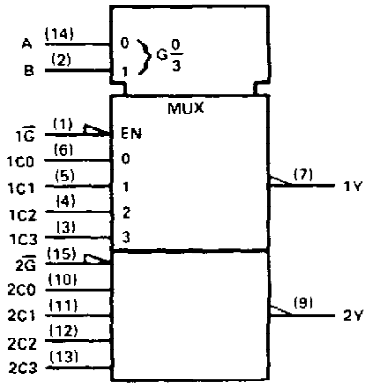
The SN54F352 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F352 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

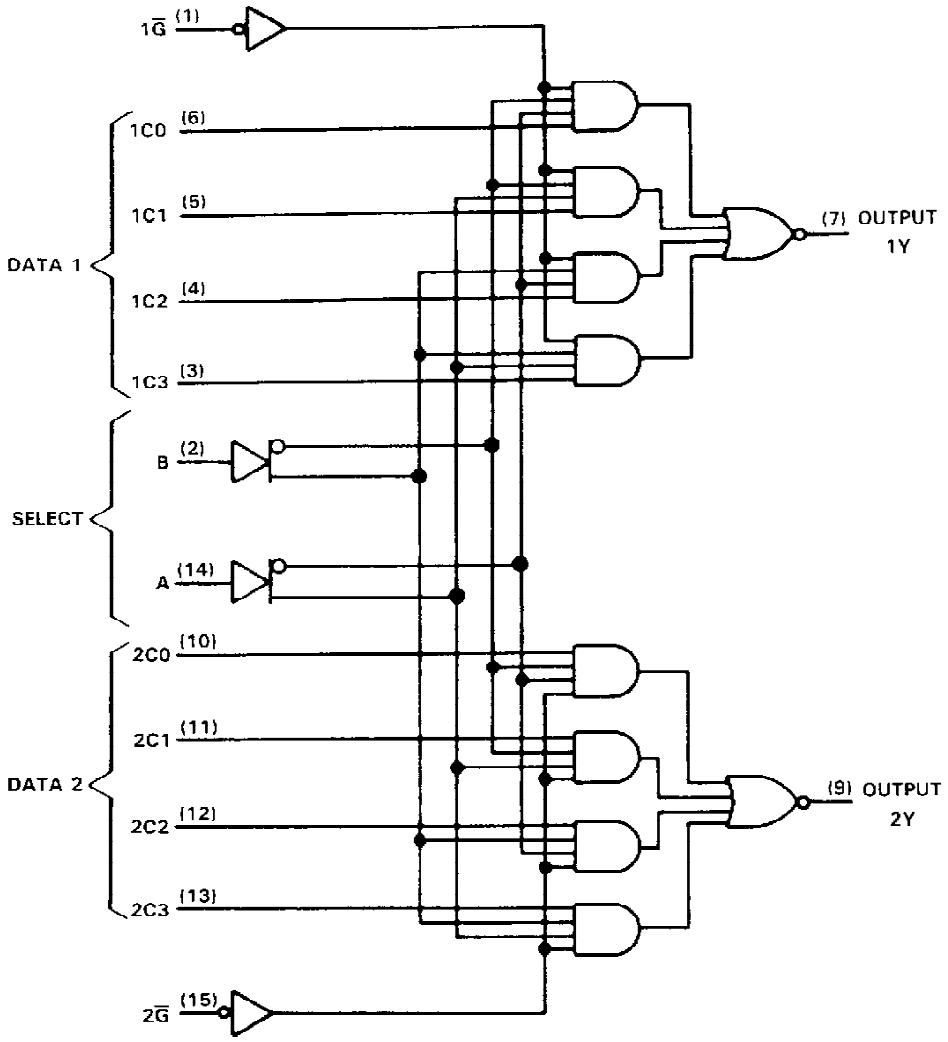
Select inputs A and B are common to both sections.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage†	−1.2 V to 7 V
Input current	−30 mA to 5 mA
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F352	−55°C to 125°C
SN74F352	0°C to 70°C
Storage temperature range	−65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F352			SN74F352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F352			SN74F352			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = −1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCH}	V_{CC} = 5.5 V,			9.3	14		9.3	14	mA
I_{CCL}	V_{CC} = 5.5 V,			13.3	20		13.3	20	

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			'F352			SN54F352		SN74F352		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2.7	7.6	11	2.2	14	2.2	12.5	ns
t_{PHL}			2.2	6.1	8.5	1.7	11	1.7	9.5	
t_{PLH}	G	Y	1.7	4.1	6	1.2	8	1.2	7	ns
t_{PHL}			2.2	4.6	7	1.7	9	1.7	8	
t_{PLH}	Data (Any C)	Y	1.7	4.8	7	1.2	9	1.2	8	ns
t_{PHL}			1	2.1	3.5	1	5	1	4	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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