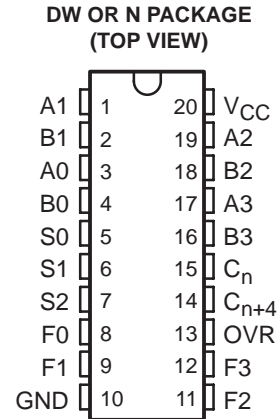


# SN74F382

## ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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- Fully Parallel 4-Bit ALU in 20-Pin Package
- Ideally Suited for High-Density Economical Processors
- Ripple-Carry ( $C_{n+4}$ ) and Overflow (OVR) Outputs
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
  - A Minus B
  - B Minus A
  - A Plus B
  - Five Other Functions
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs



### description

The SN74F382 is an arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, and OR functions of the two Boolean variables are provided without the use of external circuits. In addition, the outputs can be cleared (low) or preset (high) as desired. The device provides a ripple-carry ( $C_{n+4}$ ) output to ripple the carry to the  $C_n$  input of the next stage. It detects and indicates the two's complement overflow condition via the overflow (OVR) output. OVR is logically equivalent to  $C_{n+3} \oplus C_{n+4}$ . When the SN74F382 is cascaded to handle word lengths longer than four bits in length, only the most significant OVR is used.

The SN74F382 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECTION			ARITHMETIC/LOGIC OPERATION
S2	S1	S0	
L	L	L	Clear
L	L	H	B minus A
L	H	L	A minus B
L	H	H	A plus B
H	L	L	$A \oplus B$
H	L	H	$A + B$
H	H	L	AB
H	H	H	Preset

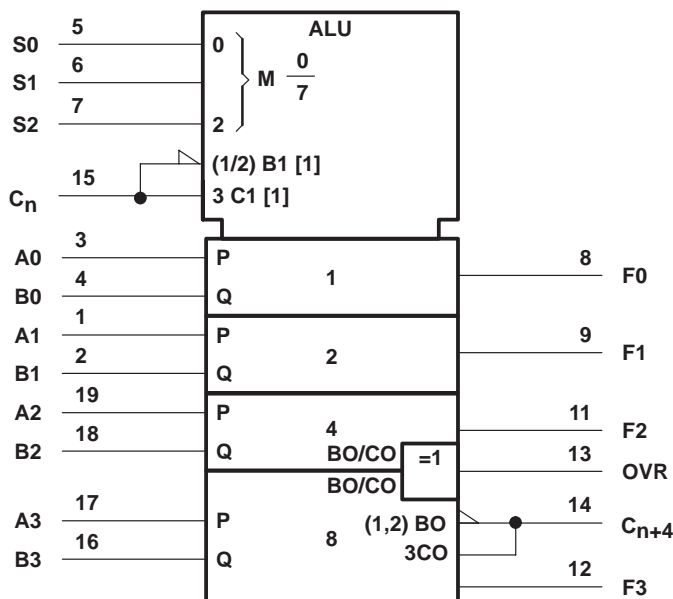
# SN74F382 ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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## PIN DESIGNATIONS

DESIGNATION	PIN NO.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	Word A inputs
B3, B2, B1, B0	16, 18, 2, 4	Word B inputs
S2, S1, S0	7, 6, 5	Function-select inputs
$C_n$	15	Carry input for addition, inverted carry input for subtraction
F3, F2, F1, F0	12, 11, 9, 8	Function outputs
$C_{n+4}$	14	Ripple-carry output
OVR	13	Overflow output
VCC	20	Supply voltage
GND	10	Ground

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## function table

Certain differences exist in the OVR and  $C_{n+4}$  function table compared with similar parts from other technologies and other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B) where these outputs perform valuable cascade functions. There are slight differences in the other modes (clear, A + B,  $A \oplus B$ , AB, and preset), in which these outputs strictly *don't care*.

The following function table is a condensed version and assumes for  $A_n$  that A0, A1, A2, and A3 inputs all agree, and for  $B_n$  that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these OVR and  $C_{n+4}$  outputs in all modes of operation to facilitate incoming inspection.

# SN74F382

## ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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FUNCTION TABLE

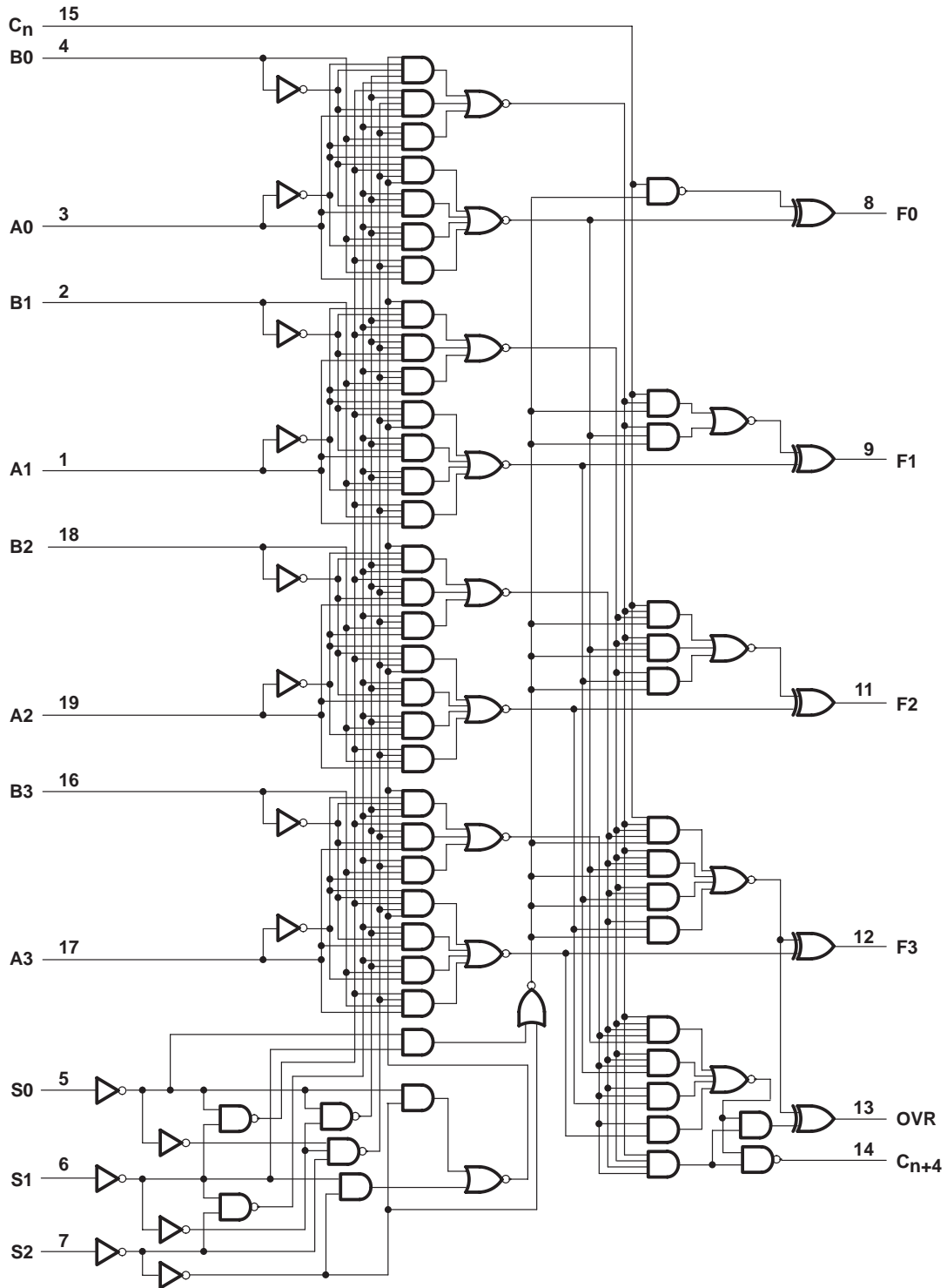
ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				OVR	C <sub>n+4</sub>			
	S2	S1	S0	C <sub>n</sub>	A <sub>n</sub>	B <sub>n</sub>	F3	F2	F1	F0					
Clear	L	L	L	X	X	X	L	L	L	L	H	H			
B minus A	L	L	H	L	L	L	H	H	H	H	L	L			
				L	L	H	H	H	H	L	L	L	L		
				L	H	L	L	L	L	L	L	L	L	L	
				L	H	H	L	L	L	L	L	L	L	L	
				H	L	L	L	L	L	L	L	L	L	L	
				H	L	H	L	L	L	L	L	L	L	L	L
				H	H	H	L	L	L	L	L	L	L	L	L
A minus B	L	H	L	L	L	L	H	H	H	H	L	L			
				L	L	H	L	L	L	L	L	L	L		
				L	H	L	L	L	L	L	L	L	L	L	
				L	H	H	L	L	L	L	L	L	L	L	
				H	L	L	L	L	L	L	L	L	L	L	
				H	L	H	L	L	L	L	L	L	L	L	L
				H	H	H	L	L	L	L	L	L	L	L	L
A plus B	L	H	H	L	L	L	L	L	L	L	L	L			
				L	L	H	H	H	H	L	L	L	L		
				L	H	L	L	L	L	L	L	L	L	L	
				L	H	H	L	L	L	L	L	L	L	L	
				H	L	L	L	L	L	L	L	L	L	L	
				H	L	H	L	L	L	L	L	L	L	L	L
				H	H	H	L	L	L	L	L	L	L	L	L
A ⊕ B	H	L	L	X	L	L	L	L	L	L	L	L			
				X	L	H	H	H	H	H	H	L	L		
				L	H	L	H	H	H	H	H	H	L	L	
				H	H	L	H	H	H	H	H	H	H	H	
				X	H	H	L	L	L	L	L	L	L	L	
A + B	H	L	H	X	L	L	L	L	L	L	L	L			
				X	L	H	H	H	H	H	H	L	L		
				X	H	L	H	H	H	H	H	H	L	L	
				L	H	H	L	L	L	L	L	L	L	L	
				H	H	H	L	L	L	L	L	L	L	L	
AB	H	H	L	X	L	L	L	L	L	L	L	H			
				X	L	H	L	L	L	L	L	L	L		
				X	H	L	L	L	L	L	L	L	L		
				L	H	H	L	L	L	L	L	L	L	L	
				H	H	H	L	L	L	L	L	L	L	L	
Preset	H	H	H	X	L	L	L	H	H	H	H	L			
				X	L	H	H	H	H	H	H	L	L		
				X	H	L	L	L	L	L	L	L	L		
				L	H	H	L	L	L	L	L	L	L		
				H	H	H	L	L	L	L	L	L	L		



# SN74F382 ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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## logic diagram (positive logic)



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## ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–1.2 V to 7 V
Input current range .....	–30 mA to 5 mA
Voltage range applied to any output in the high state .....	–0.5 V to $V_{CC}$
Current into any output in the low state .....	40 mA
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{IK}$ Input clamp current			–18	mA
$I_{OH}$ High-level output current			–1	mA
$I_{OL}$ Low-level output current			20	mA
$T_A$ Operating free-air temperature	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA	2.7			
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.3	0.5	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
$I_{IL}$	Any A or B			–2.4	mA
	Any S	$V_{CC} = 5.5$ V, $V_I = 0.5$ V		–0.6	
	$C_n$			–3	
$I_{OS}§$	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	mA
$I_{CC}$	$V_{CC} = 5.5$ V, See Note 2		54	81	mA

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with all outputs open, S0 and  $C_n$  inputs at 4.5 V, and all other inputs grounded.



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## ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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### switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	C <sub>n</sub>	Any F	2.3	5.3	11	2.3	12	ns
t <sub>PHL</sub>			2.2	4.6	7.5	2.2	8.5	
t <sub>PLH</sub>	Any A or B	Any F	2.7	6.9	12	2.4	13	ns
t <sub>PHL</sub>			2.5	6.1	10	2.3	11	
t <sub>PLH</sub>	S0, S1, S2	Any F	4.7	8.3	15	4.3	17	ns
t <sub>PHL</sub>			3.3	7.5	14	3.3	15	
t <sub>PLH</sub>	Any A or B	C <sub>n+4</sub>	3.3	6.6	10	3.3	11	ns
t <sub>PHL</sub>			3.4	6.3	10	3	10.5	
t <sub>PLH</sub>	S0, S1, S2	OVR or C <sub>n+4</sub>	3.6	9.8	16.5	3	17.5	ns
t <sub>PHL</sub>			5	8.6	13	4.6	14	
t <sub>PLH</sub>	C <sub>n</sub>	C <sub>n+4</sub>	2.2	3.9	5.5	2	6.5	ns
t <sub>PHL</sub>			3	4.8	6.5	2.6	7.5	
t <sub>PLH</sub>	C <sub>n</sub>	OVR	3.3	7	11	3	12.5	ns
t <sub>PHL</sub>			3	5	6.5	3	8	
t <sub>PLH</sub>	Any A or B	OVR	5.1	8.8	13	4.7	15	ns
t <sub>PHL</sub>			3.3	6.9	10.5	3.3	11.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74F382N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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