

SN54S133, SN74S133 13-INPUT POSITIVE-NAND GATES

SDLS202 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

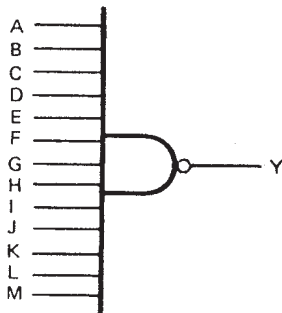
These devices contain a single 13-input NAND gate.

The SN54133 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74133 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

| INPUTS A THRU M | OUTPUT Y |
|----------------------|-------------|
| All inputs H | L |
| One or more inputs L | H |

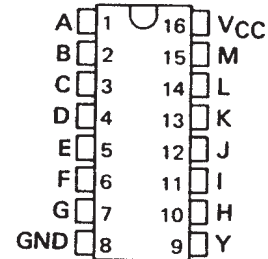
logic diagram



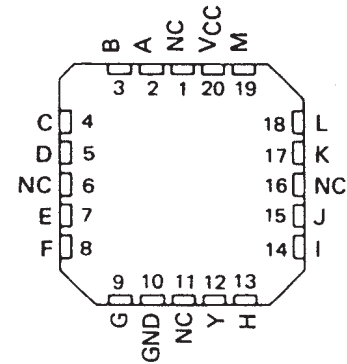
positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M} \text{ or } \overline{A + B + C + D + E + F + G + H + I + J + K + L + M}$$

SN54S133 . . . J OR W PACKAGE
SN74S133 . . . D OR N PACKAGE
(TOP VIEW)

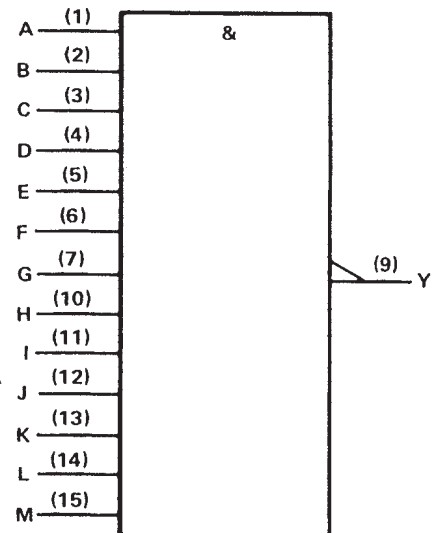


SN54S133 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



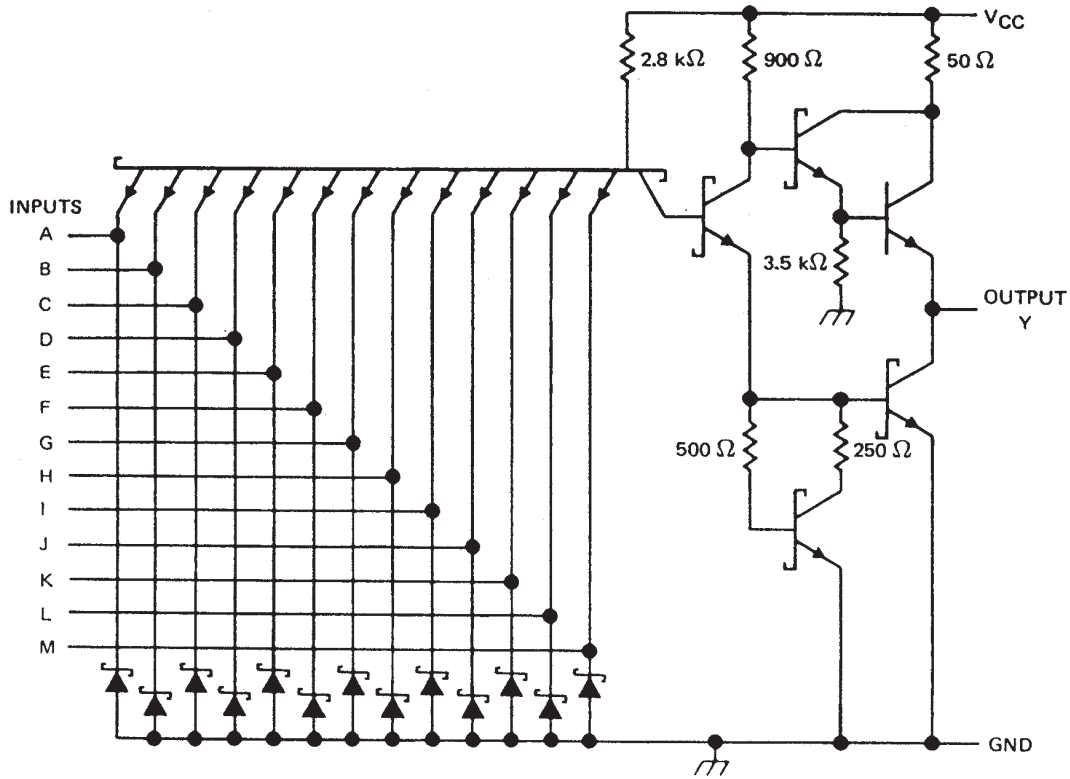
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54S133, SN74S133 13-INPUT POSITIVE-NAND GATES

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'S133



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.



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recommended operating conditions

| | SN54S133 | | | SN74S133 | | | UNIT |
|---|----------|-----|-----|----------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} High-level output current | | | -1 | | | -1 | mA |
| I _{OL} Low-level output current | | | 20 | | | 20 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS † | SN54S133 | | | SN74S133 | | | UNIT |
|-------------------|---|----------|-------|------|----------|-------|------|------|
| | | MIN | TYP ‡ | MAX | MIN | TYP ‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | | -1.2 | | | -1.2 | V |
| V _{OH} | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA | | | 0.5 | | | 0.5 | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | 50 | | | 50 | μA |
| I _{IL} | V _{CC} = MAX, V _I = 0.5 V | | | -2 | | | -2 | mA |
| I _{OS} § | V _{CC} = MAX | -40 | | -100 | -40 | | -100 | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | | 3 | 5 | | 3 | 5 | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | | 5.5 | 10 | | 5.5 | 10 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|--|-----|-----|-----|------|
| t _{PLH} | Any | Y | R _L = 280 Ω, C _L = 15 pF | | 4 | 6 | ns |
| t _{PHL} | | | | | 4.5 | 7 | ns |
| t _{PLH} | | | R _L = 280 Ω, C _L = 50 pF | | 5.5 | | ns |
| t _{PHL} | | | | | 6.5 | | ns |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|---------------------------------|
| JM38510/07009BEA | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Replaced by JM38510/37005BEA |
| JM38510/07009BFA | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| JM38510/07009BFA | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN54S133J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Replaced by SN54ALS133J |
| SN54S133J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Replaced by SN54ALS133J |
| SN74S133D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133DR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133DR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74S133N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SNJ54S133FK | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | Replaced by SNJ54ALS133FK |
| SNJ54S133FK | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | Replaced by SNJ54ALS133FK |
| SNJ54S133J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Replaced by SNJ54ALS133J |
| SNJ54S133J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | Replaced by SNJ54ALS133J |
| SNJ54S133W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | Samples Not Available |
| SNJ54S133W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | Samples Not Available |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54S133, SN74S133 :

● Catalog: [SN74S133](#)

● Military: [SN54S133](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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