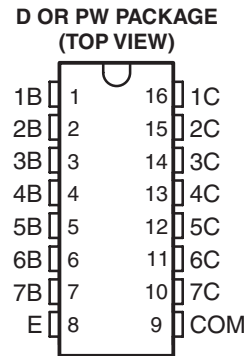


HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

Check for Samples: [ULQ2003A-Q1](#), [ULQ2004A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications



DESCRIPTION

The ULQ2003A and ULQ2004A are high-voltage high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULQ2003A has a 2.7-k Ω series base resistor for each Darlington pair, for operation directly with TTL or 5-V CMOS devices. The ULQ2004A has a 10.5-k Ω series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULQ2004A is below that of the ULQ2003A.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 105°C	SOIC – D	Tube of 40	ULQ2003ATDQ1	
		Reel of 2500	ULQ2003ATDRQ1	
	SOIC – D	Tube of 40	ULQ2004ATDQ1	Product Preview
		Reel of 2500	ULQ2004ATDRQ1	ULQ2004AT
–40°C to 125°C	TSSOP – PW	Reel of 2000	ULQ2003ATPWRQ1	U2003AT
	SOIC – D	Reel of 2500	ULQ2003AQDRQ1	ULQ2003AQ

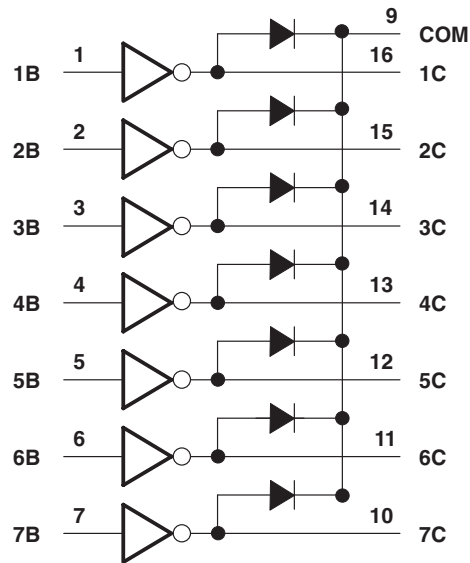
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

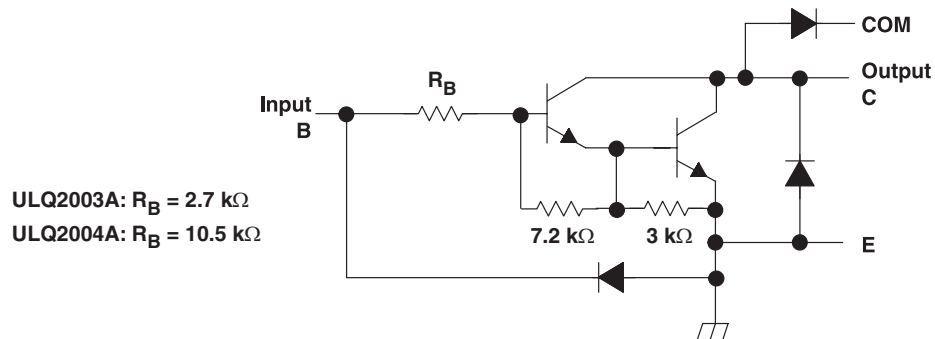


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM



SCHEMATICS (EACH DARLINGTON PAIR)



- A. All resistor values shown are nominal.
- B. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Collector-emitter voltage		50	V	
	Clamp diode reverse voltage ⁽²⁾		50	V	
V _I	Input voltage ⁽²⁾		30	V	
	Peak collector current	See Figure 14	500	mA	
I _{OK}	Output clamp current		500	mA	
	Total emitter-terminal current		-2.5	A	
P _D	Continuous total power dissipation	See <i>Dissipation Ratings Table</i>			
T _A	Operating free-air temperature range	ULQ200xAT	-40	105	°C
		ULQ200xAQ	-40	125	
θ _{JA}	Package thermal impedance ^{(3) (4)}	D package		73	°C/W
		PW package		108	
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATINGS

PACKAGE	T _A = 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING	T _A = 105°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW	342 mW	190 mW

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS		ULQ2003AT			ULQ2003AQ			ULQ2004AT			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	Figure 6	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$									5	V
			$I_C = 200\text{ mA}$		2.7		2.7					6	
			$I_C = 250\text{ mA}$		2.9		2.9						
			$I_C = 275\text{ mA}$									7	
			$I_C = 300\text{ mA}$			3		3					
			$I_C = 350\text{ mA}$									8	
$V_{CE(sat)}$ Collector-emitter saturation voltage	Figure 5		$I_I = 250\text{ }\mu\text{A}$, $I_C = 100\text{ mA}$	0.9	1.2		1	1.3		0.9	1.1		V
			$I_I = 350\text{ }\mu\text{A}$, $I_C = 200\text{ mA}$		1	1.4		1	1.5		1	1.3	
			$I_I = 500\text{ }\mu\text{A}$, $I_C = 350\text{ mA}$		1.2	1.7		1.2	1.8		1.2	1.6	
I_{CEX} Collector cutoff current	Figure 1	$V_{CE} = 50\text{ V}$, $I_I = 0$	$T_A = 25^\circ\text{C}$			100			100			50	μA
			$T_A = 105^\circ\text{C}$			165							
	Figure 2	$V_{CE} = 50\text{ V}$	$I_I = 0$									100	
			$V_I = 1\text{ V}$									500	
V_F Clamp forward voltage	Figure 8	$I_F = 350\text{ mA}$			1.7	2.2		1.7	2.2		1.7	2.1	V
$I_{I(off)}$ Off-state input current	Figure 3	$V_{CE} = 50\text{ V}$, $I_C = 500\text{ }\mu\text{A}$		30	65		30	65		50	65	μA	
I_I Input current	Figure 4	$V_I = 3.85\text{ V}$			0.93	1.35		0.93	1.35				mA
		$V_I = 5\text{ V}$									0.35	0.5	
		$V_I = 12\text{ V}$										1	
I_R Clamp reverse current	Figure 7	$V_R = 50\text{ V}$	$T_A = 25^\circ\text{C}$			100			100			50	μA
						100			100			100	
C_i Input capacitance		$V_I = 0$,	$f = 1\text{ MHz}$		15	25		15	25		15	25	pF

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	ULQ2003A, ULQ2004A			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low- to high-level output	See Figure 9		1	10	μs
t_{PHL} Propagation delay time, high- to low-level output	See Figure 9		1	10	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O = 300\text{ mA}$, See Figure 10		$V_S - 500$		mV

PARAMETER MEASUREMENT INFORMATION

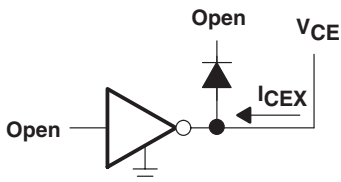


Figure 1. I_{CEX} Test Circuit

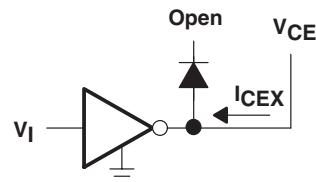


Figure 2. I_{CEX} Test Circuit

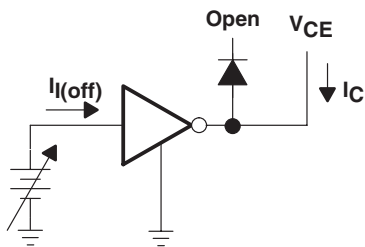


Figure 3. $I_{I(off)}$ Test Circuit

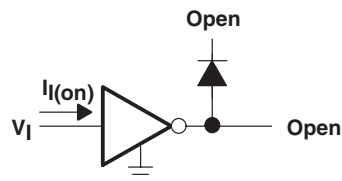


Figure 4. I_I Test Circuit

C. I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

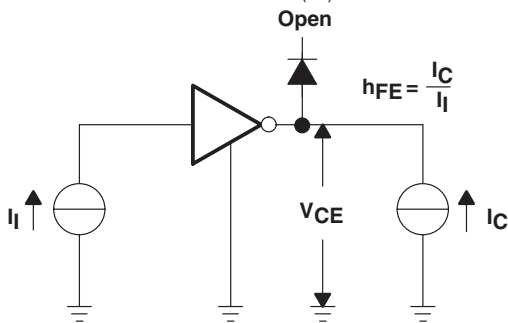


Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

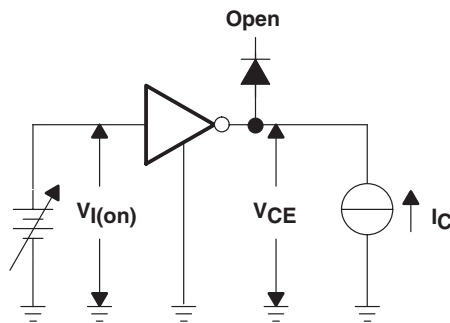


Figure 6. $V_{I(on)}$ Test Circuit

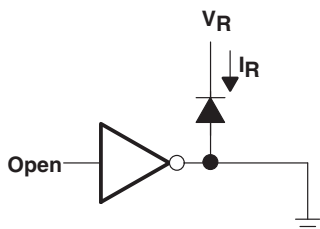


Figure 7. I_R Test Circuit

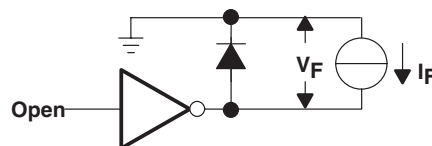
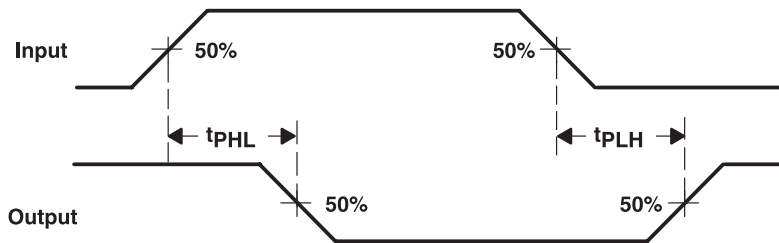


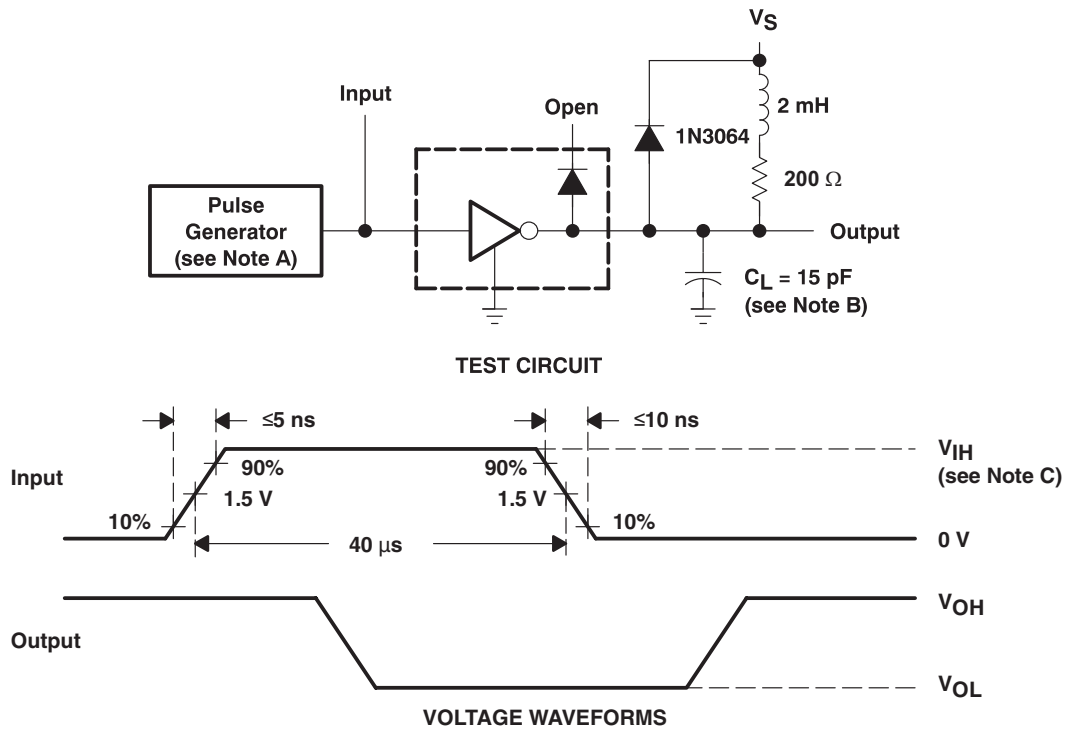
Figure 8. V_F Test Circuit



VOLTAGE WAVEFORMS

Figure 9. Propagation Delay-Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. For testing the ULQ2003A, $V_{IH} = 3 \text{ V}$; for the ULQ2004A, $V_{IH} = 8 \text{ V}$.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

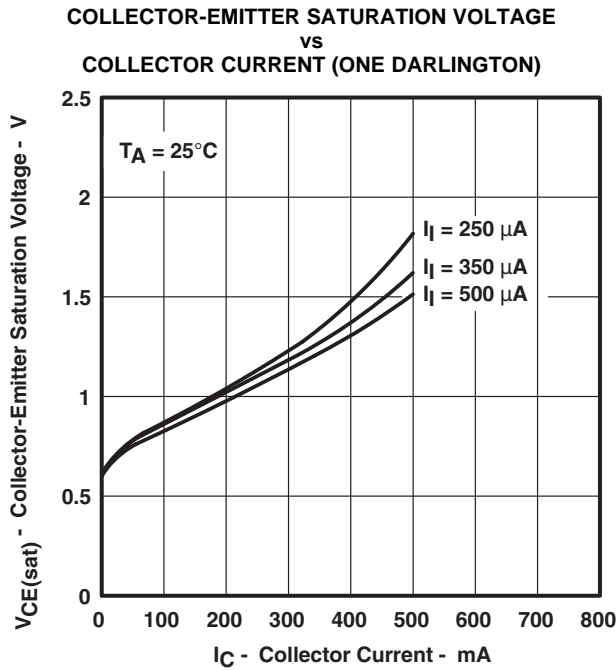


Figure 11.

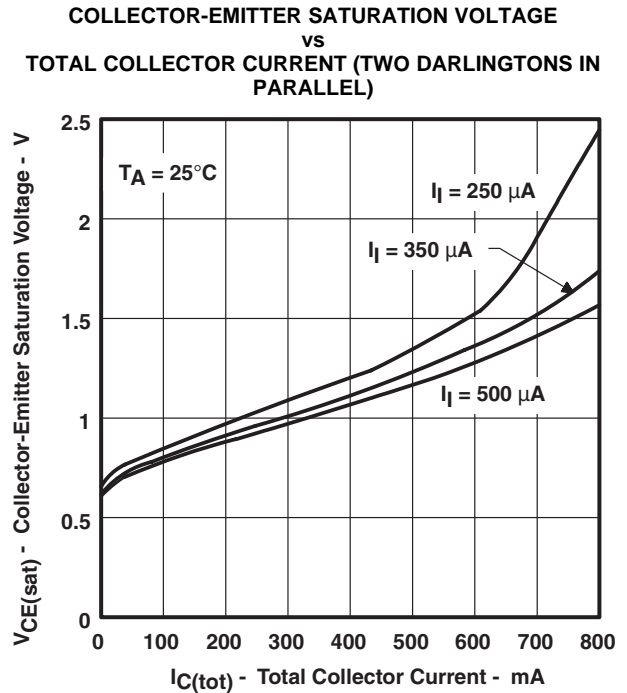


Figure 12.

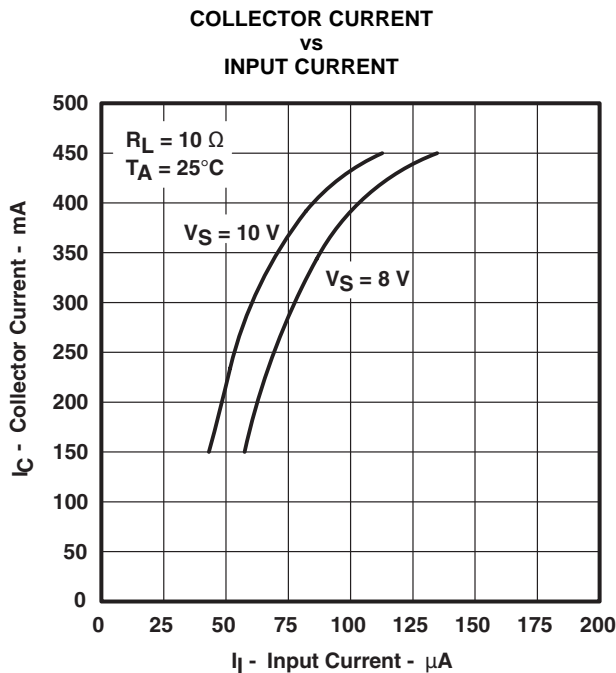


Figure 13.

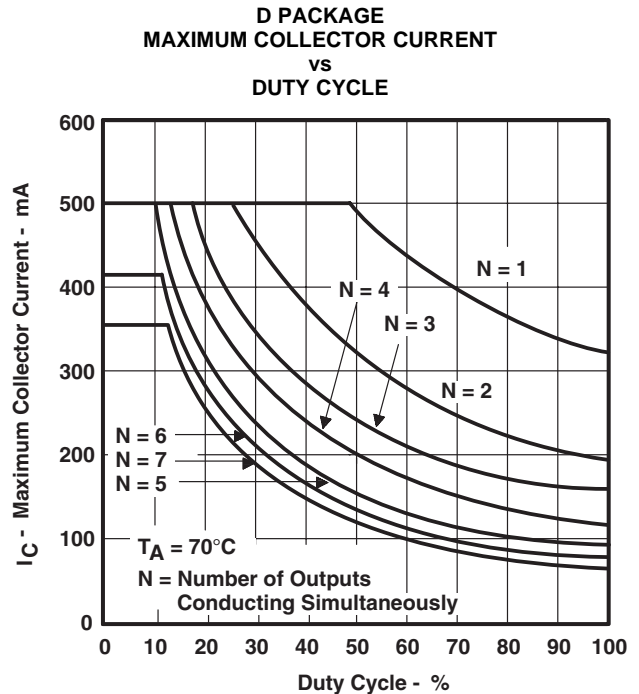


Figure 14.

APPLICATION INFORMATION

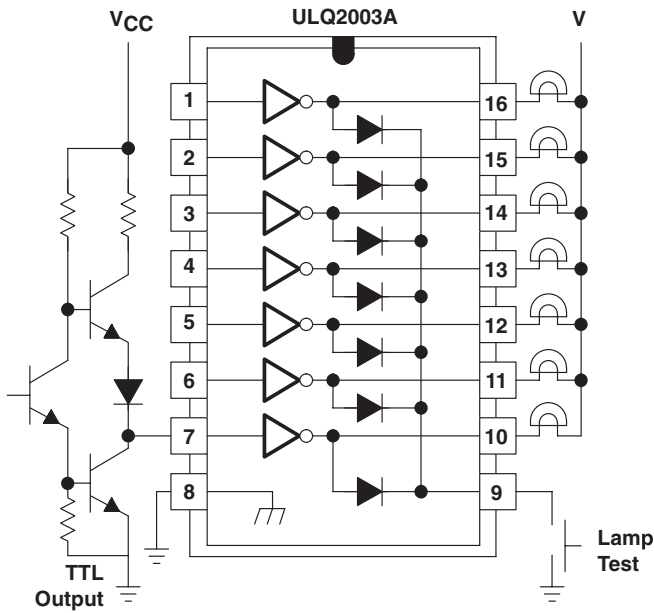


Figure 15. TTL to Load

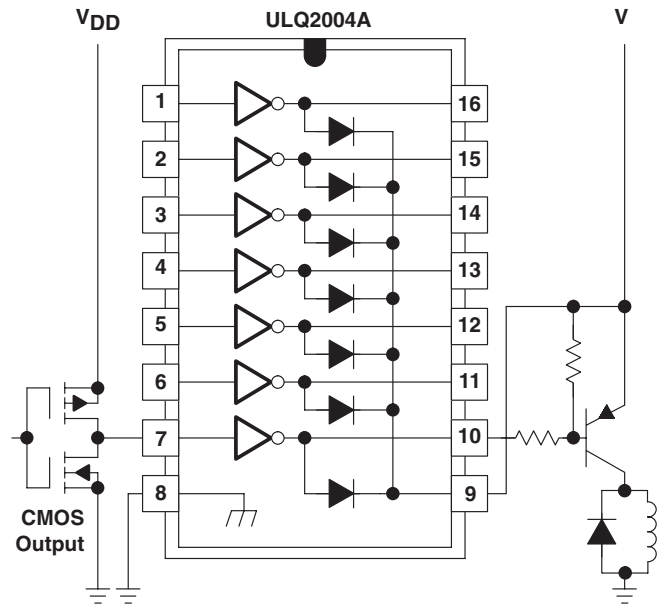


Figure 16. Buffer for Higher Current Loads

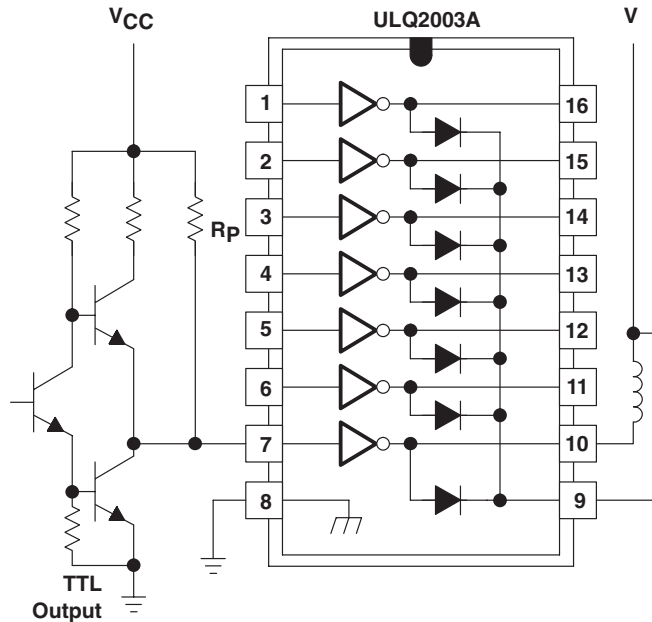


Figure 17. Use of Pullup Resistors to Increase Drive Current

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
ULQ2003AQDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDG4Q1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDQ1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2003ATPWRQ1	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2004ATDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
ULQ2004ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF ULQ2003A-Q1, ULQ2004A-Q1 :

- Catalog: [ULQ2003A](#), [ULQ2004A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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