

## DUAL MICROPOWER LinCMOS™ VOLTAGE COMPARATOR

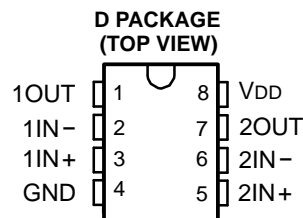
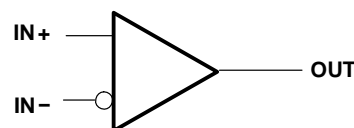
Check for Samples: [TLC393-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- AEC Q100 Qualified with the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- ESD Protection Exceeds 500 V Per MIL-STD-883, Method 3015; Exceeds 50 V Using Machine Model (C = 200 pF, R = 0)
- Low Power: 110  $\mu\text{W}$  Typ at 5 V
- Fast Response Time:  $t_{\text{PLH}} = 2.5 \mu\text{s}$  Typ With 5-mV Overdrive
- Single Supply Operation:
  - TLC393Q: 4 V to 16 V

### APPLICATIONS

- Automotive Applications


**symbol (each comparator)**


### DESCRIPTION

The TLC393 consists of dual independent micropower voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses one-twentieth the power for similar response times. The open-drain MOS output stage interfaces to a variety of loads and supplies. For a similar device with a push-pull output configuration see the TLC3702 data sheet.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393Q is characterized for operation over the full automotive temperature range of  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

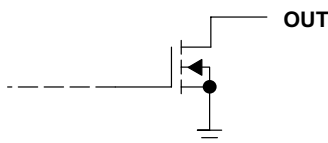
### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	$V_{\text{IOmax}}$ AT $25^{\circ}\text{C}$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	5 mV	SOIC (D)	Tape and reel	TLC393QDRQ1	C393Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

(2) Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

### Schematic


**OPEN-DRAIN CMOS OUTPUT**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	VALUE		UNIT
	MIN	MAX	
Supply voltage range, $V_{DD}$ <sup>(2)</sup>	-0.3	18	V
Differential input voltage, $V_{ID}$ <sup>(3)</sup>		±18	V
Input voltage range, $V_I$	-0.3	$V_{DD}$	V
Output voltage range, $V_O$	-0.3	16	V
Input current, $I_I$		±5	mA
Output current, $I_O$		20	mA
Total supply current into $V_{DD}$		40	mA
Total current out of GND		40	mA
Package thermal impedance, $\theta_{JA}$ <sup>(4), (5)</sup>	D Package	126	°C/W
	PW Package	149	°C/W
Electrostatic discharge (ESD)	Human Body Model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charge Device Model (CDM) AEC-Q100 Classification Level C4B	750	V
Operating free-air temperature range	-40	125	°C
Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$	4	5	16	V
Common-mode input voltage, $V_{IC}$	0		$V_{DD} - 1.5$	V
Low-level output current, $I_{OL}$			20	mA
Operating free-air temperature, $T_A$	-40		125	°C

## ELECTRICAL CHARACTERISTICS

 at specified operating free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = V_{ICRmin}$ , $V_{DD} = 5\text{ V to }10\text{ V}$ , See <sup>(2)</sup>	25°C		1.4	5	mV
			–40°C to 125°C			10	
$I_{IO}$	Input offset current	$V_{IC} = 2.5\text{ V}$	25°C		1		pA
			125°C			15	nA
$I_{IB}$	Input bias current	$V_{IC} = 2.5\text{ V}$	25°C		5		pA
			125°C			30	nA
$V_{ICR}$	Common-mode input voltage range		25°C	0 to $V_{DD} - 1$			V
			–40°C to 125°C	0 to $V_{DD} - 1.5$			
CMMR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C		84		dB
			125°C		84		
			–40°C		84		
$k_{SVR}$	Supply-voltage rejection ratio	$V_{DD} = 5\text{ V to }10\text{ V}$	25°C		85		dB
			125°C		84		
			–40°C		84		
$V_{OL}$	Low-level output voltage	$V_{ID} = -1\text{ V}$ , $I_{OL} = 6\text{ mA}$	25°C		300	400	mV
			125°C			800	
$I_{OH}$	High-level output current	$V_{ID} = 1\text{ V}$ , $V_O = 5\text{ V}$	25°C		0.8	40	nA
			125°C			1	∞A
$I_{DD}$	Supply current (both comparators)	Outputs low, No load	25°C		22	40	∞A
			–40°C to 125°C			90	

(1) All characteristics are measured with zero common-mode voltage unless otherwise noted.

(2) The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V (with a 2.5-kM load to VDD).

## SWITCHING CHARACTERISTICS

 $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 3)

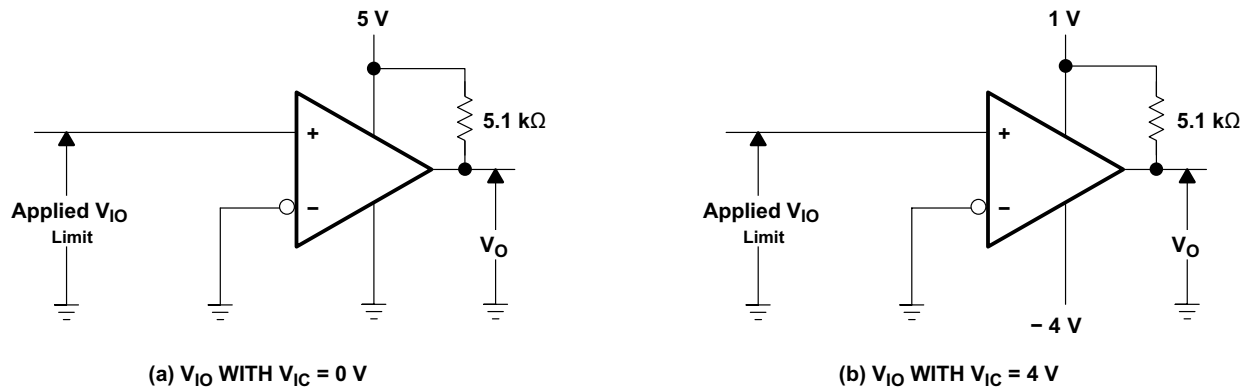
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$t_{PLH}$	Propagation delay time, low-to-high level output	$f = 10\text{ kHz}$ , $C_L = 15\text{ pF}$	Overdrive = 2 mV		4.5		∞s	
			Overdrive = 5 mV		2.5			
			Overdrive = 10 mV		1.7			
			Overdrive = 20 mV		1.2			
			Overdrive = 40 mV		1.1			
$t_{PHL}$	Propagation delay time, high-to-low level output	$f = 10\text{ kHz}$ , $C_L = 15\text{ pF}$	$V_I = 1.4\text{-V step at IN +}$		1.1		∞s	
			Overdrive = 2 mV		3.6			
				Overdrive = 5 mV		2.1		
				Overdrive = 10 mV		1.3		
				Overdrive = 20 mV		0.85		
				Overdrive = 40 mV		0.55		
			$V_I = 1.4\text{-V step at IN +}$		0.1			
$t_f$	Fall time, output	$f = 10\text{ kHz}$ , $C_L = 15\text{ pF}$	Overdrive = 50 mV		22		∞s	

## PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection ratio, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the  $V_{ICR}$  test, rather than changing the input voltages, to provide greater accuracy.



**Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits**

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

The voltage divider formed by R9 and R10 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION (continued)

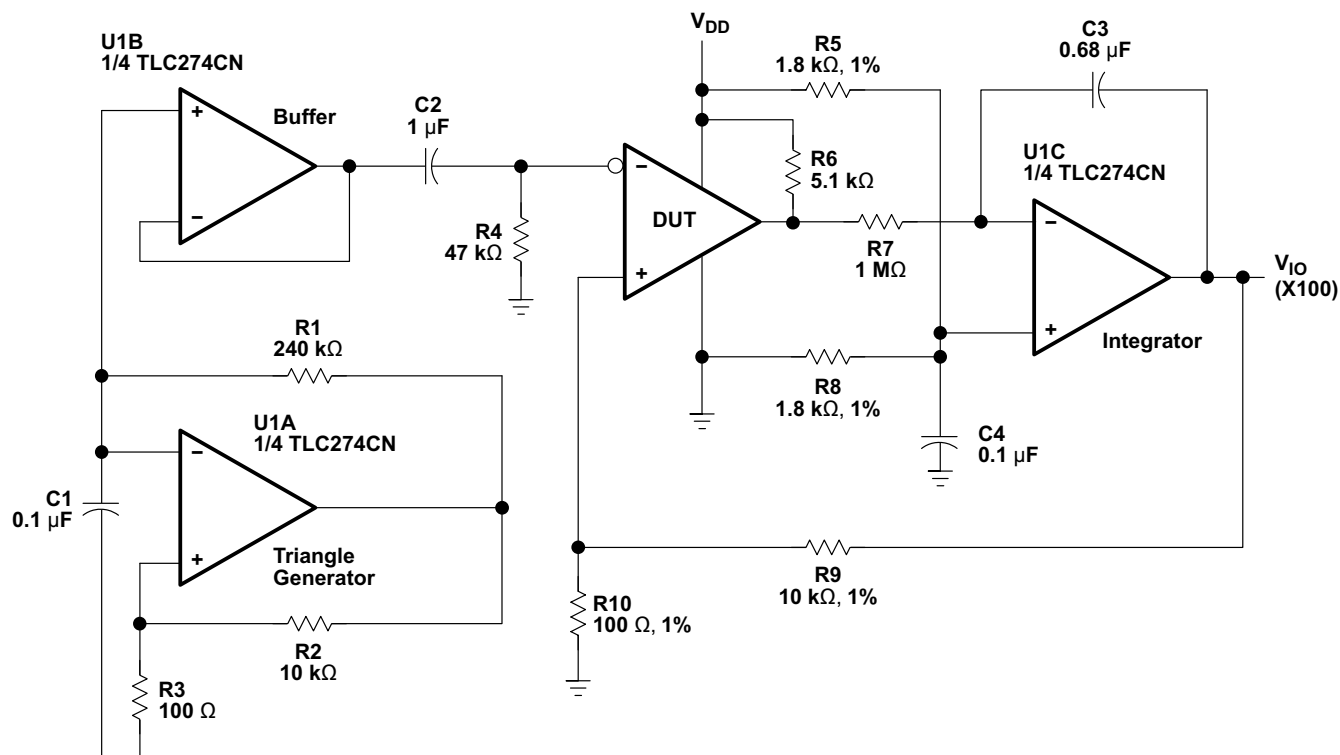
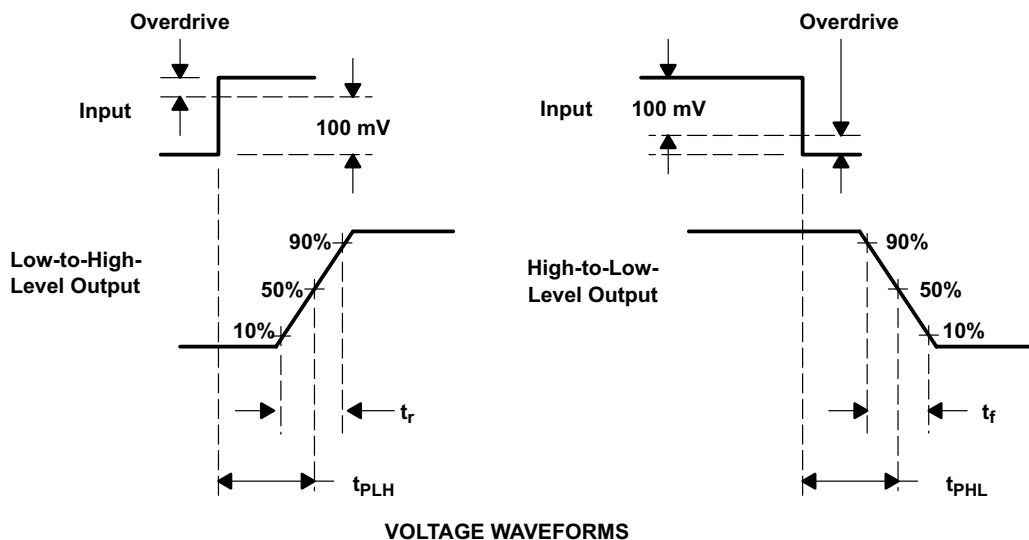
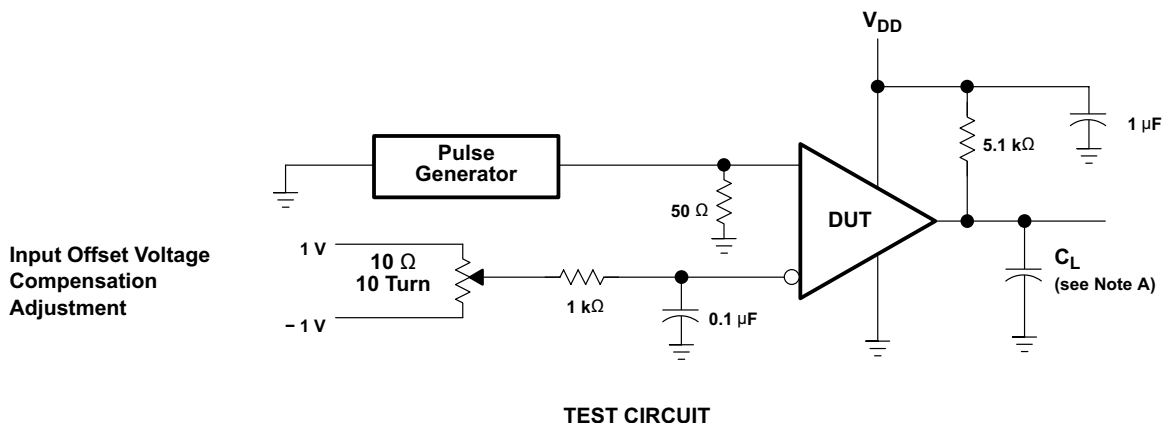


Figure 2. Circuit for Input Offset Voltage Measurement

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105 mV or 5 mV overdrive, causes the output to change state.

PARAMETER MEASUREMENT INFORMATION (continued)



A.  $C_L$  includes probe and jig capacitance.

**Figure 3. Propagation Delay, Rise Time, and Fall Time Circuit and Voltage Waveforms**

**Table 1. Table of Graphs**

			<b>FIGURE</b>
$V_{IO}$	Input offset voltage	Distribution	<a href="#">Figure 4</a>
$I_{IB}$	Input bias current	vs Free-air temperature	<a href="#">Figure 5</a>
CMRR	Common-mode rejection ratio	vs Free-air temperature	<a href="#">Figure 6</a>
$k_{SVR}$	Supply-voltage rejection ratio	vs Free-air temperature	<a href="#">Figure 7</a>
$V_{OL}$	Low-level output voltage	vs Low-level output current	<a href="#">Figure 8</a>
		vs Free-air temperature	<a href="#">Figure 9</a>
$I_{OH}$	Low-level output current	vs High-level output voltage	<a href="#">Figure 10</a>
		vs Free-air temperature	<a href="#">Figure 11</a>
$I_{DD}$	Supply current	vs Supply voltage	<a href="#">Figure 12</a>
		vs Free-air temperature	<a href="#">Figure 13</a>
$t_{PLH}$	Low-to-high level output propagation delay time	vs Supply voltage	<a href="#">Figure 14</a>
$t_{PHL}$	High-to-low level output propagation delay time	vs Supply voltage	<a href="#">Figure 15</a>
	Low-to-high-level output response	Low-to-high level output propagation delay time	<a href="#">Figure 16</a>
	High-to-low level output response	High-to-low level output propagation delay time	<a href="#">Figure 17</a>
$t_f$	Fall time	vs Supply voltage	<a href="#">Figure 18</a>

### TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the related operating free-air temperature ranges of the various devices.

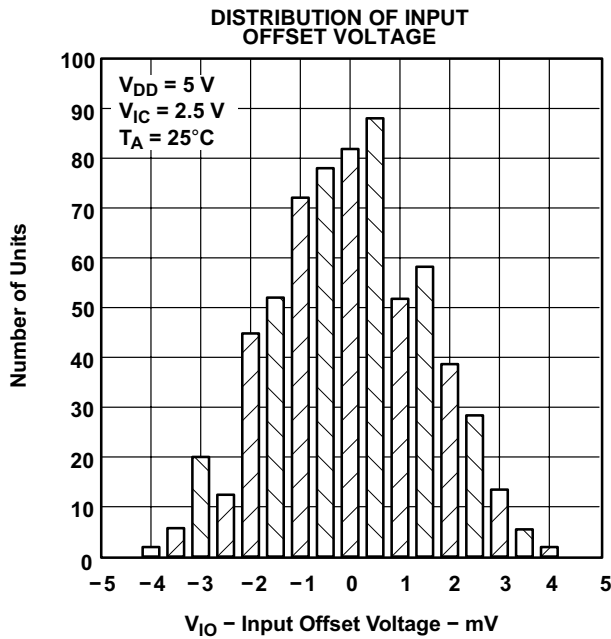


Figure 4.

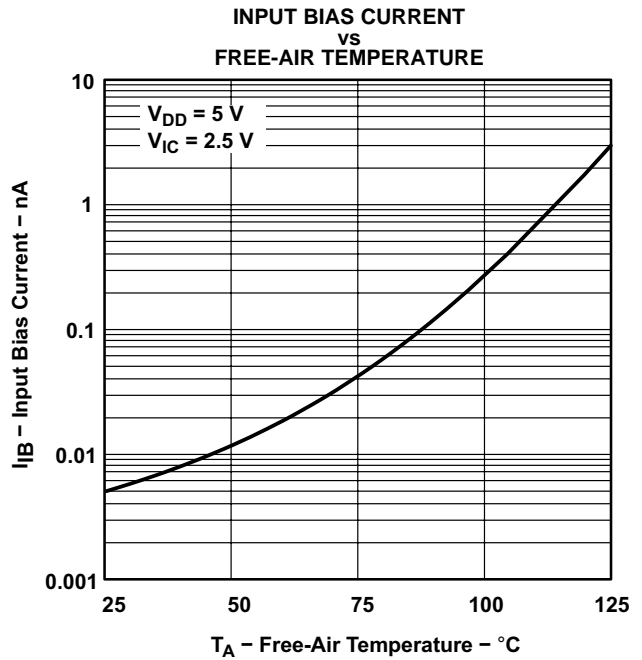


Figure 5.

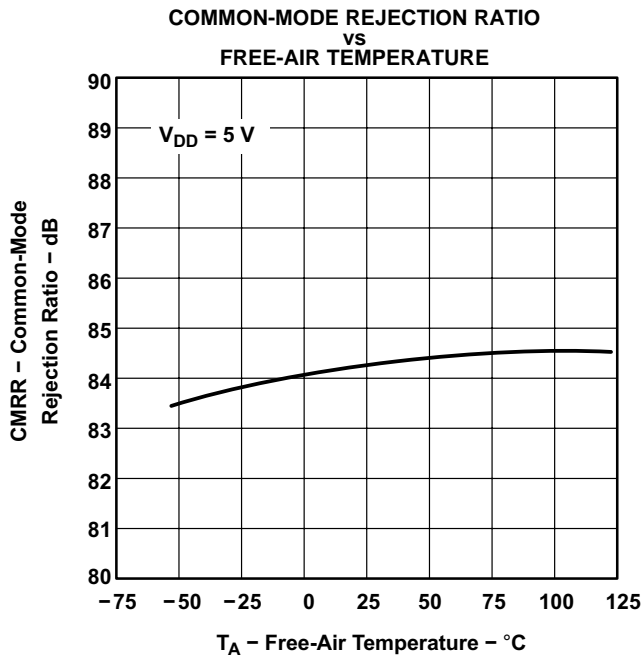


Figure 6.

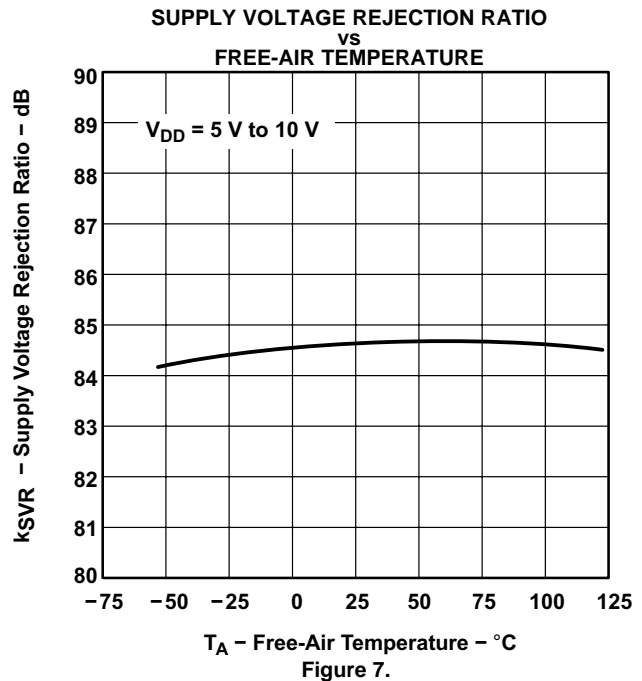


Figure 7.



**TYPICAL CHARACTERISTICS (continued)**

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

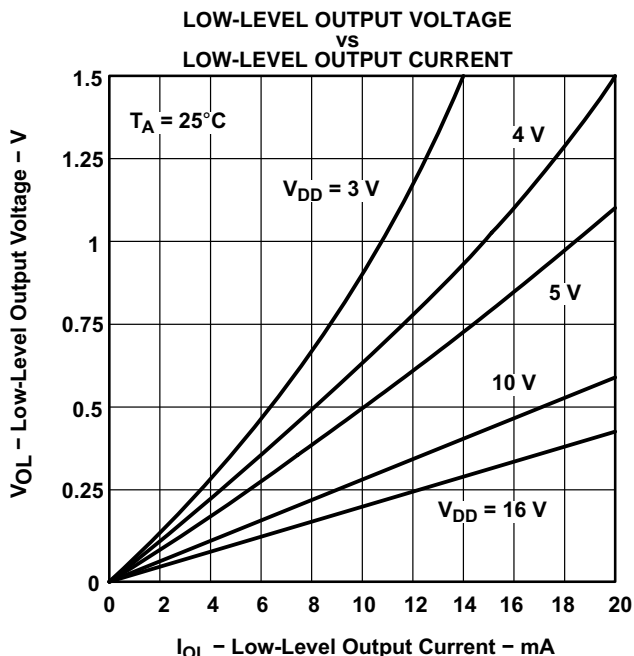


Figure 8.

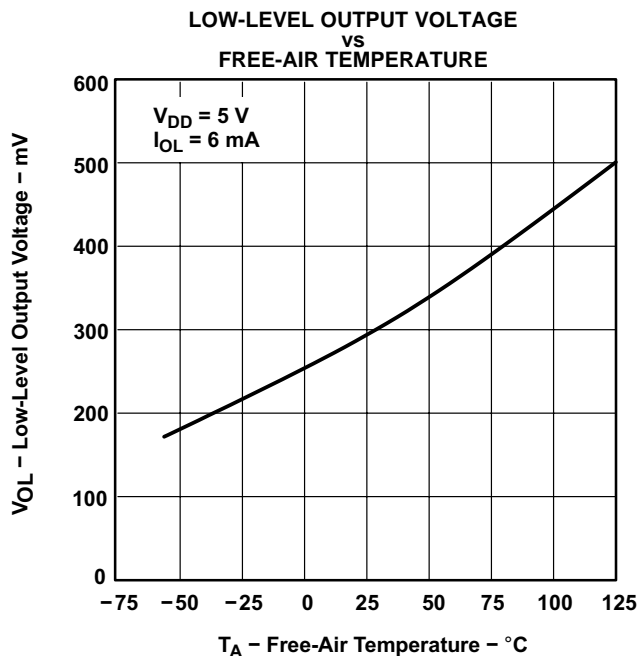


Figure 9.

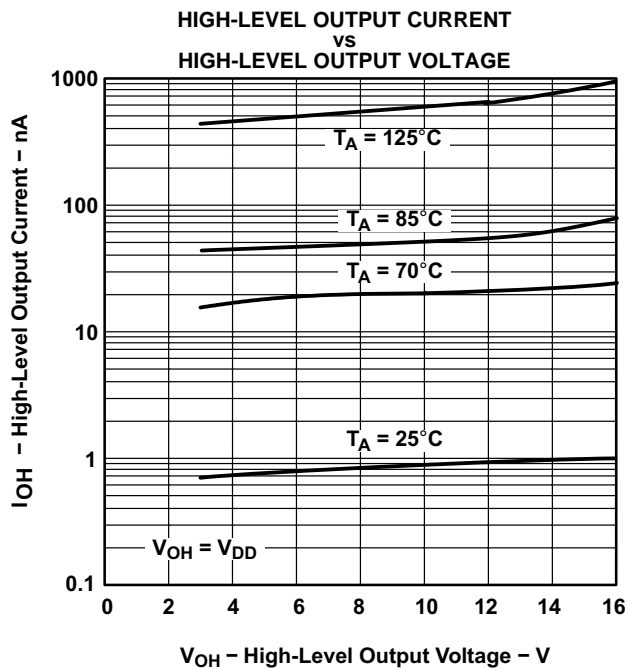


Figure 10.

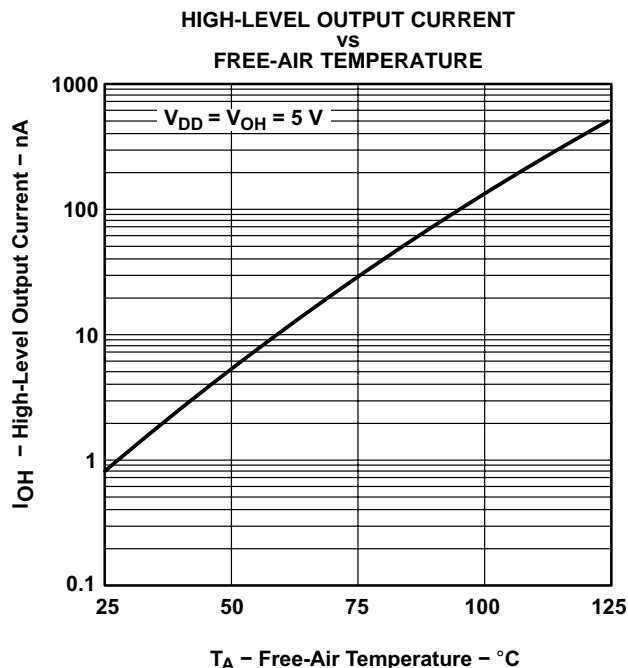
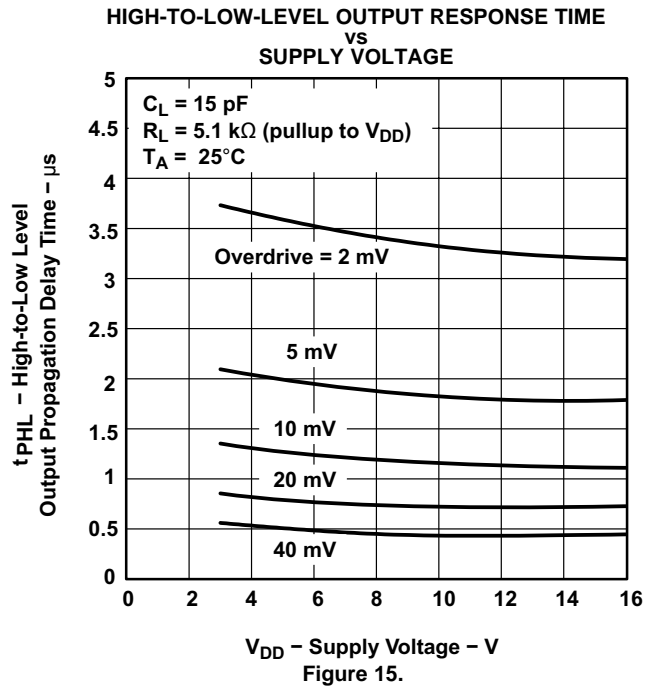
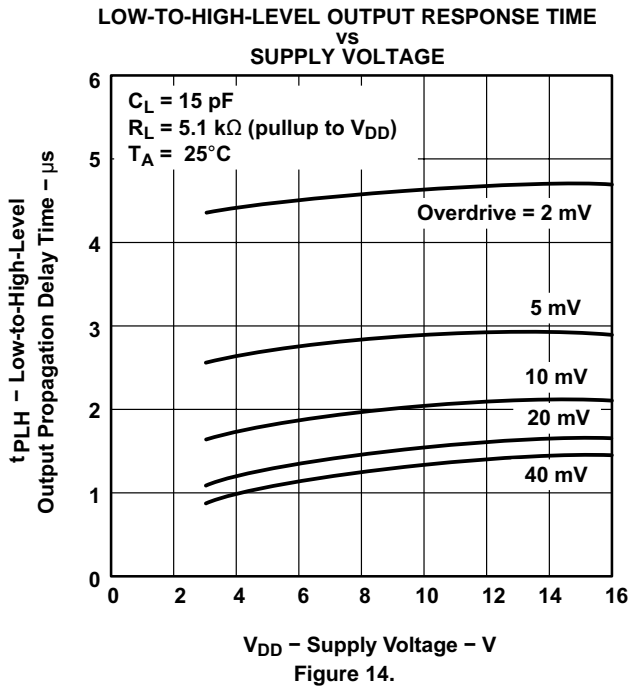
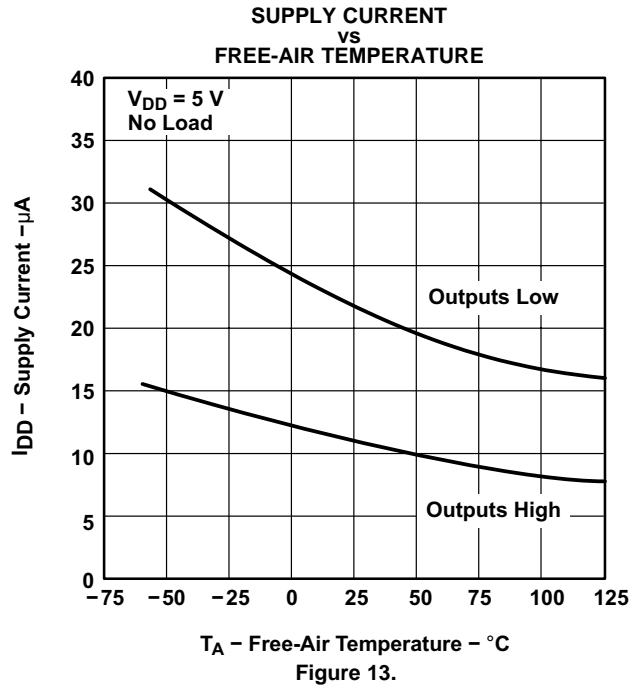
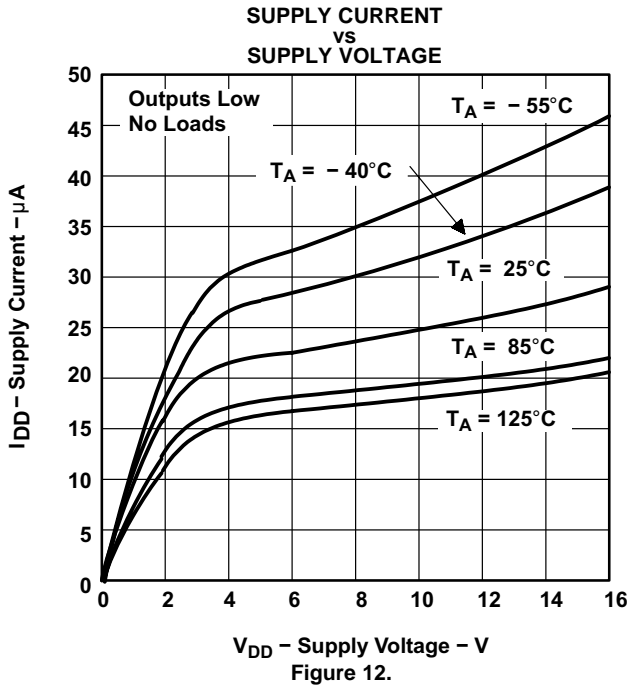


Figure 11.

**TYPICAL CHARACTERISTICS (continued)**

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



**TYPICAL CHARACTERISTICS (continued)**

Data at high and low temperatures are applicable only within the reated operating free-air temperature ranges of the various devices.

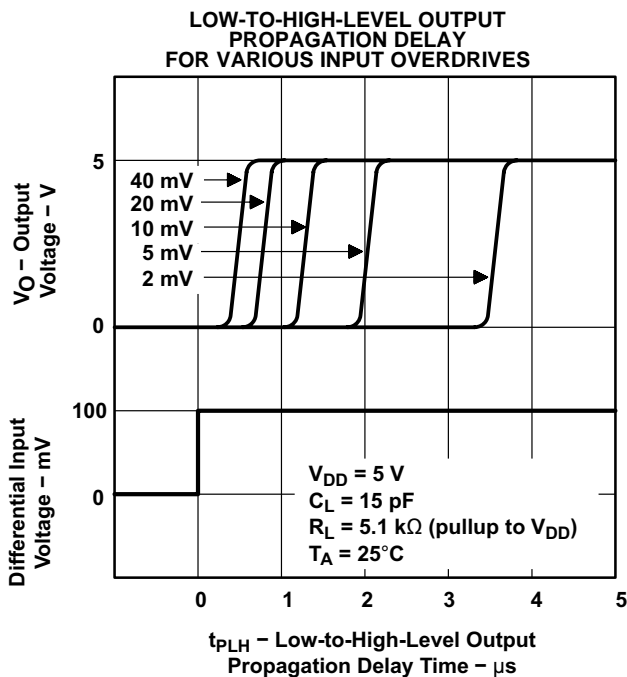


Figure 16.

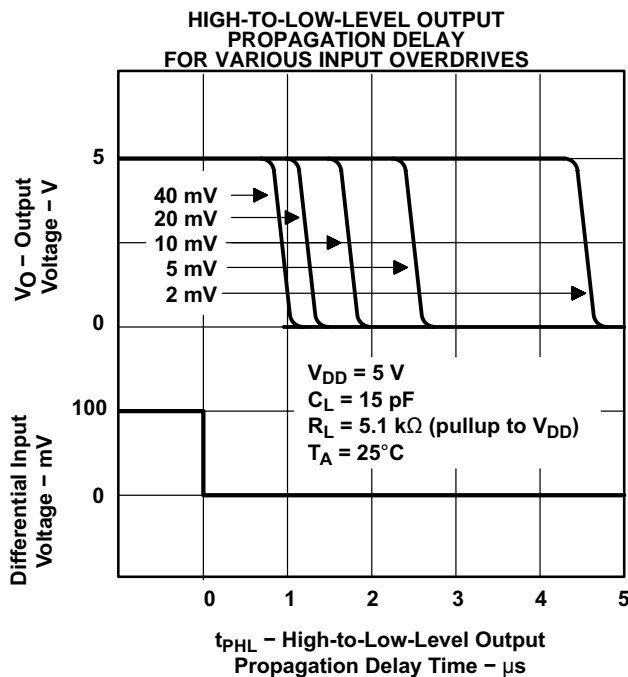


Figure 17.

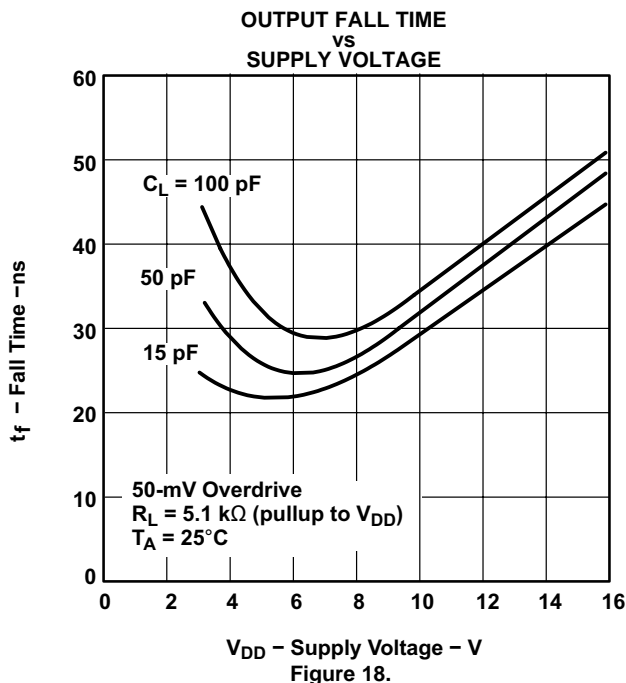


Figure 18.

APPLICATION INFORMATION

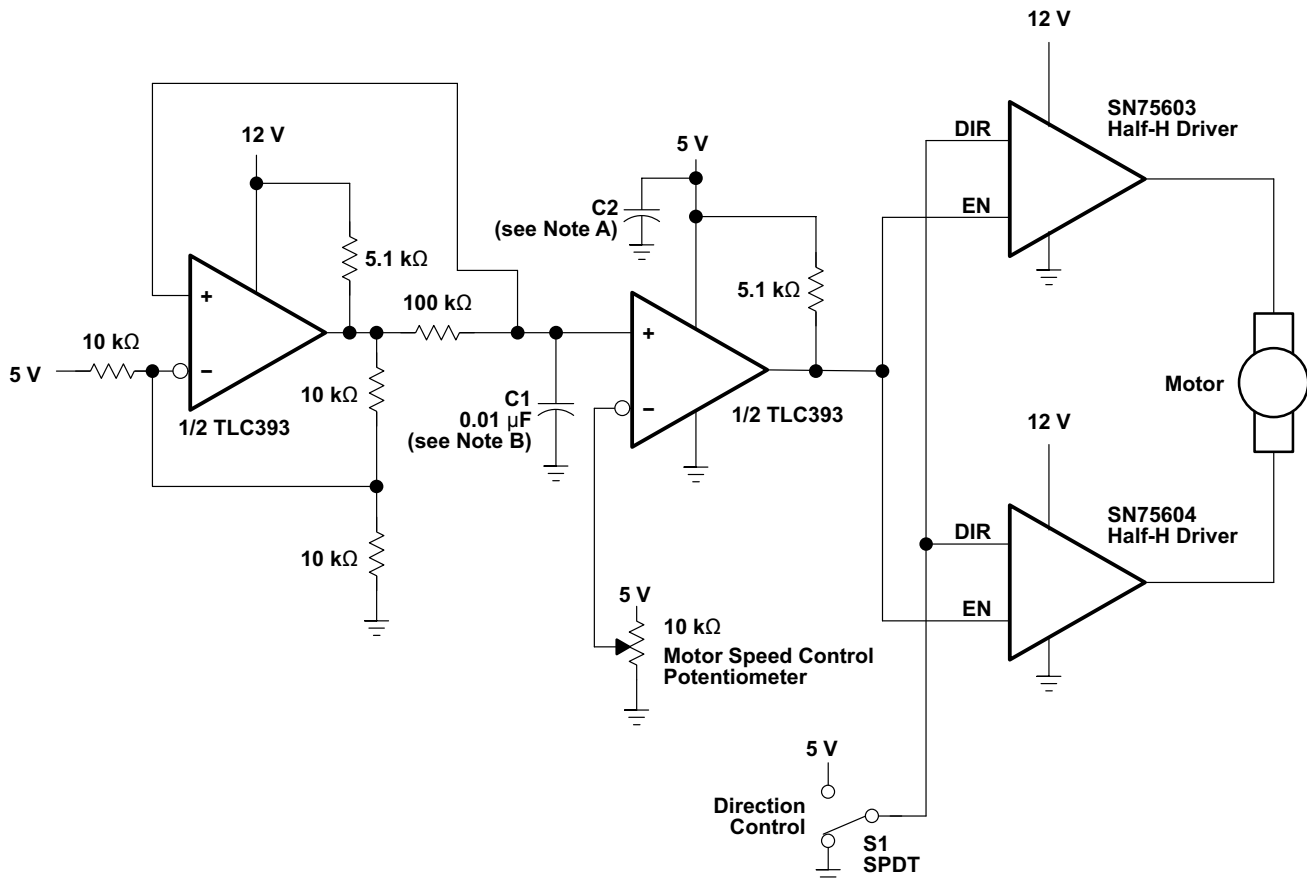
The input should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with  $V_{DD} = 5\text{ V}$ , both inputs must remain between  $-0.2\text{ V}$  and  $4\text{ V}$  to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor ( $0.1\text{-}\mu\text{F}$ ) positioned as close to the device as possible.

The TLC393 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

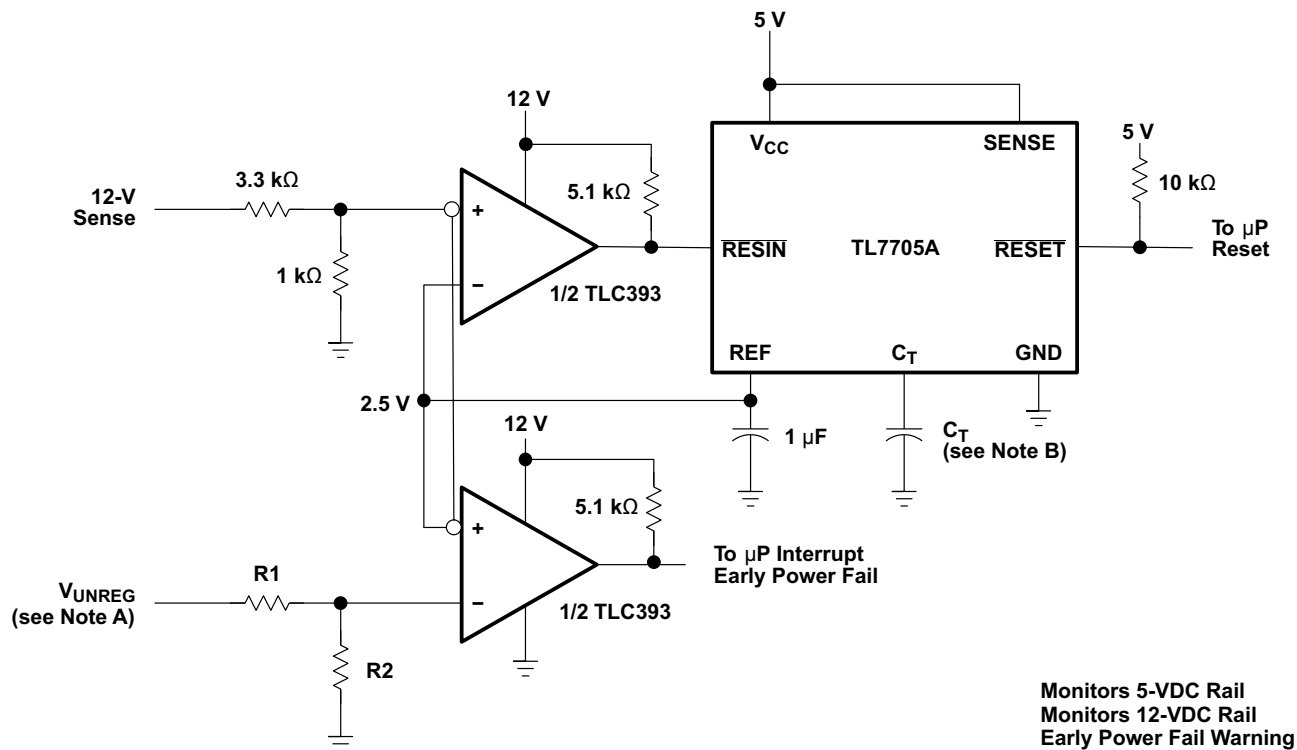
Table 2. Table of Applications

	FIGURE
Pulse-Width-Modulated Motor Speed Controller	Figure 19
Enhanced Supply Supervisor	Figure 20
Two-Phase Nonoverlapping Clock Generator	Figure 21



- A. The recommended minimum capacitance is  $10\text{ }\mu\text{F}$  to eliminate common ground switching noise.
- B. Adjust C1 for change in oscillator frequency.

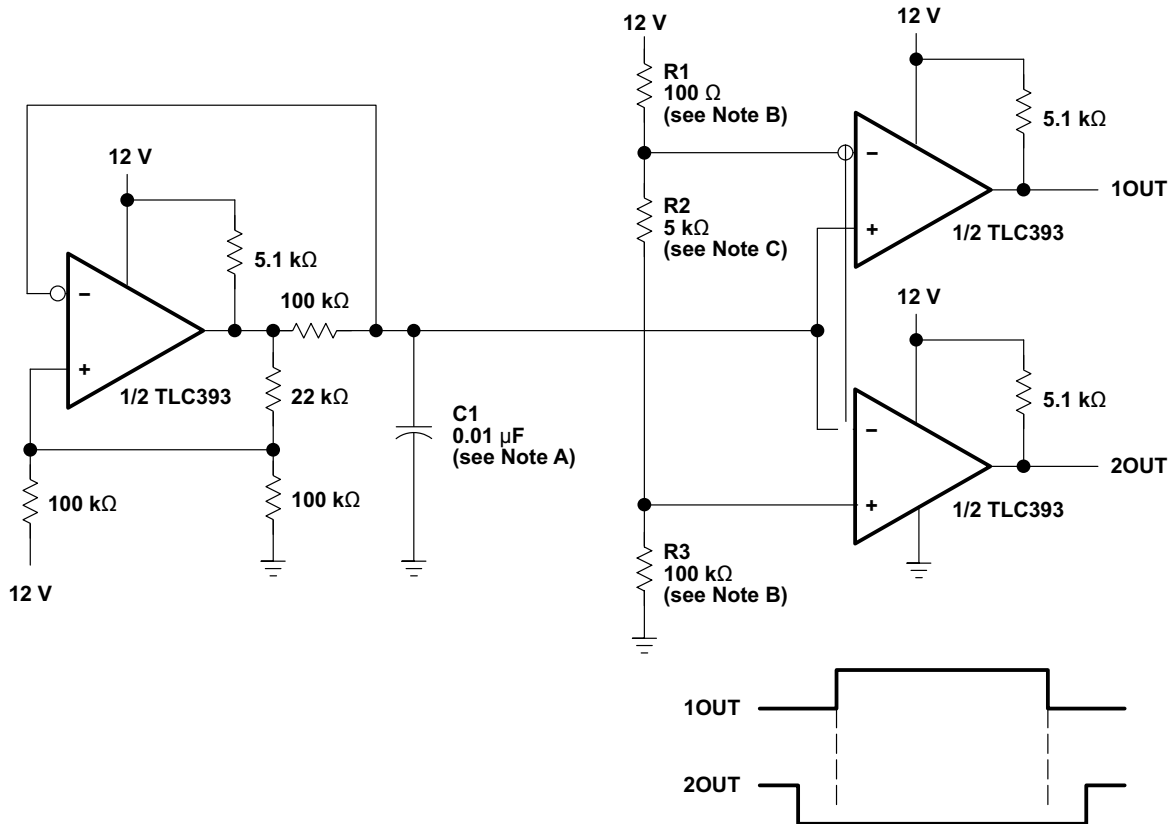
Figure 19. Pulse-Width-Modulated Motor Speed Controller



Monitors 5-VDC Rail  
Monitors 12-VDC Rail  
Early Power Fail Warning

- A.  $V_{UNREG} = 2.5 \frac{(R1 + R2)}{R2}$
- B. The value of  $C_T$  determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor



- A. Adjust C1 for a change in oscillator frequency where:  
 $1/f = 1.85(100\text{ k}\Omega)C1$
- B. Adjust R1 and R3 to change duty cycle
- C. Adjust R2 to change deadtime

**Figure 21. Two-Phase Nonoverlapping Clock Generator**

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**REVISION HISTORY**

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**Changes from Original (September 2004) to Revision A** **Page**

- Deleted Feature: Qualified in Accordance With AEC-Q100 ..... 1
  - Deleted Feature: Customer-Specific Configuration Control... ..... 1
- 

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**Changes from Revision A (April 2008) to Revision B** **Page**

- Added Feature: AEC Q100 Qualified with the Following Results: ..... 1
  - Deleted the TSSOP (PW) Package from the Ordering Information table ..... 1
  - Added Electrostatic discharge (ESD) to the Absolute Maximum table ..... 2
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC393QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393Q1	<a href="#">Samples</a>
TLC393QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C393Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLC393-Q1 :**



- Catalog: [TLC393](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

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