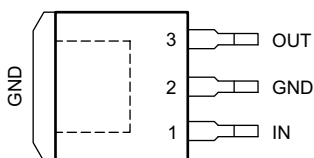
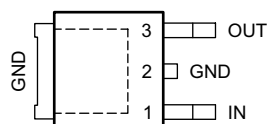
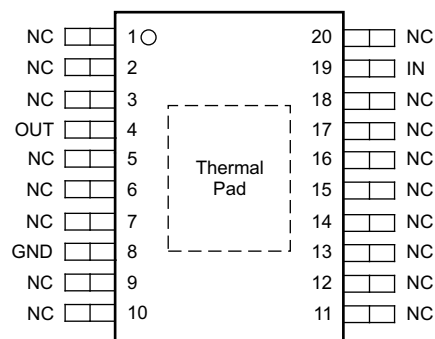


## LOW-DROPOUT VOLTAGE REGULATOR

Check for Samples: [TL720M05-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- Output Voltage of  $5\text{ V} \pm 2\%$
- Very Low Current Consumption
- Very Low Dropout Voltage
- Short-Circuit Protection
- Reverse-Polarity Protection
- ESD Protection > 6 kV

**KTT (TO-263) Package  
(Top View)**

**KVU (TO-252) Package  
(Top View)**

**PWP (HTSSOP) Package  
(Top View)**


### DESCRIPTION

The TL720M devices are monolithic integrated low-dropout voltage regulators offered in 3-pin TO packages. They regulate an input voltage up to 45 V to  $V_{OUT}$  of 5 V with 2% tolerance. The devices can drive loads up to 450 mA and are short-circuit proof. At overtemperature, the incorporated temperature protection turns off the TL720M devices.

The input capacitor ( $C_{IN}$ ) compensates for line fluctuation. Using a resistor of approximately  $1\ \Omega$  in series with  $C_{IN}$  dampens the oscillation of input inductivity and input capacitance. The output capacitor ( $C_{OUT}$ ) stabilizes the regulation circuit. Output is stable at  $C_{OUT} \geq 22\ \mu\text{F}$  and  $\text{ESR} \leq 5\ \Omega$ , within the operating temperature range.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

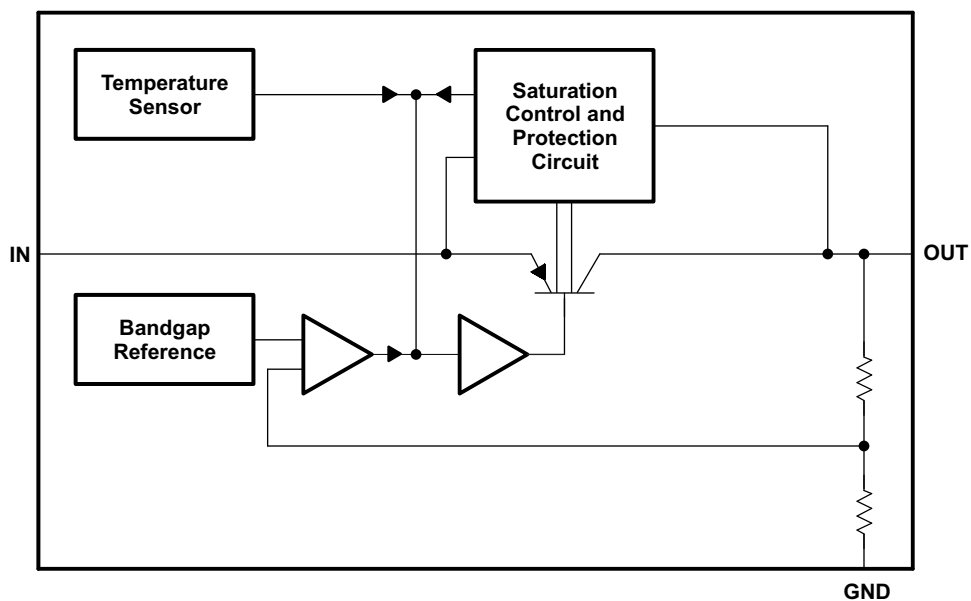


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PIN FUNCTIONS**

NAME	NO.			DESCRIPTION
	KTT	KVU	PWP	
IN	1	1	19	Input voltage. Connect to ground as close to device as possible, through a ceramic capacitor.
GND	2	2	8	Ground. Internally connected to heatsink
OUT	3	3	4	Output. Connect to ground with $\geq 22\text{-}\mu\text{F}$ capacitor, ESR $< 5\ \Omega$ at 10 kHz.
NC	–	–	1–3, 5–7, 9–18, 20	Not connected

**FUNCTIONAL BLOCK DIAGRAM**



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-42	45	V
V <sub>O</sub>	Output voltage range	-1	40	V
T <sub>J</sub>	Operating virtual-junction temperature range	-40	150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	TL720M05-Q1			UNIT	
	KTT	KVU	PWP		
	3 PINS	3 PINS	20 PINS		
θ <sub>JA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	34.2	45.3	39.3	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance <sup>(3)</sup>	38.2	36.8	22.7	°C/W
θ <sub>JB</sub>	Junction-to-board thermal resistance <sup>(4)</sup>	44.9	30.8	19.1	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter <sup>(5)</sup>	6	2.8	0.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter <sup>(6)</sup>	44.5	30.2	18.9	°C/W
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	0.8	0.7	1.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>I</sub>	Input voltage	5.5	42	V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C
T <sub>J</sub>	Operating virtual-junction temperature	-40	150	°C

## ELECTRICAL CHARACTERISTICS

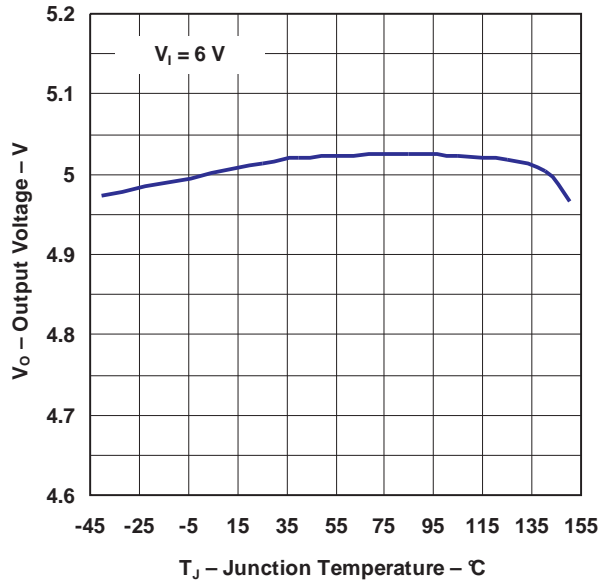
over recommended operating free-air temperature range,  $V_I = 13.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted)  
(see [Figure 1](#))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_O$	Output voltage	$I_O = 5\text{ mA}$ to $400\text{ mA}$ , $V_I = 6\text{ V}$ to $28\text{ V}$	4.9	5	5.1	V
		$I_O = 5\text{ mA}$ to $200\text{ mA}$ , $V_I = 6\text{ V}$ to $40\text{ V}$	4.9	5	5.1	
$I_O$	Output current limit		450	700	950	mA
$I_Q$	Current consumption $I_q = I_I - I_O$	$I_O = 1\text{ mA}$	$T_J = 25^\circ\text{C}$	100	220	$\mu\text{A}$
			$T_J \leq 85^\circ\text{C}$	100	220	
		$I_O = 250\text{ mA}$		5	10	mA
		$I_O = 400\text{ mA}$		12	22	
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$I_O = 300\text{ mA}$ , $V_{do} = V_I - V_O$		250	500	mV
	Load regulation	$I_O = 5\text{ mA}$ to $400\text{ mA}$		15	30	mV
	Line regulation	$\Delta V_I = 8$ to $32\text{ V}$ , $I_O = 5\text{ mA}$	-15	5	15	mV
PSRR	Power-supply ripple rejection	$f_r = 100\text{ Hz}$ , $V_r = 0.5\text{ V}_{pp}$		60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift			0.5		mV/K

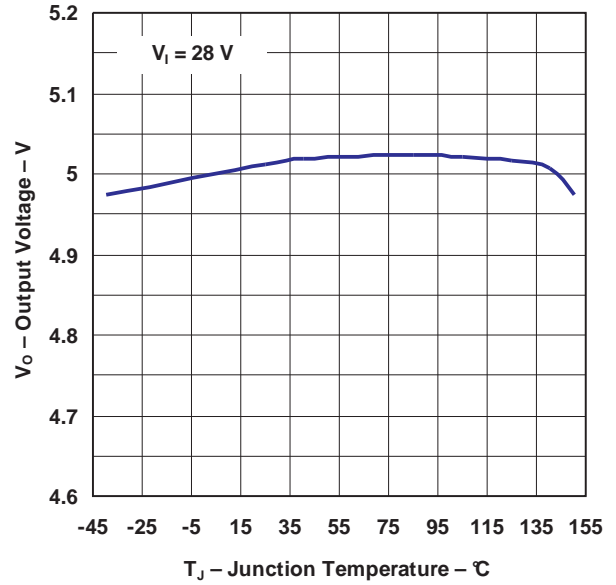
(1) Measured when the output voltage  $V_O$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{ V}$

TYPICAL CHARACTERISTICS

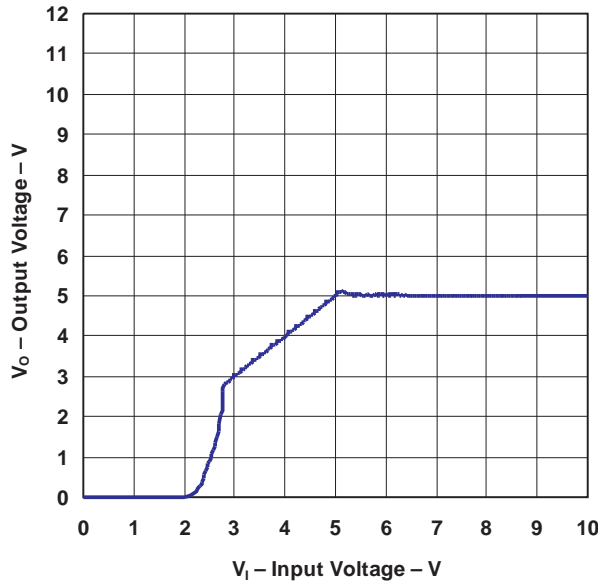
OUTPUT VOLTAGE  
VS  
JUNCTION TEMPERATURE



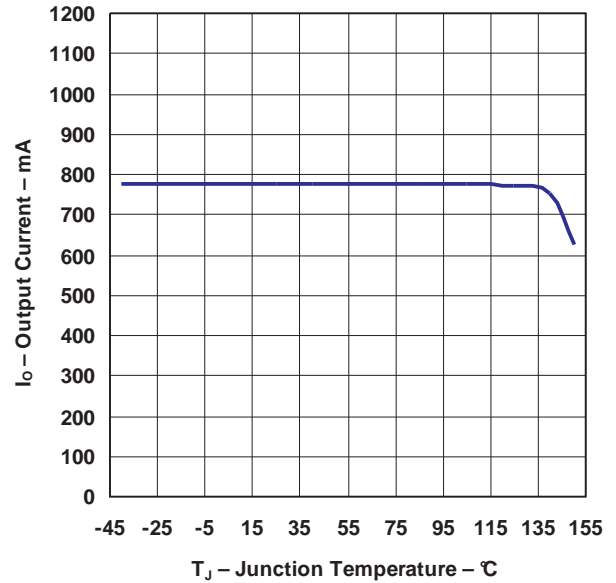
OUTPUT VOLTAGE  
VS  
JUNCTION TEMPERATURE



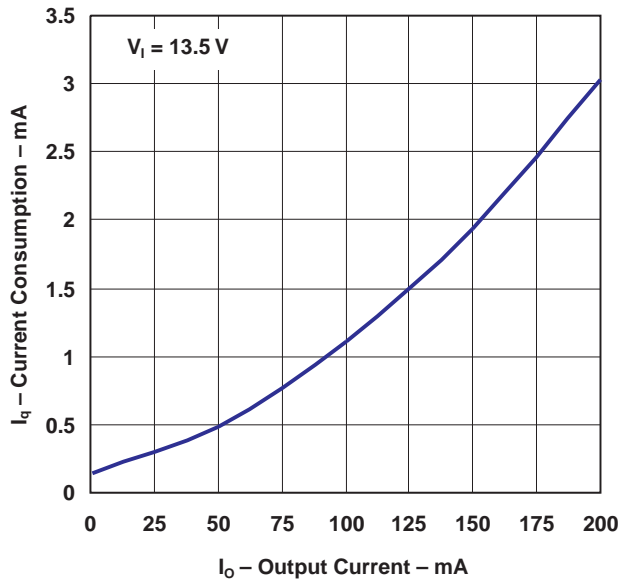
OUTPUT VOLTAGE  
VS  
INPUT VOLTAGE



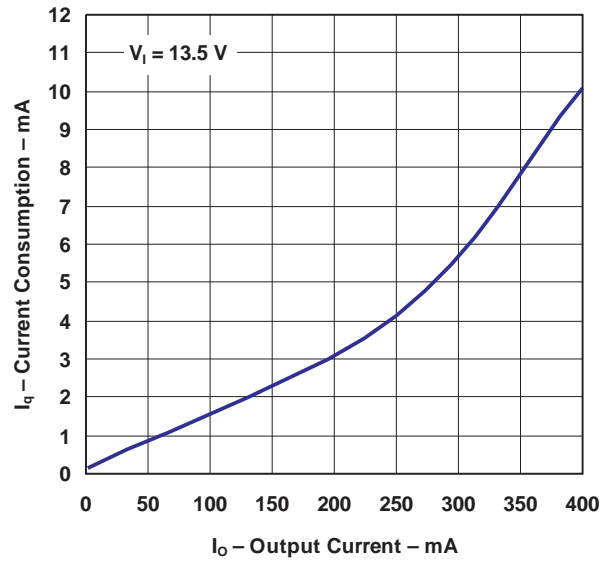
OUTPUT CURRENT  
VS  
JUNCTION TEMPERATURE



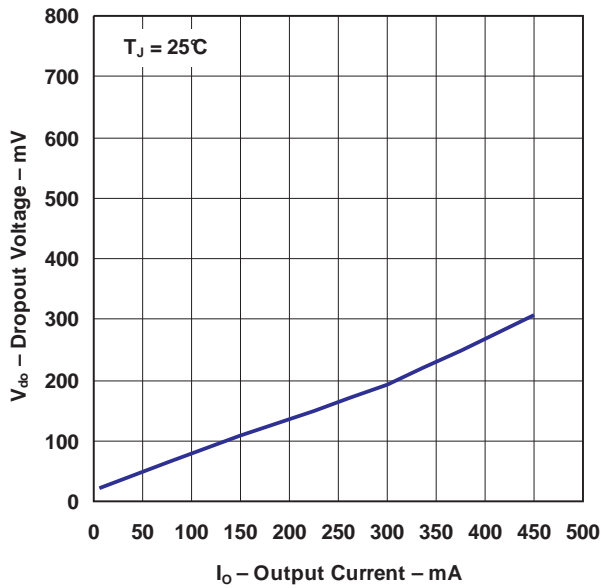
**TYPICAL CHARACTERISTICS (continued)**  
**CURRENT CONSUMPTION**  
**vs**  
**OUTPUT CURRENT**



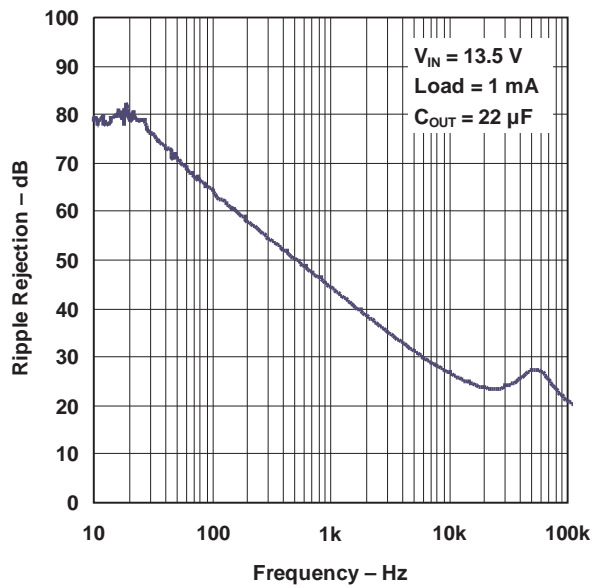
**CURRENT CONSUMPTION**  
**vs**  
**OUTPUT CURRENT**



**DROPOUT VOLTAGE**  
**vs**  
**OUTPUT CURRENT**

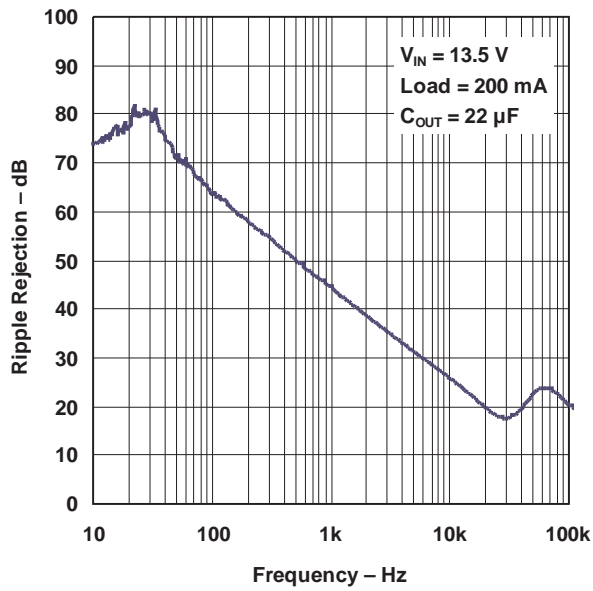


**POWER-SUPPLY RIPPLE REJECTION**  
**vs**  
**FREQUENCY**

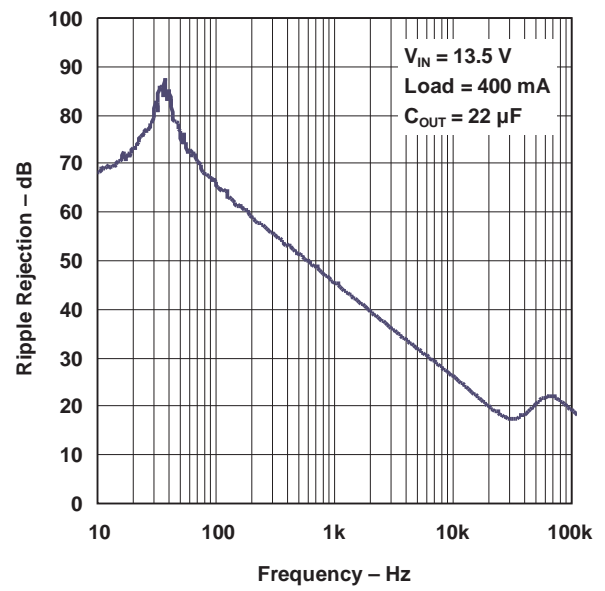


**TYPICAL CHARACTERISTICS (continued)**

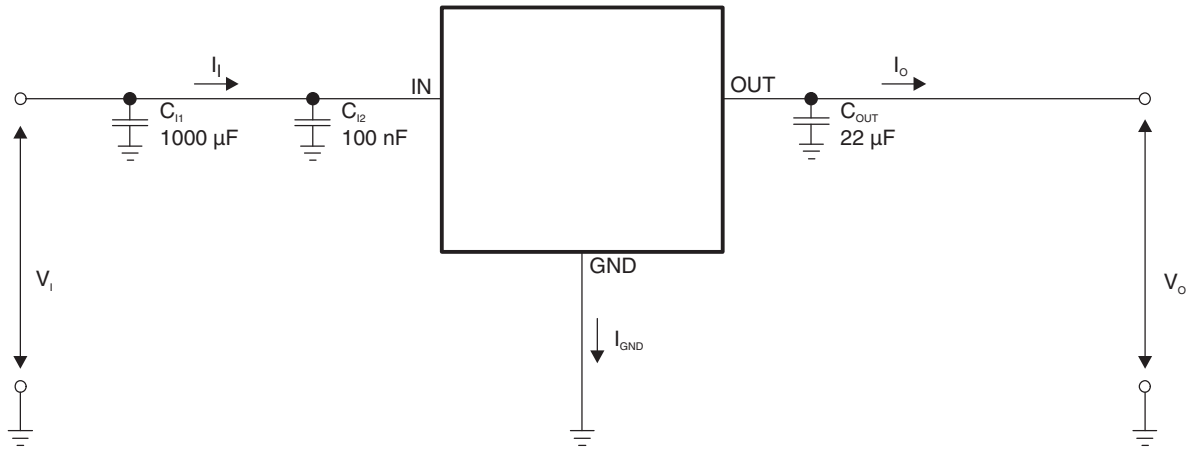
**POWER-SUPPLY RIPPLE REJECTION  
VS  
FREQUENCY**



**POWER-SUPPLY RIPPLE REJECTION  
VS  
FREQUENCY**



**PARAMETER MEASUREMENT INFORMATION**



**Figure 1. Test Circuit**



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**REVISION HISTORY**

<b>Changes from Revision F (May 2013) to Revision G</b>	<b>Page</b>
• Removed Ordering Information table. ....	<a href="#">1</a>

---

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL720M05QKTRRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	T720M05Q	<a href="#">Samples</a>
TL720M05QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	720M05Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL720M05QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



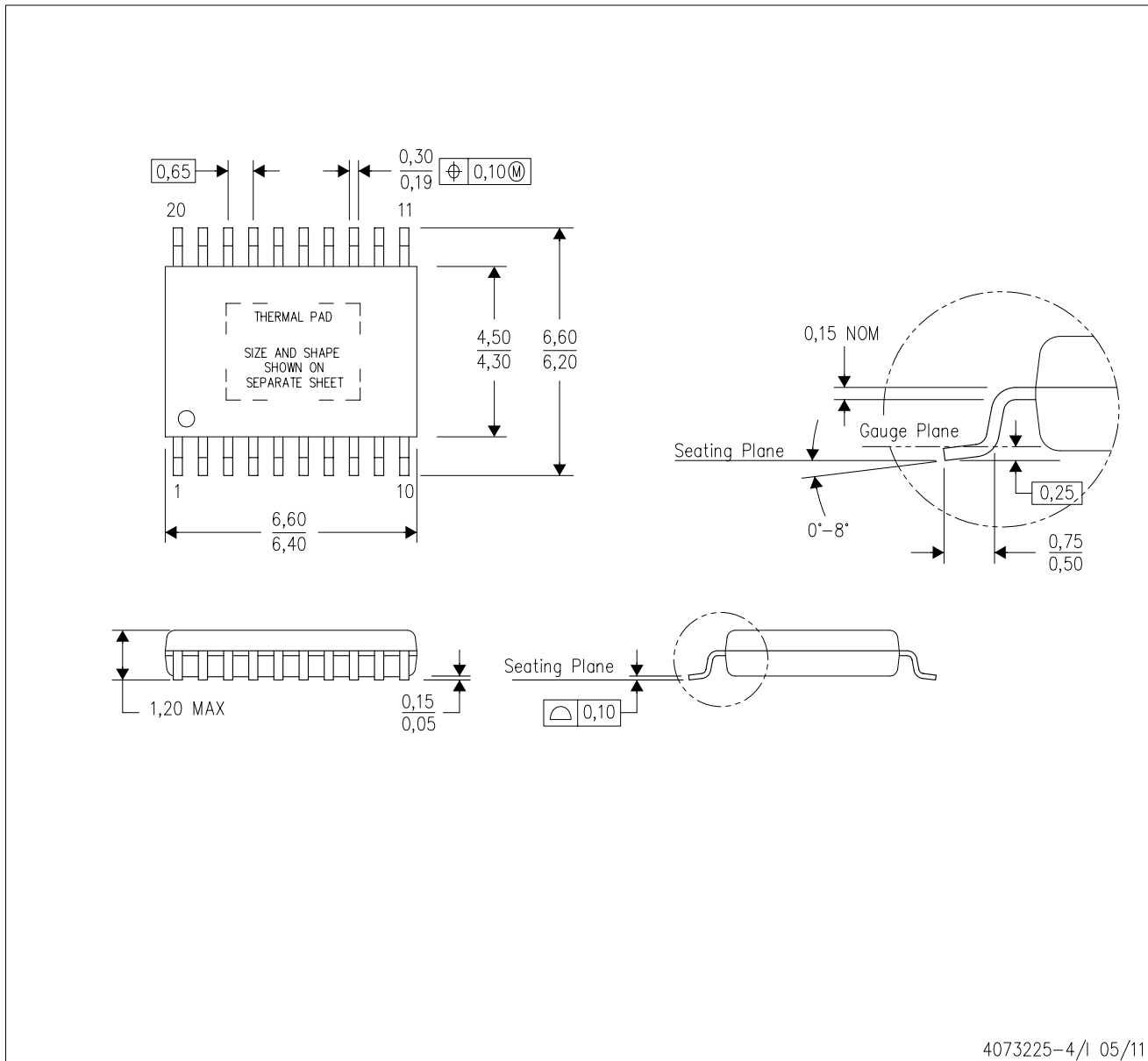
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL720M05QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0

# MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



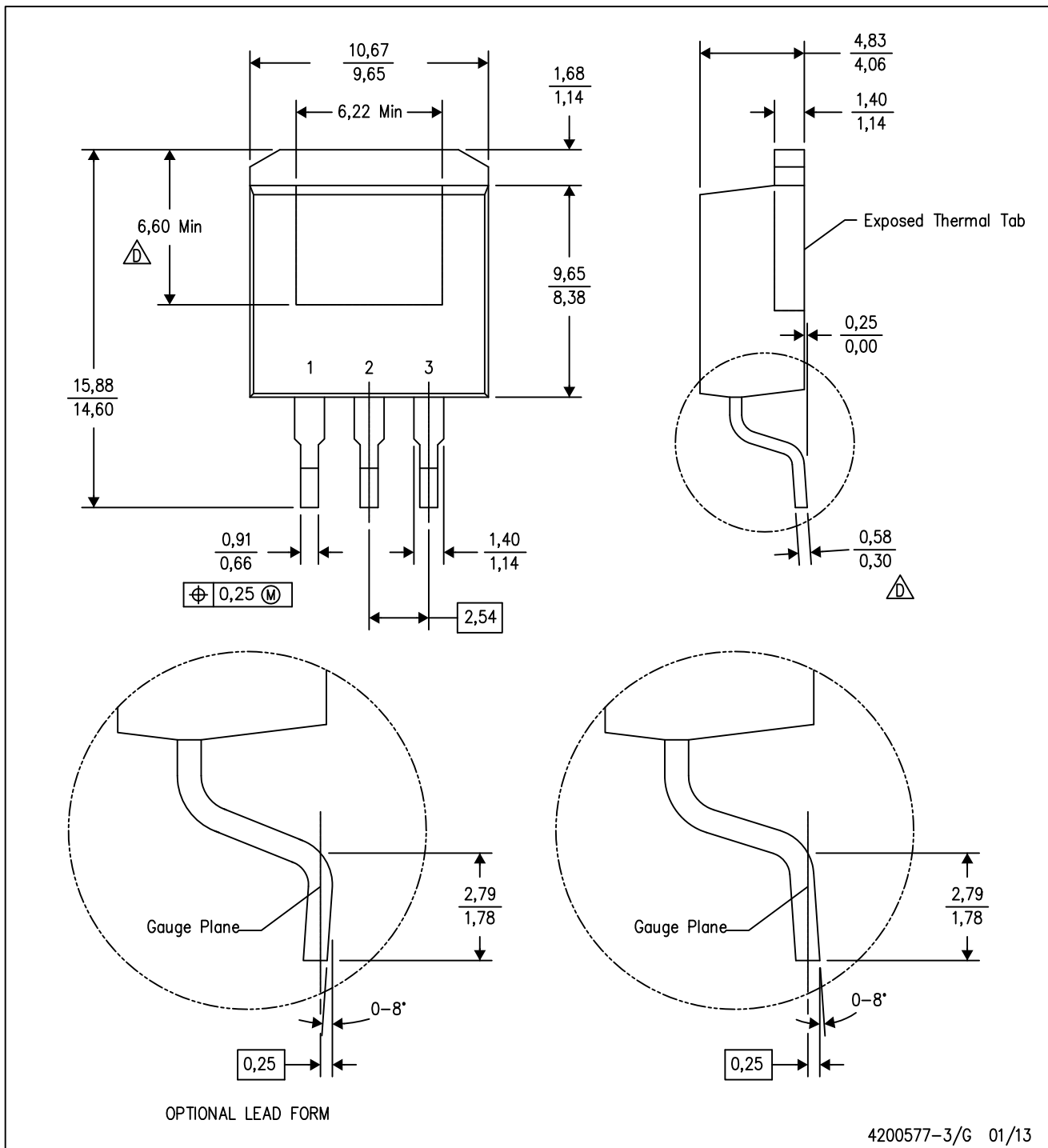
4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

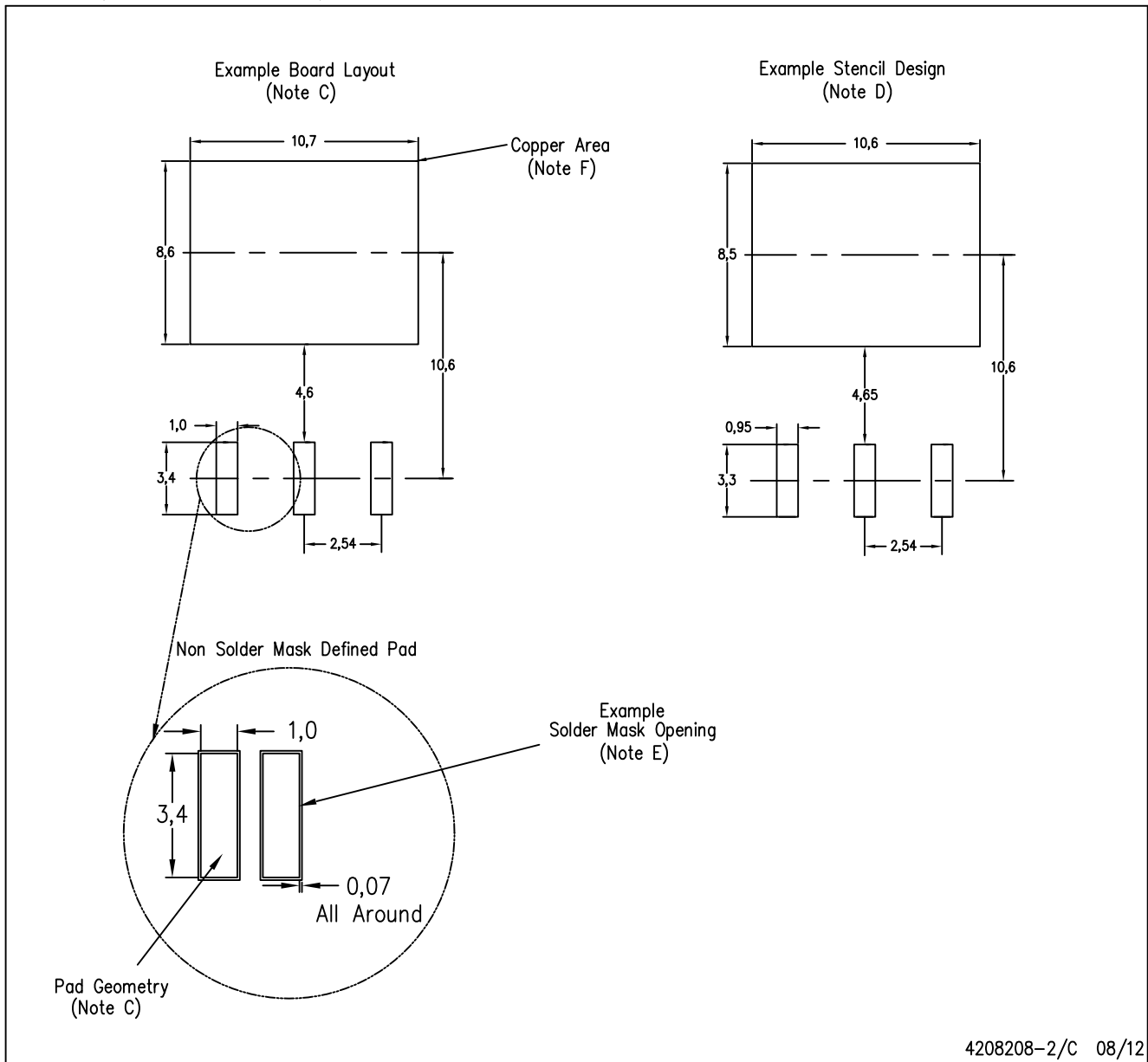


4200577-3/G 01/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
  - (D) Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

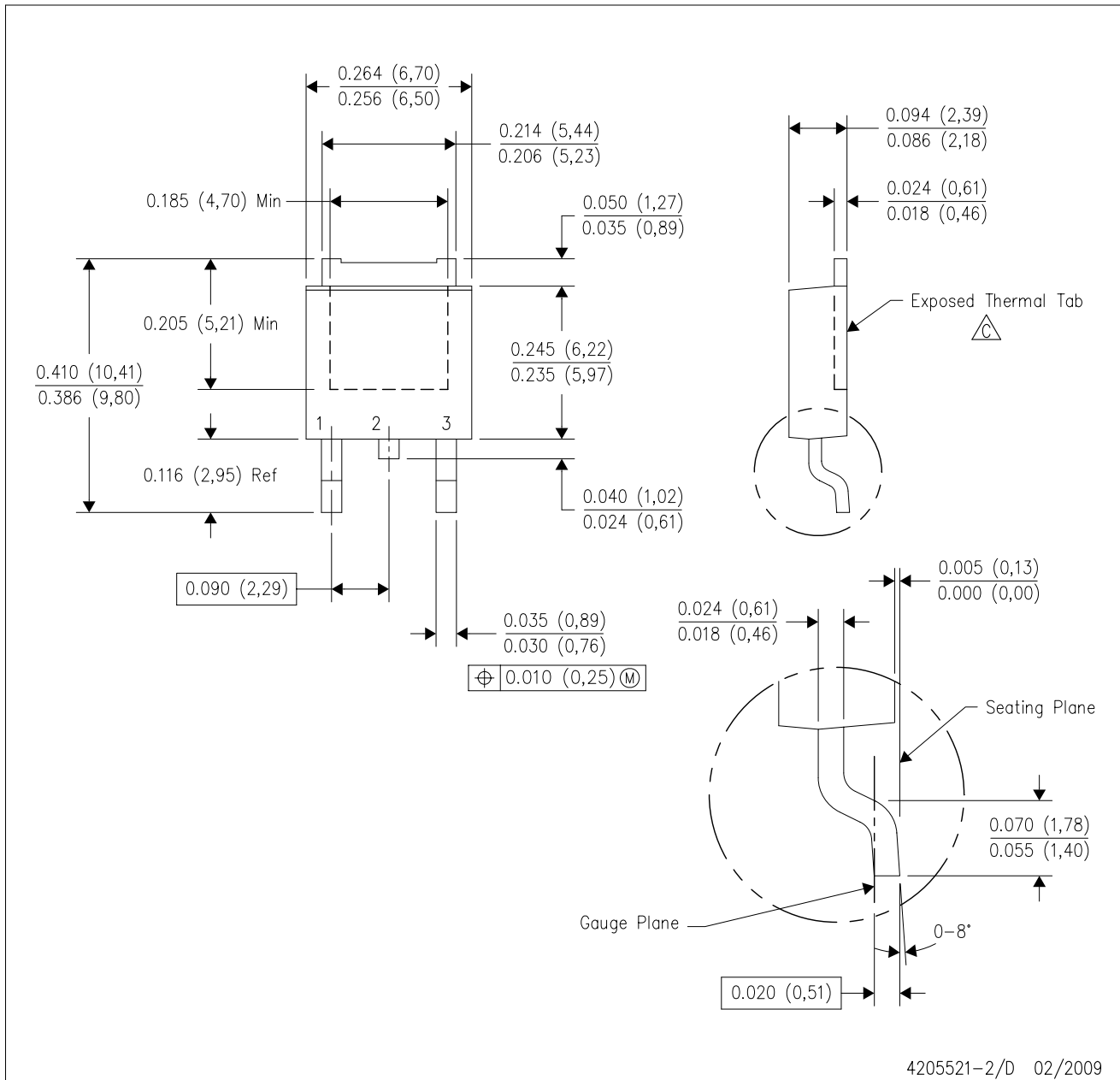


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
  - This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

# MECHANICAL DATA

KVU (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

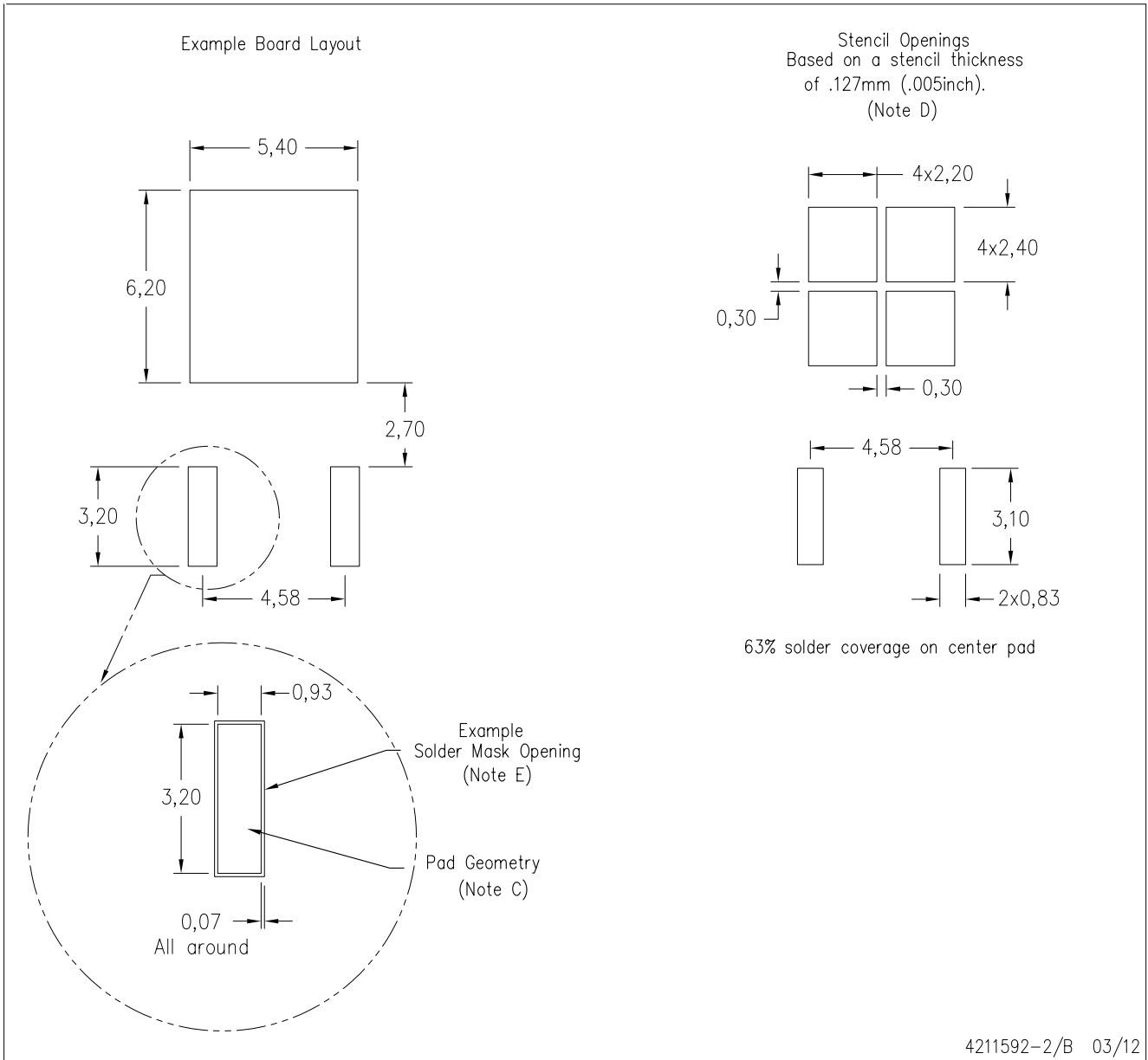


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - △ The center lead is in electrical contact with the exposed thermal tab.
  - D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
  - E. Falls within JEDEC TO-252 variation AA.



KVU (R-PSFM-G3)

PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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