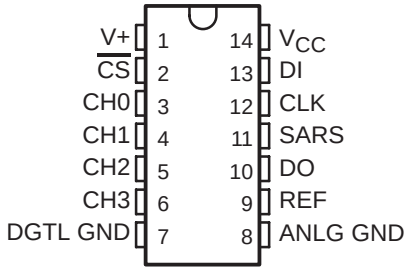
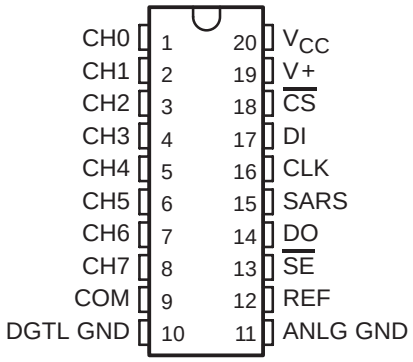
- **8-Bit Resolution**
- **Easy Microprocessor Interface or Stand-Alone Operation**
- **Operates Ratiometrically or With 5-V Reference**
- **4- or 8-Channel Multiplexer Options With Address Logic**
- **Shunt Regulator Allows Operation With High-Voltage Supplies**
- **Input Range 0 to 5 V With Single 5-V Supply**
- **Remote Operation With Serial Data Link**
- **Inputs and Outputs are Compatible With TTL and MOS**
- **Conversion Time of 32 µs at f_{clock} = 250 kHz**
- **Designed to Be Interchangeable With National Semiconductor ADC0834 and ADC0838**

DEVICE	TOTAL UNADJUSTED ERROR	
	A SUFFIX	B SUFFIX
ADC0834	± 1 LSB	± 1/2 LSB
ADC0838	± 1 LSB	± 1/2 LSB

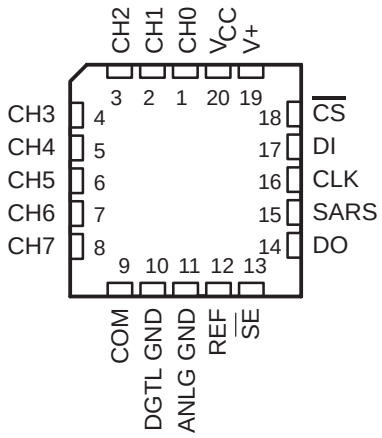
AD0834 . . . N PACKAGE
(TOP VIEW)



ADC0838 . . . N PACKAGE
(TOP VIEW)



ADC0838 . . . FN PACKAGE
(TOP VIEW)



description

These devices are 8-bit successive- approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

The ADC0834 (4-channel) and ADC0838 (8-channel) multiplexer is software configured forsingle-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0834AC, ADC0834BC, ADC0838AC, and ADC0838BC are characterized for operation from 0°C to 70°C. The ADC0834AI, ADC0834BI, ADC0838AI, and ADC0838BI are characterized for operation from −40°C to 85°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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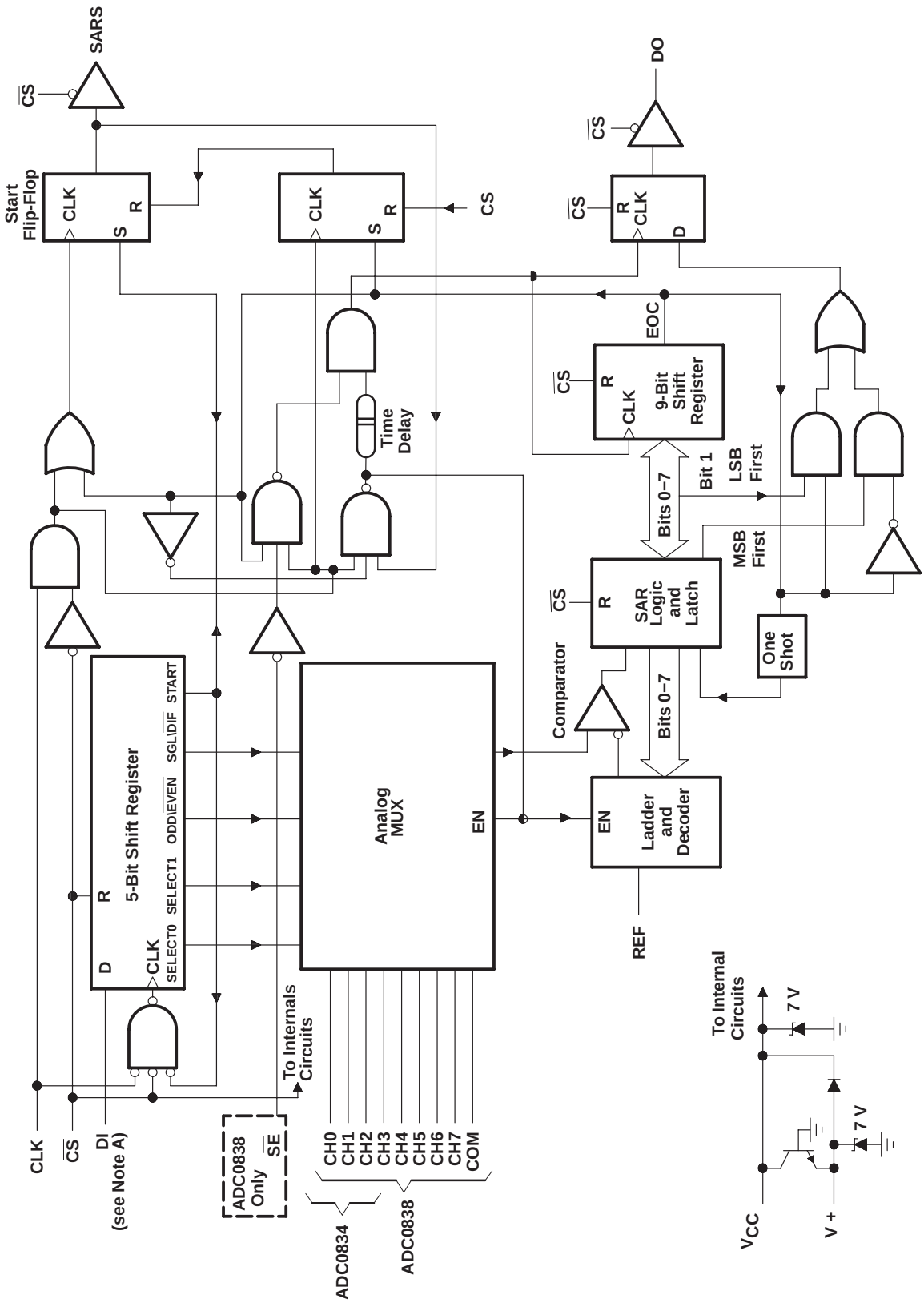
functional block diagram



NOTE A: For the ADC0834, DI is input directly to the D input of SELECT 1; SELECT 0 is forced to a high.

functional description

The ADC0834 and ADC0838 use a sample data comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of $\overline{SE}$, an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single-ended), to an adjacent input (differential), or to a common terminal (pseudo-differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (−) polarity. If the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial data link from the controlling processor. A serial-communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer addressing sequence. The multiplexer address is shifted into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single-ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs . For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the ADC0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting $\overline{CS}$ low, which enables all logic circuits. $\overline{CS}$ must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on DI is clocked into the multiplexer address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR Status output (SARS) goes high to indicate that a conversion is in progress, and DI to the multiplexer shift register is disabled the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. The data output DO comes out of the high-impedance state and provides a leading low for this one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive ladder output. As the conversion proceeds, conversion data is simultaneously output from the DO output pin, with the most significant bit (MSB) first.

After eight clock periods, the conversion is complete and the SARS output goes low.

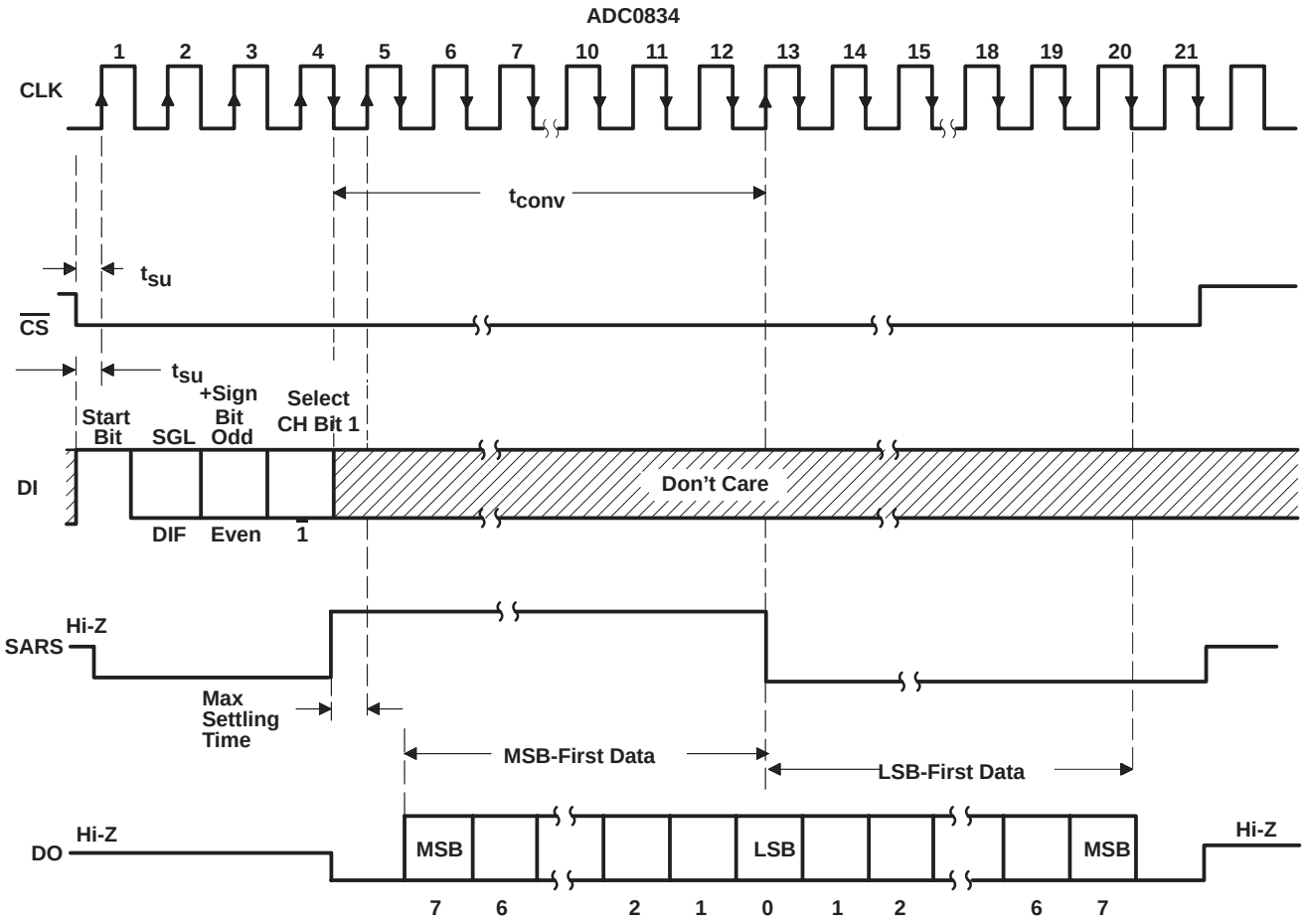
The ADC0834 outputs the least-significant-bit-first data after the MSB-first data stream. If $\overline{SE}$ is held high on the ADC0838, the value of the least significant bit (LSB) will remain on the data line. When $\overline{SE}$ is forced low, the data is then clocked out as LSB-first data. (To output LSB first, $\overline{SE}$ must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When $\overline{CS}$ goes high, all internal registers are cleared. At this time the output circuits go to the high-impedance state. If another conversion is desired, $\overline{CS}$ must make a high-to-low transition followed by address information.

functional description (continued)

DI and DO can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because DI is only examined during the multiplexer addressing interval and DO is still in a high-impedance state.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

sequence of operation



ADC0834 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/$\overline{\text{DIF}}$	ODD/$\overline{\text{EVEN}}$	SELECT BIT 1	O	1	2	3
L	L	L	+	−		
L	L	H			+	−
L	H	L	−	+		
L	H	H			−	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, − or + = polarity of selected input pin

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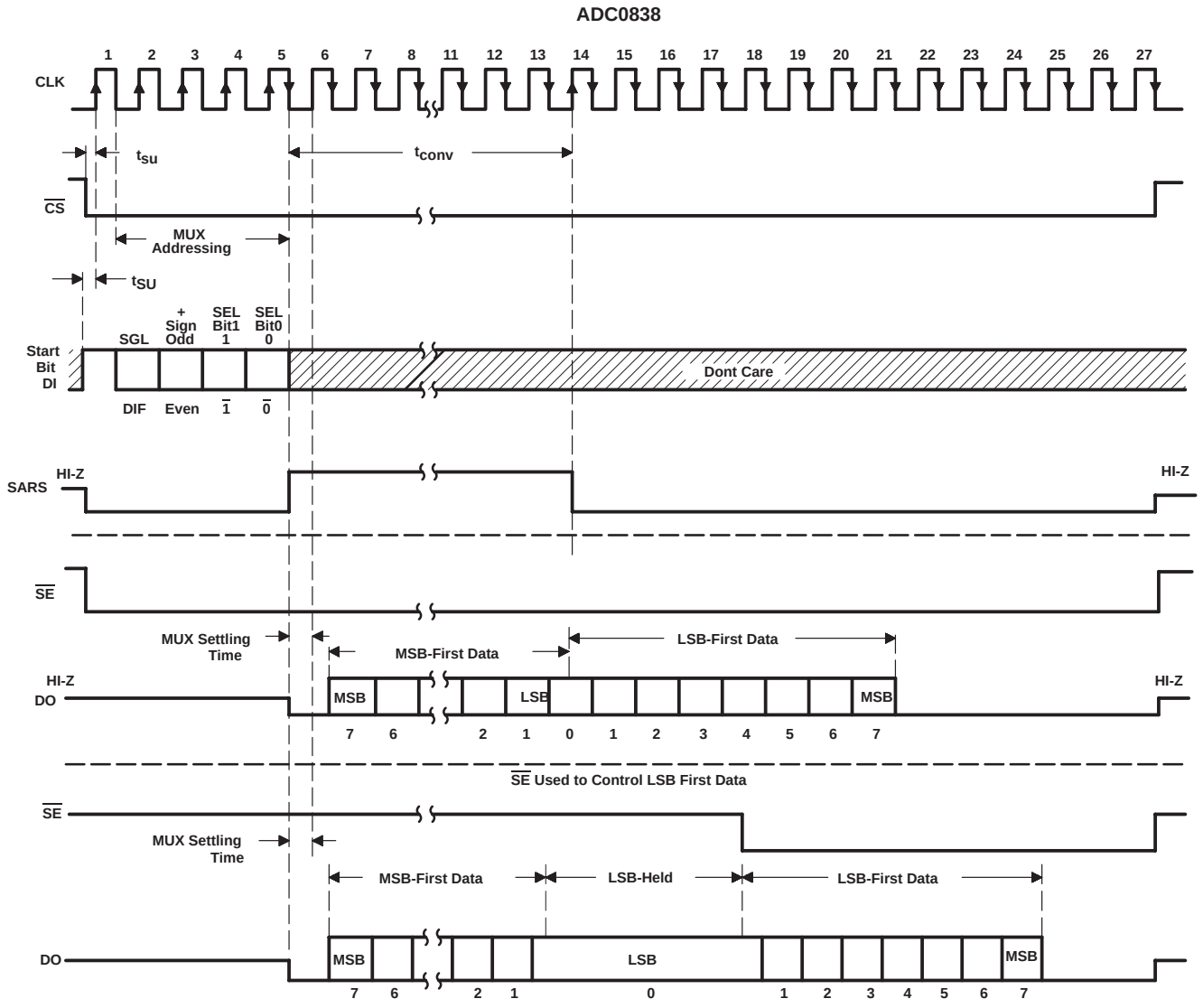
sequence of operation



ADC0838 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/$\overline{\text{DIF}}$	ODD/$\overline{\text{EVEN}}$	SELECT		0		1		2		3		
		1	0	0	1	2	3	4	5	6	7	
L	L	L	L	+	−							
L	L	L	H			+	−					
L	L	H	L					+	−			
L	L	H	H							+	−	
L	H	L	L	−	+							
L	H	L	H			−	+					
L	H	H	L					−	+			
L	H	H	H							−	+	
H	L	L	L	+								−
H	L	L	H			+						−
H	L	H	L					+				−
H	L	H	H							+		−
H	H	L	L		+							−
H	H	L	H				+					−
H	H	H	L						+			−
H	H	H	H								+	−

H = high level, L = low level, − or + = polarity of selected input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC}+ 0.3 V
Input current: V+ input . . . . . 15 mA
Any other input . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: AC and BC suffixes . . . . . 0°C to 70°C
AI and BI suffixes . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resist or is recommended to limit current into the V+ input.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 3)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high		220			ns
t_{su}	Setup time, $\overline{CS}$ low, $\overline{SE}$ low, or data valid before clock↑		350			ns
t_h	Hold time, data valid after clock↑		90			ns
T_A	Operating free-air temperature	AC and BC suffixes	0		70	°C
		AI and BI suffixes	−40		85	

NOTE 3: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 µs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		AC, BC SUFFIX			AI, BI SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-levl output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 µA	2.8			2.4			V
		V_{CC} = 4.75 V,	I_{OH} = −10 µA	4.6			4.5			
V_{OL}	Low-levl output voltage	V_{CC} = 5.25 V,	I_{OH} = 1.6 mA			0.34			0.4	V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	µA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	µA
I_{OH}	High-level output (source) current	V_{OH} = 0,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO or SARS)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	µA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance							5		pF
C_o	Output capacitance							5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).
‡ All typical values are at V_{CC} = V+ = 5 V, T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V + = 5 V, f_{clock} = 250 kHz (unless otherwise noted) (continued)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 3	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby input current (see Note 4)	On-channel	V_I = 5 V			1	µA
		Off-channel	V_I = 0			−1	
		On-channel	V_I = 0			−1	
		Off−channel	V_I = 5 V			1	
$r_{i(REF)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_Z	Internal zener diode breakdown voltage	I_I = 15 mA at V+ pin, See Note 2	6.3	7	8.5	V
I_{CC}	Supply current			1	2.5	mA

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, V+ = 5 V, T_A = 25°C.

NOTES: 4. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

5. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} .Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog input s that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.950 V for all variations of temperature and load.

6. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics V + = 5 V, f_{clock} = 250 kHz, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	AI, AC SUFFIX			BI, BC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 6)		V_{ref} = 5 V, T_A = MIN to MAX			±1			±1/2	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
	Change in zero-error from V_{CC} = 5 V to internal zener diode operation (see Note 2)		I_I = 15 mA at V+ pin, V_{ref} = 5 V, V_{CC} open			1			1	LSB
t_{pd}	Propagation delay time, output data after CLK↓, (see Note 7)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dos}	Output disable time, DO or SARS after CS↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)					8			8	clock periods

† All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES:2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

6. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

7. The most significant bit (MSB) data is output directly from the comparator and therefore requires additional delay to allow for comparator response time.

PARAMETER MEASUREMENT INFORMATION

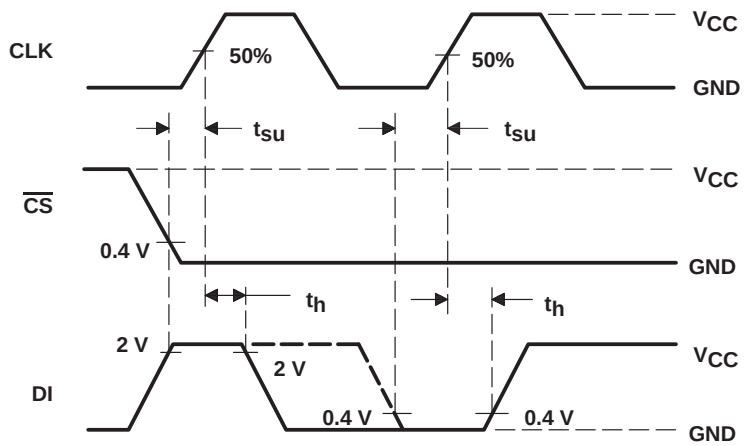


Figure 1. Data Input Timing

PARAMETER MEASUREMENT INFORMATION

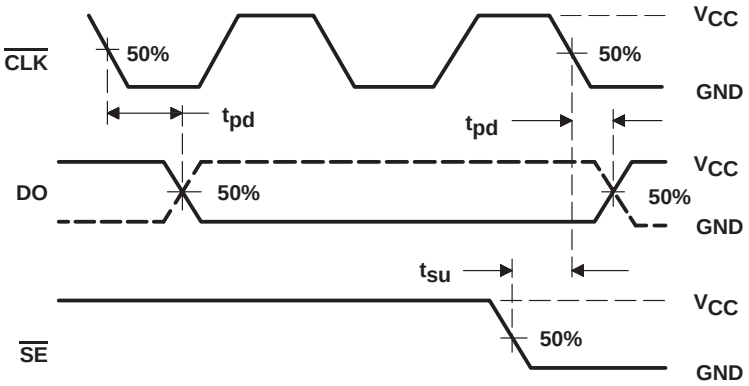
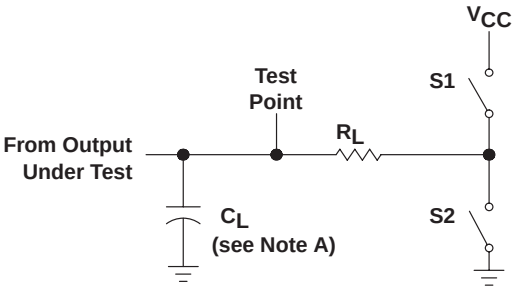
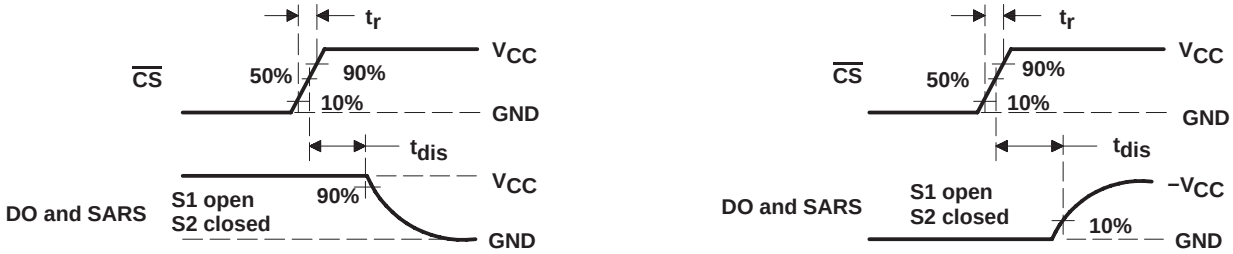


Figure 2. Data Output Timing



LOAD CIRCUIT



VOLTAGE WAVEFORMS **VOLTAGE WAVEFORMS**

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR vs REFERENCE VOLTAGE

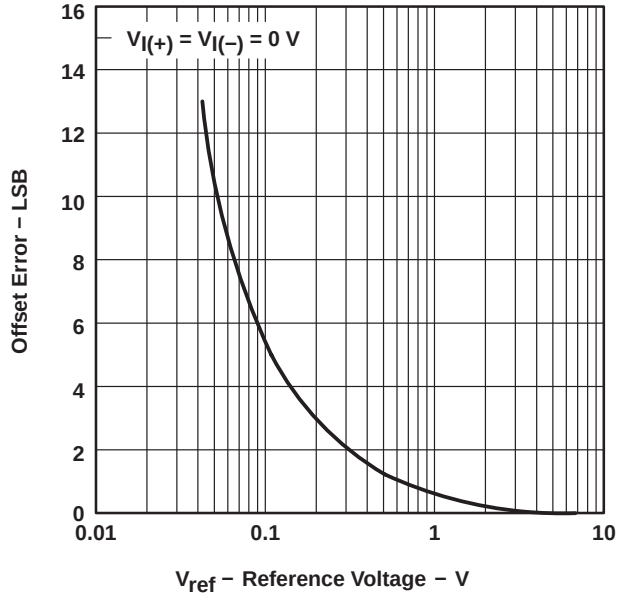

Figure 4

LINEARITY ERROR vs REFERENCE VOLTAGE

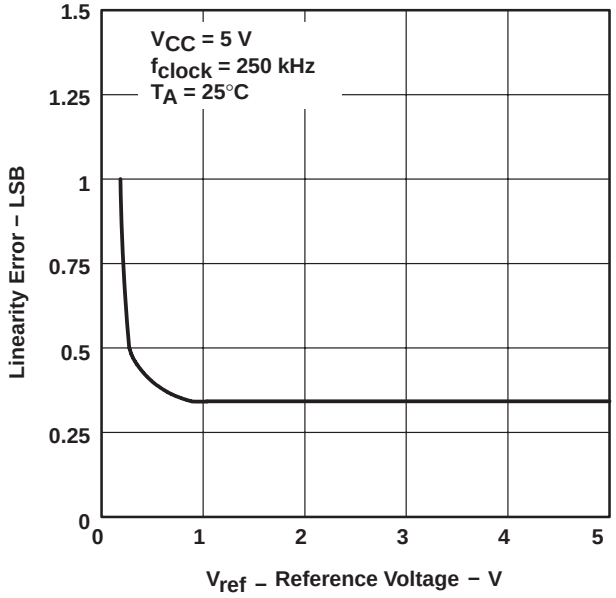

Figure 5

LINEARITY ERROR vs FREE-AIR TEMPERATURE

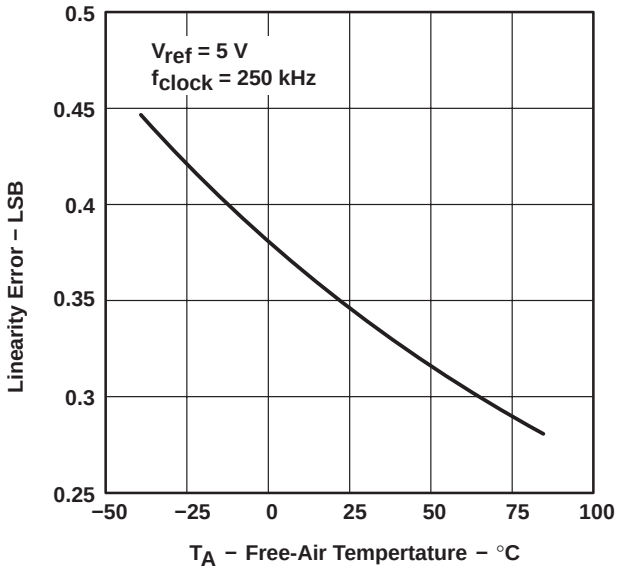

Figure 6

LINEARITY ERROR vs CLOCK FREQUENCY

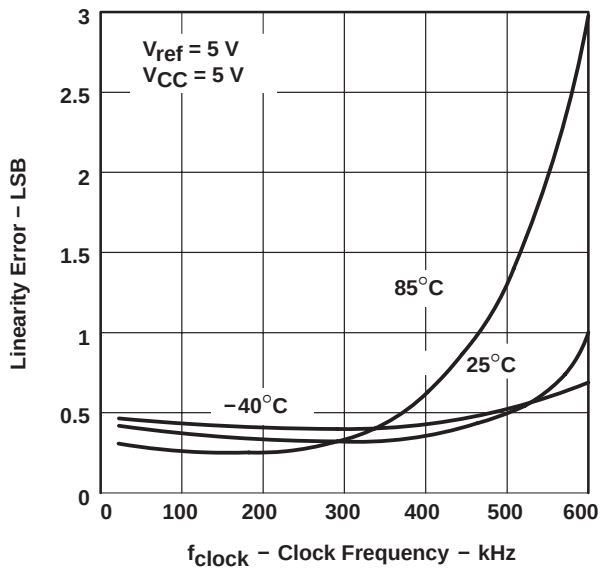

Figure 7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

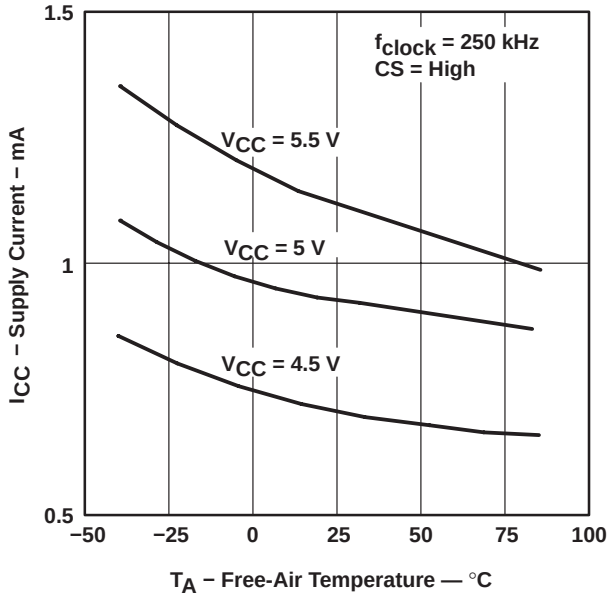

Figure 8

SUPPLY CURRENT vs CLOCK FREQUENCY

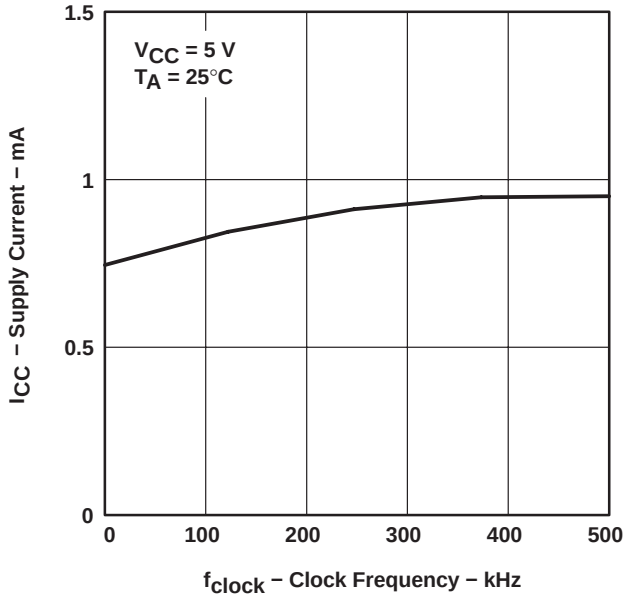

Figure 9

OUTPUT CURRENT vs FREE-AIR TEMPERATURE

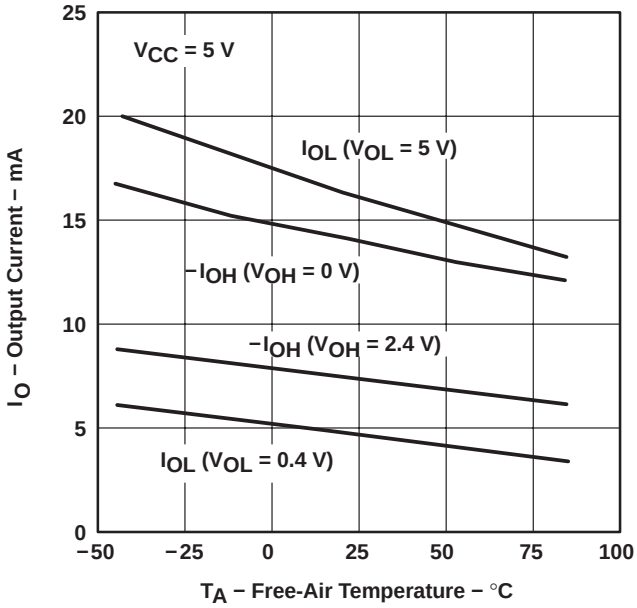

Figure 10

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